GaN High Power Amplifier, 25 W
6 – 18 GHz

CMPA601J025F
Rev. V1

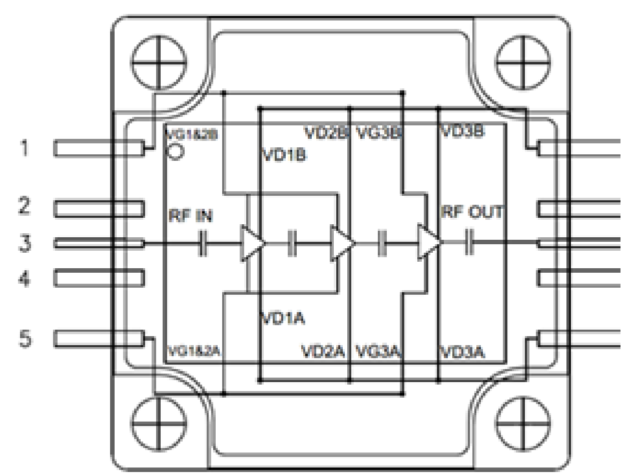
Features

- Saturated Power: 25 W
- Power Added Efficiency: 20%
- Large Signal Gain: 20 dB
- Small Signal Gain: 30 dB
- Input Return Loss: -10 dB
- Output Return Loss: -8 dB
- CW operation

Applications

- Electronic Warfare
- Test Instrumentation
- Radar
- Broadband Amplifiers

Functional Schematic



Description

MACOM's CMPA601J025F is a 25 W package MMIC HPA utilizing MACOM's high performance, 0.15µm GaN-on-SiC production process. The CMPA601J025F operates from 6 - 18 GHz and supports a variety of end applications such as electronic warfare, test instrumentation, radar and general amplification. The CMPA601J025F achieves 25 W of saturated output power with 20 dB of large signal gain and typically 20% power-added efficiency under CW operation.

Packaged in a 15 mm bolt-down, flange package, the CMPA601J025F provides superior broadband, RF performance and thermal management allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Pin Configuration[1]

Pin #	Name
1, 5	VG
2, 4, 7, 9	GND
3	RF Input
6, 10	VD
8	RF Output

1. The backside of the MMIC must be connected to RF, DC, and thermal ground

Ordering Information

Part Number	Package (MOQ/Mult)
CMPA601J025F	Tray (10/10)
CMPA601J025F-AMP	Sample Board (1/1)

DC-0030740

RF Electrical Specifications: V_D = 22 V, I_{DQ} = 1.2 A, CW, T_C = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Frequency (GHz)	Units	Min.	Typ.	Max.
Output Power	P_{IN} = 24 dBm	6.0 9.5 13.6 18.0	dBm	— 45.0 42.5 42.0	43.5 46.0 44.0 43.0	—
Power Added Efficiency	P_{IN} = 24 dBm	6.0 9.5 13.6 18.0	%	— 27 13 13	33 35 19 19	—
Large Signal Gain	P_{IN} = 24 dBm	6.0 9.5 13.6 18.0	dB	— 21.0 18.5 18.0	19.5 21.0 20.0 19.0	—
Small Signal Gain	P_{IN} = -25 dBm	6.0 9.5 13.6 18.0	dB	—	31 34 29 27	—
Input Return Loss	P_{IN} = -25 dBm	6 - 18	dB	—	-10	—
Output Return Loss	P_{IN} = -25 dBm	6 - 18	dB	—	-8	—

DC Electrical Specifications:

Parameter	Units	Min.	Typ.	Max.
Drain Voltage	V	—	22	—
Gate Voltage	V	—	-1.9	—
Quiescent Drain Current	A	—	1.2	—
Saturated Drain Current	A	—	5.5	—

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power	P_{IN}	dBm	—	24	—
Drain Voltage	V_D	V	—	22	—
Gate Voltage	V_G	V	—	-1.9	—
Quiescent Drain Current	I_{DQ}	A	—	>1.2	—
Operating Temperature	T_C	°C	-40	—	+60

Absolute Maximum Ratings[2,3]

Parameter	Symbol	Unit	Min.	Max.
Input Power	P_{IN}	dBm	—	24
Drain to Source Breakdown Voltage	V_{DS}	V	—	84
Drain Voltage	V_D	V	—	22
Gate Voltage	V_G	V	-8	+2
Drain Current	I_D	A	—	5.9
Gate Current	I_G	mA	—	11
Dissipated Power @ +85°	P_{DISS}	W	—	130
VSWR	—	Ratio	—	3:1
Junction Temperature (MTTF > 1E6 Hrs)	T_J	°C	—	+225°C
Storage Temperature	T_{STG}	°C	-55	+150
Mounting Temperature (30 seconds)	T_M	°C	—	+320
Screw Torque	τ	in-oz	—	40

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

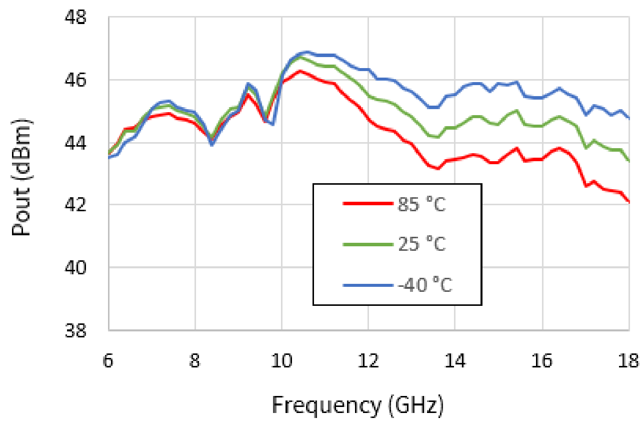
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

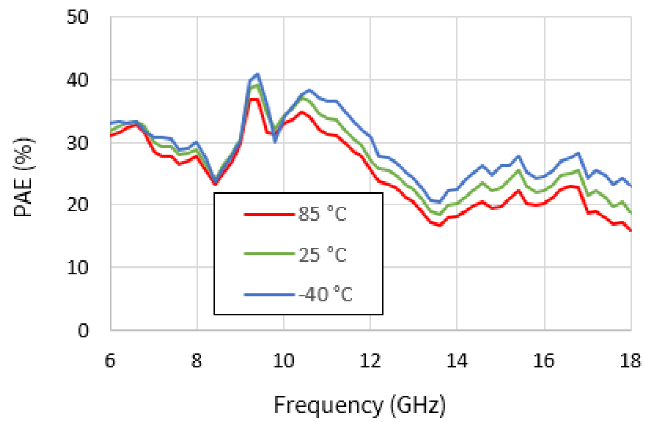
Typical Performance Curves – Large Signal over Temperature

V_D = 22 V, I_{DQ} = 1.2 A, CW, P_{IN} = 24 dBm

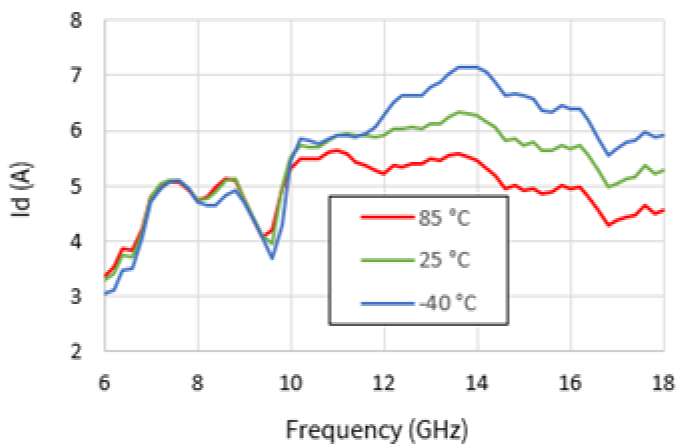
Output Power vs. Frequency



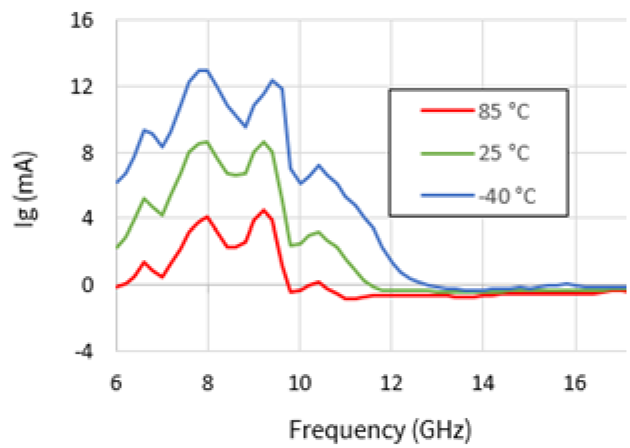
Power Added Efficiency vs. Frequency



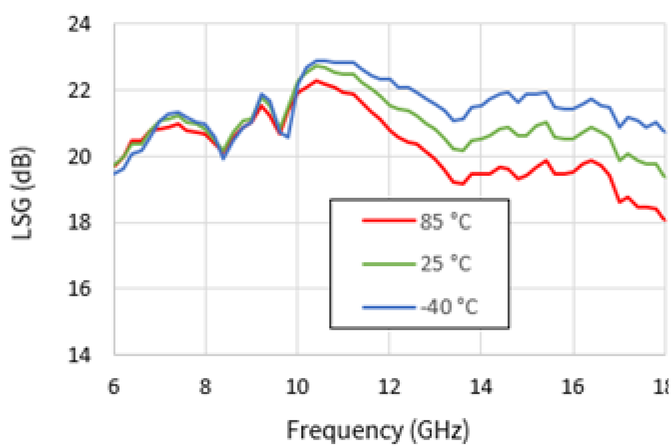
Drain Current vs. Frequency



Gate Current vs. Frequency



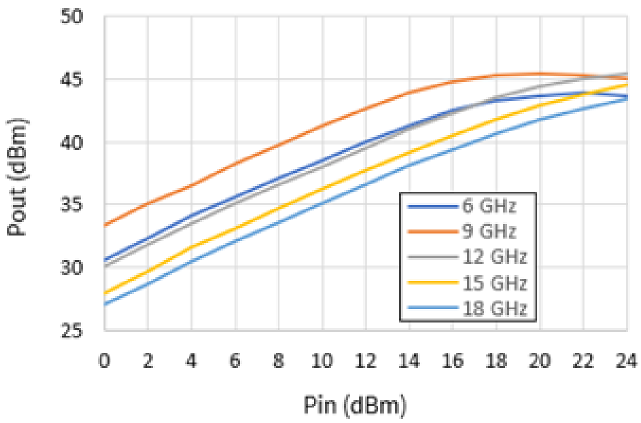
Large Signal Gain vs. Frequency



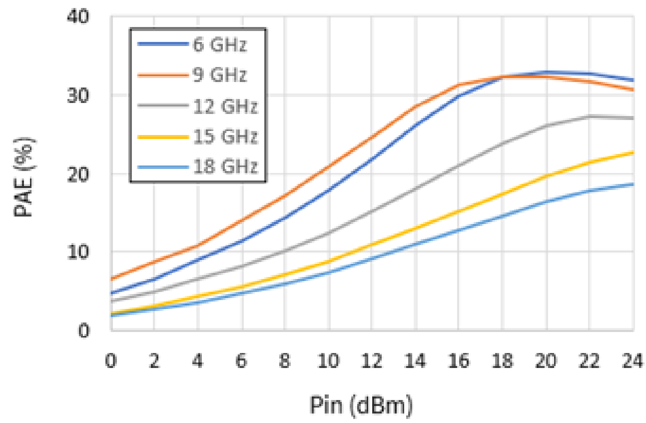
Typical Performance Curves – Drive-Up over Frequency

V_D = 22 V, I_{DQ} = 1.2 A, CW, T_C = 25°C

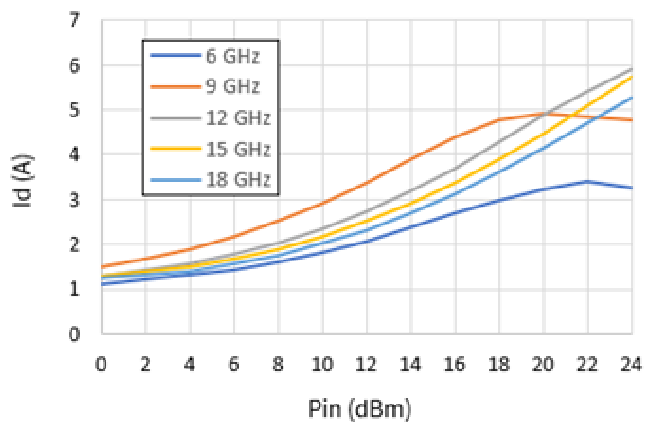
Output Power vs. Input Power



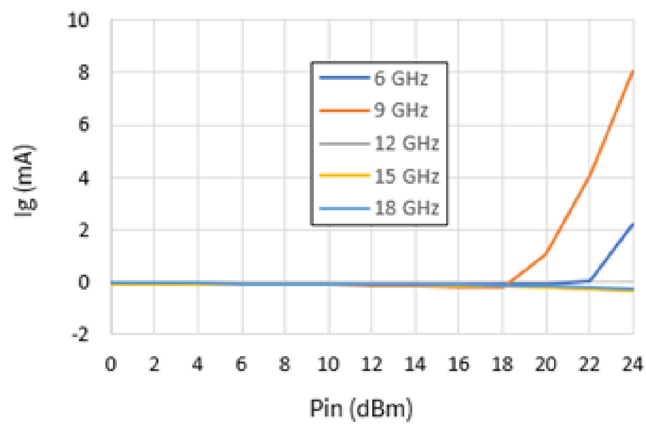
Power Added Efficiency vs. Input Power



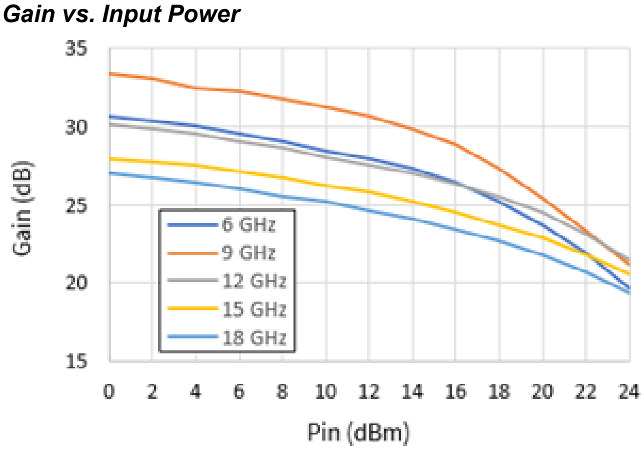
Drain Current vs. Input Power



Gate Current vs. Input Power



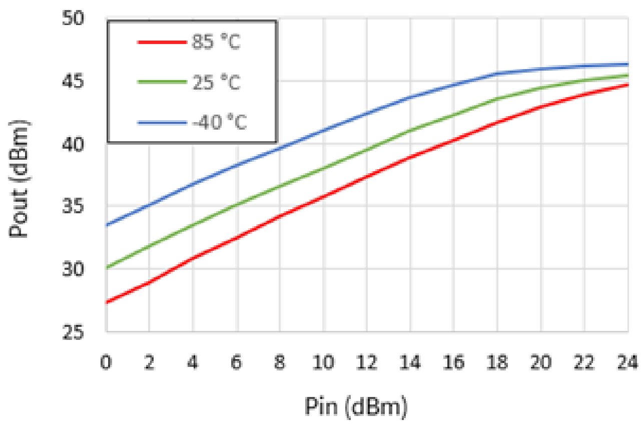
Gain vs. Input Power



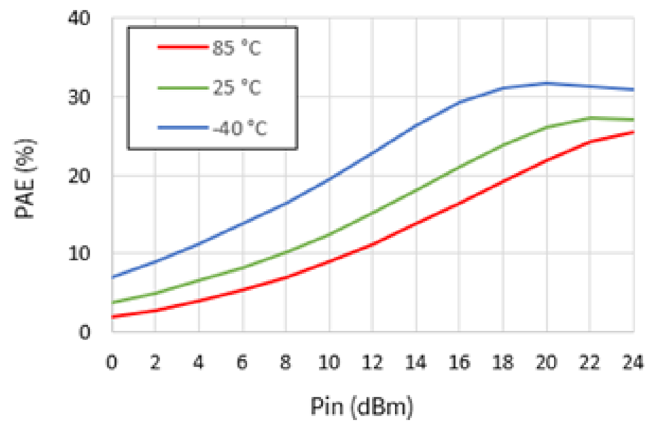
Typical Performance Curves – Drive-Up over Temperature

V_D = 22 V, I_{DQ} = 1.2 A, CW, Frequency = 12 GHz

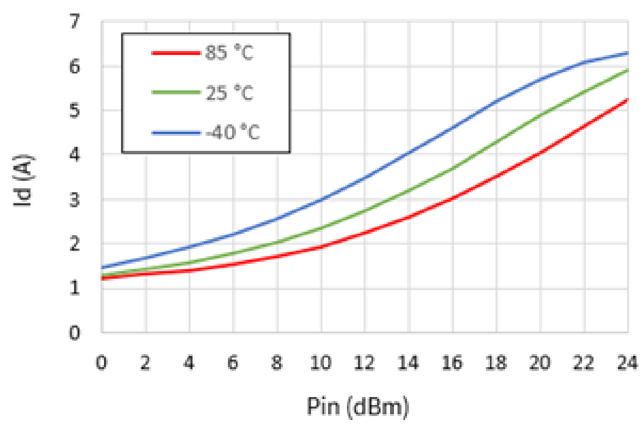
Output Power vs. Input Power



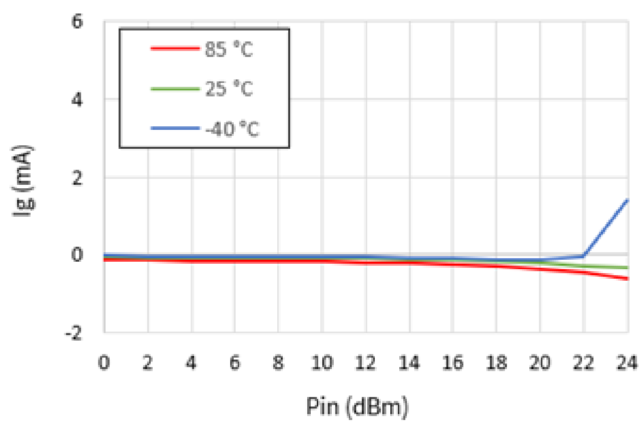
Power Added Efficiency vs. Input Power



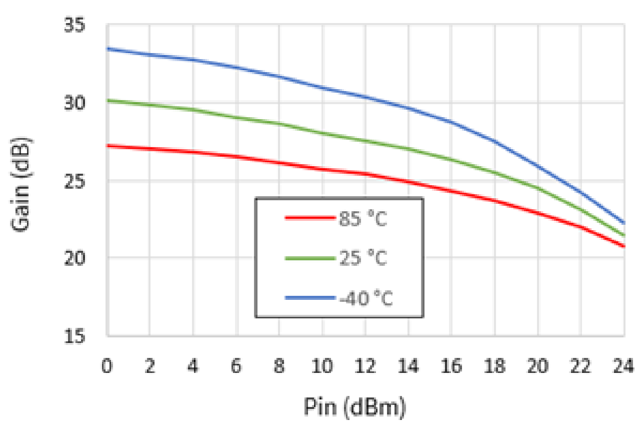
Drain Current vs. Input Power



Gate Current vs. Input Power



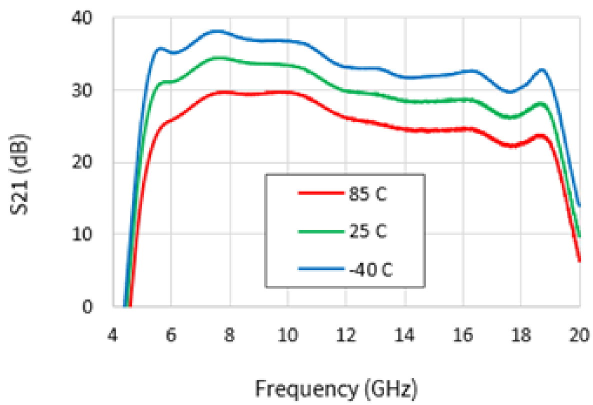
Gain vs. Input Power



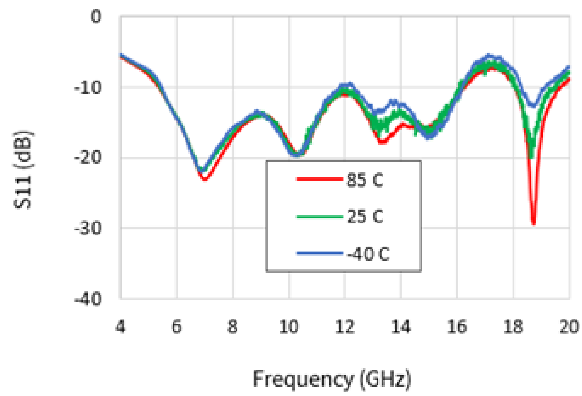
Typical Performance Curves – Small Signal over Temperature

V_D = 22 V, I_{DQ} = 1.2 A, CW, P_{IN} = -25 dBm

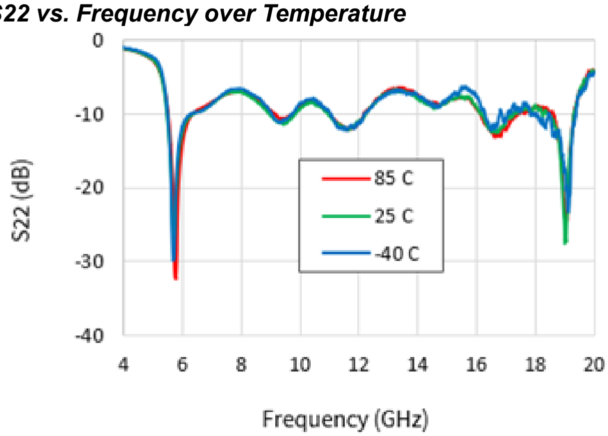
S21 vs. Frequency over Temperature



S11 vs. Frequency over Temperature



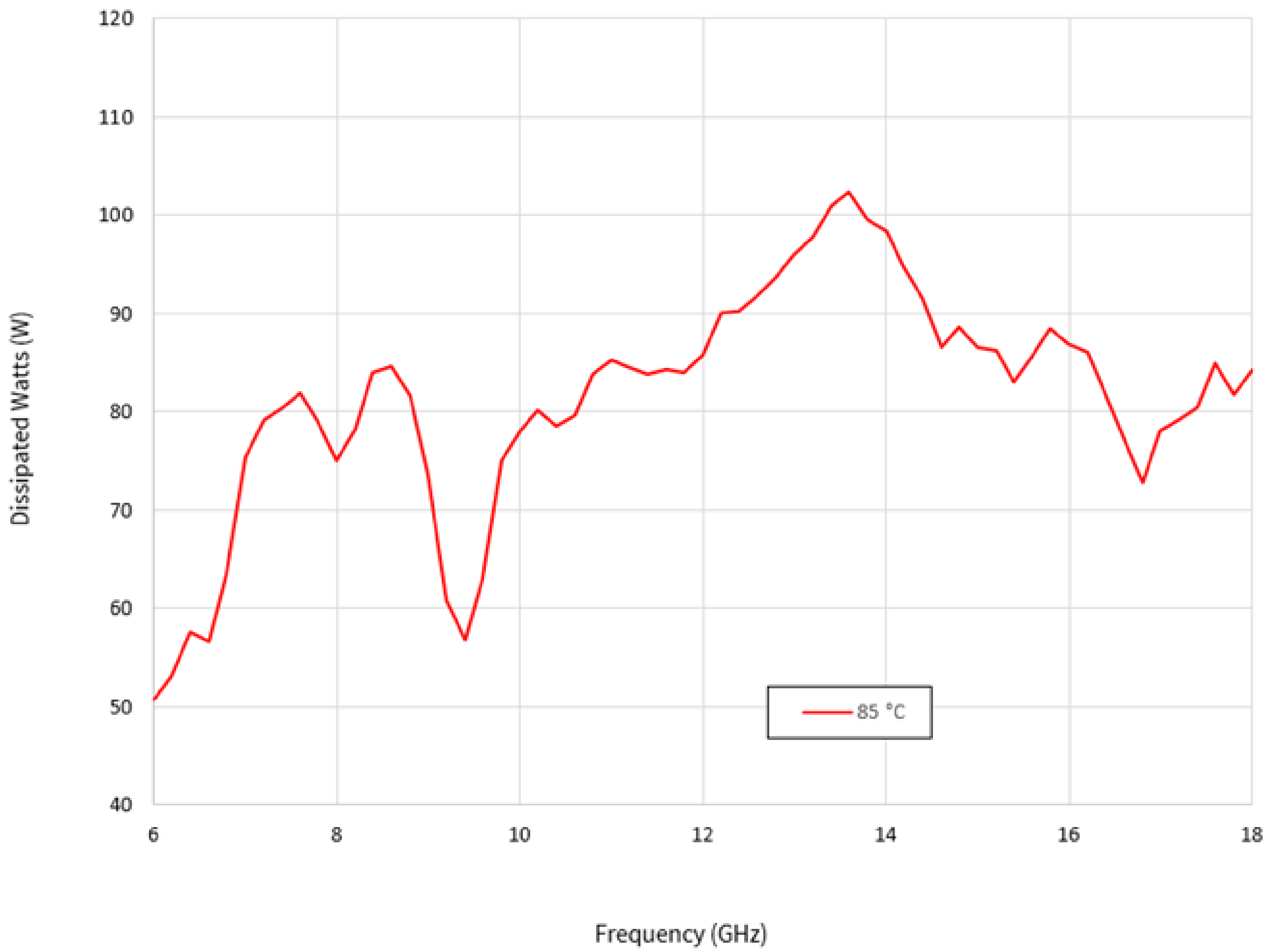
S22 vs. Frequency over Temperature



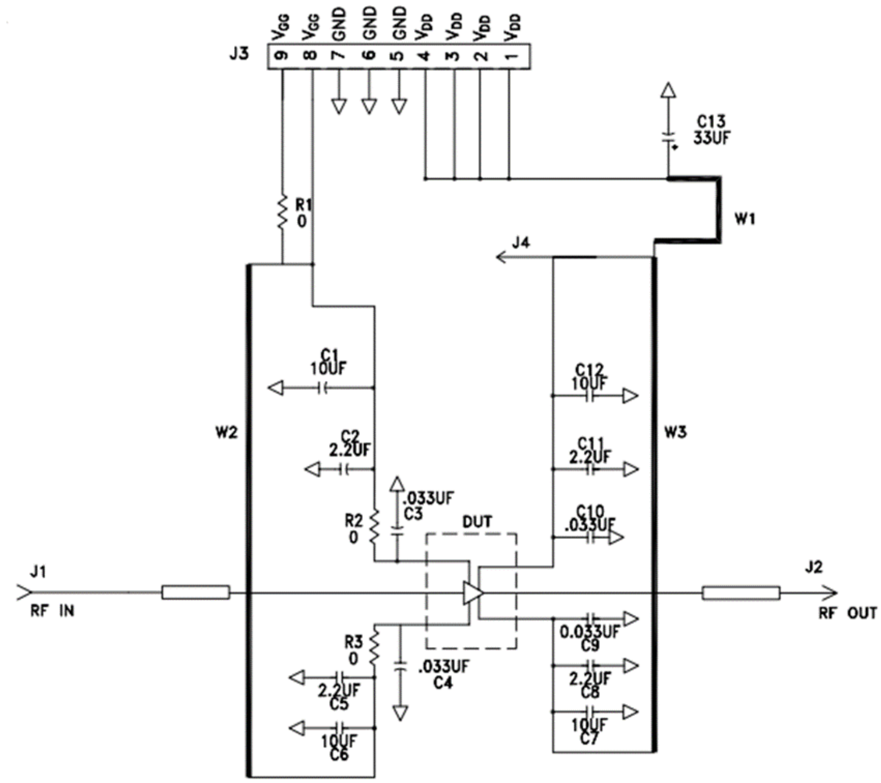
Thermal Characteristics

Parameter	Operating Conditions	Value
Operating Junction Temperature (T_J)	Freq = 13.6 GHz, V_D = 22 V, I_{DQ} = 1.2 A, I_{DRIVE} = 5.6 A , P_{IN} = 24 dBm, P_{OUT} = 43.2 dBm, P_{DISS} = 102 W, T_{CASE} = 60°C, CW	231ºC
Thermal Resistance, Junction to Case ($R_{\theta JC}$)		1.68ºC/W

Power Dissipation vs. Frequency (T_C = 85°C)



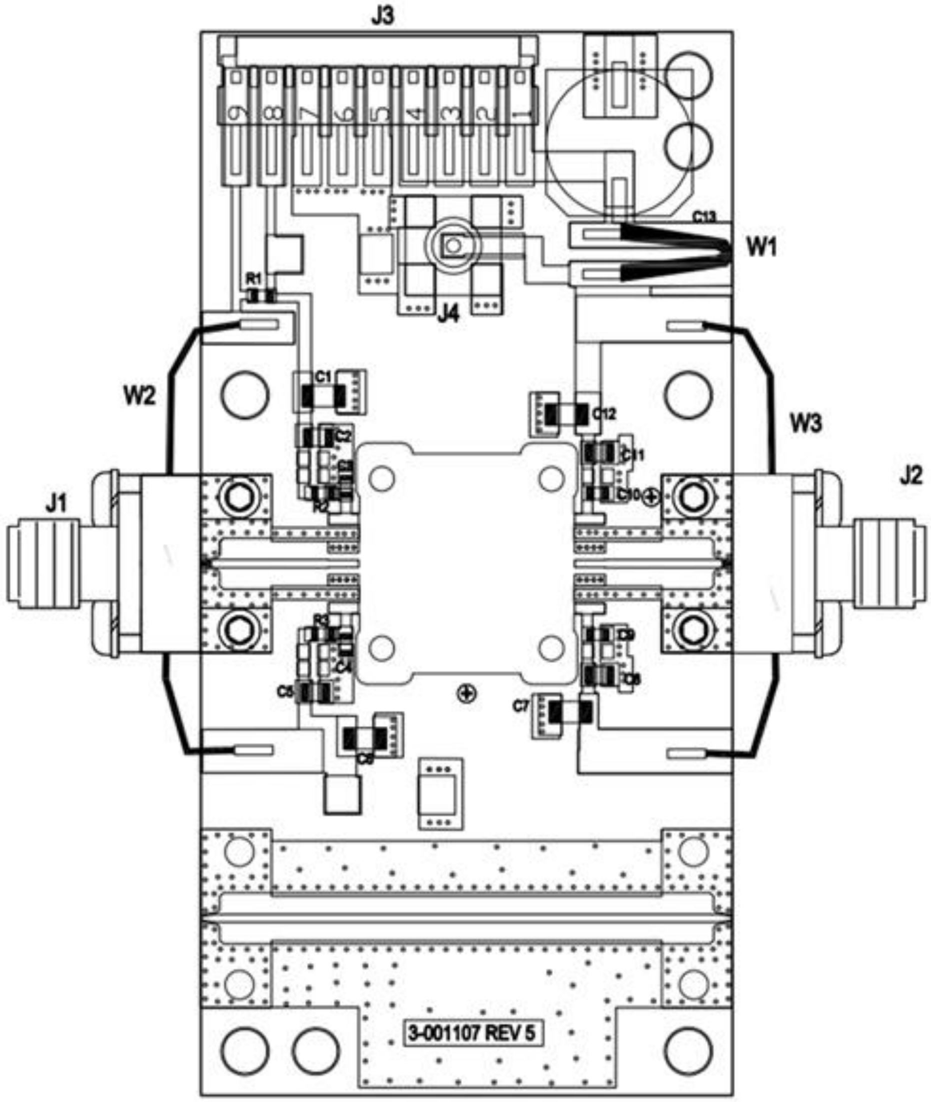
Evaluation Board Schematic (CMPA601J025F-AMP)



Parts List

Part	Value	Qty
R1,R2,R3	RES 0.0 OHM 1/10W 0603 SMD	3
C1,C6,C7,C12	CAP, 10uF, +/-10%, 50V, 1206	4
C2,C5,C8,C11	CAP, 2.2uF, +/-10%, 50V, 0805	4
C13	CAP, 33 uF, 20%, 100V, ELECTROLYTIC	1
C3,C4,C9,C10	CAP, .033uF, 50V,0603	4
-	PCB, RO3003, .010 THK, HPHF Package	1
-	BASEPLATE 3.0x1.5x0.25Cu	1
J1,J2	CONN, SMA JACK (FEMALE) END LAUNCH CONNECTOR	2
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
W1	WIRE, BLACK, 30 AWG	1
W2,W3	WIRE, BLACK, 22 AWG	2
U1	CMPA601J025F	1

Evaluation Board Assembly Drawing (CMPA601J025F-AMP)



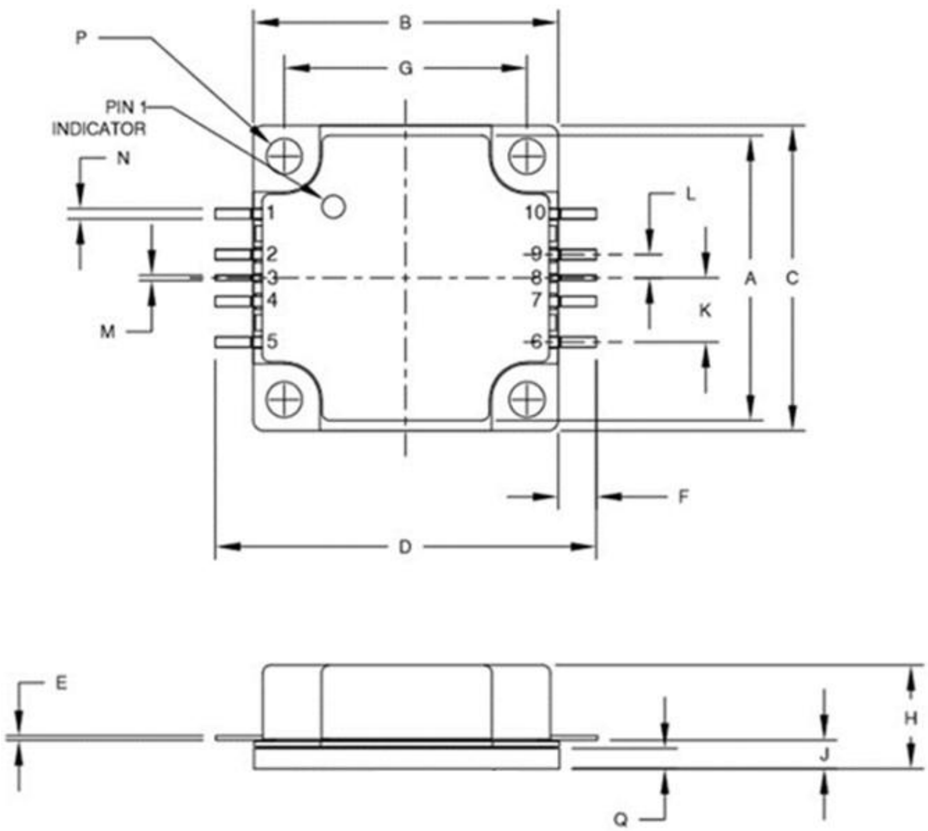
Bias On Sequence

1. Ensure RF is turned off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G = -5V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

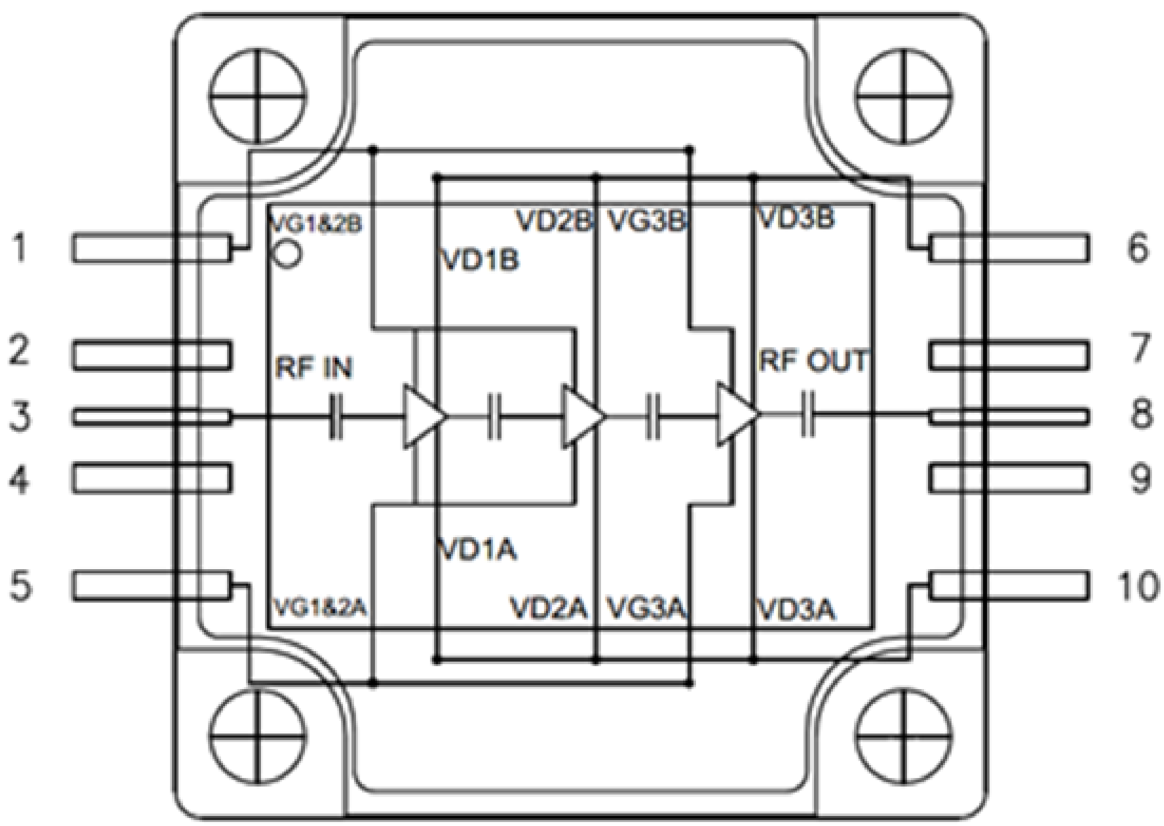
Mechanical Information



DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.555	.560	.565	14.10	14.22	14.35
B	.595	.600	.605	15.11	15.24	15.37
C	.595	.600	.605	15.11	15.24	15.37
D	-	(.750)	-	-	(19.05)	-
E	.006	.008	.010	0.15	0.20	0.25
F	.065	.075	.085	1.66	1.91	2.16
G	.473	.478	.483	12.01	12.14	12.27
H	.191	.203	.215	4.86	5.16	5.46
J	.049	.056	.063	1.24	1.42	1.60
K	.121	.126	.131	3.07	3.20	3.33
L	.041	.046	.051	1.04	1.17	1.30
M	.005	.010	.015	0.13	.25	0.38
N	.015	.020	.025	0.38	.51	0.63
P	.065	.070	.075	1.65	1.78	1.90
Q	.038	.040	.042	0.97	1.02	1.07

Pin Description

Pin #	Name	Description
1, 5	VG	Pins 1 and 5 must be electrically connected to the gate bias voltage.
6, 10	VD	Pins 6 and 10 must be electrically connected to the drain bias voltage.
2, 4, 7, 9	GND	RF and DC ground.
3	RFIN	RF Input. 50-ohm matched. Internally DC blocked.
8	RFOUT	RF Output. 50-ohm matched. Internally DC blocked.
Base	GND	RF and DC ground.



Revision History

Rev	Date	Change Description
V1P	11/27/2024	Preliminary release
V1	12/17/2025	Production release.