

OpenPA

The book of PA-RISC

**Paul
Weissmann**

Bonn

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OpenPA is a resource for HP PA-RISC and Itanium computers with technical descriptions of workstations, servers, their hardware architecture and supported operating systems. This project is independent of and does not represent The Hewlett Packard Company in any way. This book, now in its 13th release, is the offspring of the online project OpenPA.net.

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OpenPA.net was founded in December 1999 at a time when Google just started and Wikipedia did not exist yet. The idea was a central independent resource for information on PA-RISC Unix computers, widely available in the second-hand market of the late 1990s and early 2000s. OpenPA development and contributions peaked in those early years with a lively community around PA-RISC and open source systems.

The current OpenPA Book edition: <https://www.openpa.net/print.html>

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Chapter 1

Introduction

OpenPA is an information resource for PA-RISC computers, technology and operating systems; a registered serial publication with ISSN 1866-2757. First published in 1999, OpenPA has been edited and updated regularly for more than 25 years as an independent, non-commercial publication.

PA-RISC is a RISC computer architecture designed by Hewlett-Packard in the 1980s, used in HP 9000 and Visualize workstations and servers until the 2000s. Some older predecessors of PA-RISC from the 1980s and successors based on HP/Intel Itanium are also covered, as are available Unix operating systems.

OpenPA is based on public information from sources such as HP handbooks as well as articles, journals and conferences. OpenPA does not represent and is not affiliated with Hewlett Packard in any way. This site is provided as an informational resource only, for owners and users of PA-RISC computer systems and software.

Paul Weissmann is editor of OpenPA and also publishes OpenKRITIS on critical infrastructures and Insel Westberlin, a Berlin archive. He can be reached by mail. An OpenPA Book Edition of the complete project is available.

How come?

OpenPA.net was founded in December 1999 at a time when Google just started and Wikipedia did not exist yet. The idea was a central independent resource for information on PA-RISC Unix computers, which were widely available in the second-hand market of the late 1990s, early 2000s. OpenPA and contributions peaked in those early years with a lively community around PA-RISC and open source systems.

1999-2004

The open PA-RISC information resource was started in 1999 when second-hand PA-RISC systems became affordable for hobbyists after being phased out of the industry for modern COTS Windows NT and Linux servers. Not much PA-RISC information was readily available on the web then, when other Unix and RISC platforms such as Sun were documented well.

A 715/100 from a local newspaper ad started the interest and slowly led to an archive of PA-RISC documentation from the 1990s. Edited into a simple web site with frames, it was published with

hosting provided by Bill Bradford of SunHELP. The late Mickey appeared soon after, with lots of PA-RISC wisdom and first forays in the new PA-RISC open source scene – very incomplete then.

After two years in 2001, the site was renamed OpenPA.net and moved to a Digital DECstation 5000 on 1Mb dialup. Increasing support from HP for the PA-RISC Linux project made a lot of official PA-RISC documentation available. Open source operating systems made significant progress, including OpenBSD and Linux. Most HP 9000/700 and many “lettered” workstations were documented on OpenPA during that time, as were most PA-RISC processors, chipsets and operating systems.

2005-2008

Updates became less frequent after 2005 with minor additions such as the PA-8800 and PA-8900 processors, PA-RISC architecture and operating systems. An OpenPA print edition was finally released with several hundred pages PA-RISC content.

A burst of activity in 2008 resulted in much new content like 64-bit PA-RISC workstations and rp Series, some mainframes such as Convex SPP, V-Class and some early HP Itanium. Information on the fringes of PA-RISC was added, including third-party processors and OEM systems from Japan and early-1980s PA-RISC computers.

2009-2019

Update frequency and additions stalled considerably after 2008 with mostly low-intensity maintenance and reshuffling of content for more than a decade. The overall Internet and PA-RISC information changed a lot during that time.

Much HP documentation disappeared during the 2010s, so many links to original sources and references had to be removed. Interest in and support for PA-RISC in open-source systems dwindled as well.

Major housecleaning was done several times from 2016 on, checking links, content and rewriting much original language. Some new additions included a PA-RISC timeline and original equipment prices, a new OpenPA print edition and some restructured sections plus various cleanups in the backend.

2020-2024

OpenPA was refreshed again in the 2020s. Some longer new articles were written after the 20-year anniversary and an effort was made to find new sources to properly document PA-RISC history, based on the great and old pages.

Some new activities were started plus content was made more readable, sources consolidated and some rather unknown aspects of PA-RISC documented, like PRO, the 1980s, HP-UX and some odd operating systems, Apollo and PRISM.

Many OpenPA articles were updated, bad ideas from previous years (decades) reversed and some severely outdated text rewritten with new language. There is still some old content throughout OpenPA and many ideas still to be implemented. More information on the fringes was added – Intel-based Visualize computers and RISC laptops of the 1990s.

The yearbook

Year	Changes	Content	Backend
1999	Started	PA-RISC overview from the 90s	Frames, “dark-mode”
2000	7	HP 9000 700s, operating systems	Hosted at sunhelp
2001	7	32-bit processors, hardware, more systems	mickey@ appeared
2002	21	BSD, A/B/C/J lettered-systems, some 64-bit, X-Terms	Renamed, own server
2003	30	Complete 64-bit, four-digit systems, 3rd-party, more OS	
2004	14	Benchmarks, FOCUS, graphics, SCSI, architecture	Complete revamp, CSS
2005	3	Small updates	
2006	4	Final PA-RISCs - Mako, C8000	OpenPA book
2007	3	History, small updates	Limited paperback
2008	18	Mainframe/Cell, Itanium, 1980s PA-RISC, others	
2009	3	CPU and I/O architecture, much cleanup	10y anniversary
2010	2	T-Class, chipsets	
2011			
2012	1		OpenPA book update
2013			
2014	1	Cleanup and housekeeping	
2015	2	Handle disappearing sources and documents	
2016	6	Restructure chipset content, timeline, cleanup	
2017			
2018	3	PA-RISC story, OS updates, disappearing sources	Cloud move
2019			20y anniversary
2020	3	Agilent PA-RISC, many systems updates	
2021	2	Content mopup, OS history	Backend mopup
2022	3	Research OS reorganization, Apollo/PRISM, mopup	OpenPA book update
2023	5	PA-RISC history, 1980s, PRO in Japan, OpenPA and Internet	
2024	19	Oddball OSs, HP-UX, Visualize FX, PA-RISC architecture, Intel Visualize, RISC laptops, graphics	Frontend, graphics
2025	2		Backend, Book update

People

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Many people helped OpenPA with contributions and support over the years:

- ◇ Bill Bradford † for hosting this site in its early days
- ◇ Dave Fotland for the PA-7200 and HP 9000/840 information
- ◇ Dennis Grevenstein for information and documentation
- ◇ Frank McConnell for the HP 9000/500 and FOCUS information
- ◇ Götz Hoffart for the CSS/HTML help and inspiration
- ◇ Grant Grundler for support with HPPA and PA-RISC Linux over the years
- ◇ Helge Deller for additions to PA-RISC Linux

- ◇ Michael Piotrowski for corrections and HP-UX background information
- ◇ Michael Shalayeff † for providing PA-RISC and general wisdom
- ◇ Mike Hibler for information on HPBSD and Utah operating systems
- ◇ Miod Vallat for various PA-RISC explanations and corrections
- ◇ Ruby Lee for the PA-RISC Stirling information
- ◇ Thibaut Varene for PA-RISC Linux help and the development section
- ◇ Thomas Schanz for the CC photos of PA-RISC
- ◇ Ti Kan for the technical explanations on the Stratus architecture
- ◇ Dozens contributors and readers that sent in corrections, clarifications and questions

Thank you all!

OpenPA and Internet History

When OpenPA was founded in 1999, companies like HP just began opening up to open source projects, the Internet and the public in general. Information started to be published more freely on the new Web. Our main efforts at OpenPA during that time were finding, analyzing and correlating the large amount of distributed information into a single website.

PA-RISC computers were still used in the early 2000s and their resale to second hand users just started. Open source projects and hobbyists profited in a large, active community.

Our challenges at OpenPA during that time were finding all available information, as search engines were still young in the late 1990s, and making sense of it all – as it was just so much and new sources kept appearing. This phase went on until the mid-2000s with solid and stable sources.

The Internet and available information have changed since in a profound way. Almost all original sources disappeared in the two decades since then, and much has been lost on “the Information Highway” – making OpenPA the authoritative source for PA-RISC. What started as a documentation exercise of collecting new information in the 1990s Internet has become an historic archive of the PA-RISC era.

Over two decades of work researching PA-RISC and HP 9000 resulted in over 200 articles on OpenPA (now 216), on the PA-RISC landscape in an era long forgotten now.

The Internet never forgets

It seems the Internet *does* forget.

When much PA-RISC information and many sources became public in the late 1990s, there was no real reason to believe they would disappear any time soon again. It seemed most will have good place in repositories, search engines, archives and hobbyists sites (such as GeoCities et al).

However, that changed only a few years later.

OpenPA started right in the period around the dot-com bubble when much documentation and IT was easily available and the Internet and online content looked likely to be around forever.

During the economic and corporate upheavals of the 2000s much information, not only PA-RISC, fell by the wayside and the nature of the Internet and how companies used it changed. Journals closed and

got rid of their archives, websites just vanished, companies merged and removed or lost old documentation in the process. Few primary sources remained since.

Professional Computing in the 80s and 90s

HP produced a great deal of documentation and information for PA-RISC over the years. From PA-RISC inception in the 1980s until the late 1990s, much of that information was confined to commercial, industrial and research relationships and was not open to the general public. HP partners and clients had access to that library of documentation on PA-RISC hardware, architecture and software.

A complete ecosystem was available around HP products including HP 9000 and PA-RISC– user groups, conferences, trade journals and specific distribution channels. HP, the HP 9000 series and HP-UX were focused strongly on industrial, engineering and instrumentation customer bases, so documentation and PA-RISC information tended to stay confined to those circles, with less academic (public) exposure than other vendors and architectures.

It was hard to access HP and PA-RISC documentation in this period if not a HP partner or client. Even though called “Information Age” already, access was tightly confined in the 80s and 90s to those with PA-RISC vendor links or deeper technological interests. This is probably one of the reasons HP 9000 and HPPA computers were not documented as well as other architectures.

It was all very conservative until the the end of the 90s, the era OpenPA started.

The Open Era of the Internet

Around the time open source and Linux took off in the late 1990s, HP began to take notice of fledging open source projects for PA-RISC that potentially had a wider distribution. Many PA-RISC computers found their way in the late 1990s to larger customer bases including university research projects and development groups.

This created more demand for proper documentation on PA-RISC systems outside the usual sales and vendor channels. Lots of information on PA-RISC was released because of this in the late 1990s and early 2000s plus many business magazines and industry journals started publishing on the web, including access to their archives.

There was almost too much information available at that time. Search engines were still new-ish and often still directory-based. Many public and specialized repositories existed and were openly accessible as well. In this open era, a splurge of documentation was released by vendors from their commercial, sales and research archives and put freely on the web with no questions asked.

You could even get printed architecture books for free from some vendors for research, and some operating system releases were available freely due to “Y2K” .

It was a great time researching and documenting PA-RISC as more and more repositories and sources kept appearing. Finding and sorting all this information from expanding sources proved maybe the hardest, as there was so much to choose from.

Fleeting Information

PA-RISC documentation and information changed after these few years of open access. It slowly started in the mid-2000s with corporate upheavals and a profoundly changing technology landscape. Linux

and open source projects began arriving at scale in many formerly traditional Unix niches and the Intel/Windows NT ecosystem took swathes out of the RISC workstation market.

RISC and Unix lost significance for clients and thus commercially for vendors. IT had to become cheap and easy, a train which the conservative Unix servers and workstations did not really catch. Traditional IT vendors slowly lost interest in RISC computers with their business units too and providing documentation for increasingly unloved products became an afterthought.

The financial crisis at the end of the 2000s led to more corporate upheavals and economic hardship and more IT consolidation followed. Departments closed and took their websites and documentation with them. Whole business units disappeared with their products. Business press and trade journals were hit as well, and many publishing repositories with articles from the exciting 80s to 2000s information technology vanished without a trace or archive.

Many original PA-RISC sources and documents vanished during the 2010s, as the commercial RISC and Unix era got slowly forgotten and information on it too.

OpenPA thus had to make more use of secondary sources and industry articles that remained available – which in turn also started disappearing in the 2020s. Not much was left compared to the early 2000s – most original HP documentation on PA-RISC, contemporary articles, news releases, prices and even ads were gone.

This changed recently in the 2020s again. Many archives and mirrors were able to collect PA-RISC and HP 9000 documentation over the last few years, so proper linking to those resources became possible again.

1.0.1 RISC History

It got quite difficult to maintain articles based on ever fluctuating sources. This might just be the transitional nature of the Internet, but it was surprising to see so much go after doing this for over two decades. And it got worse in the meantime – so much has been lost as of the 2020s in both official company archives and secondary sources like the press.

This site has become an historic archive on PA-RISC and HP 9000 since many other sources are just not around anymore. Originally envisaged to be a platform to filter and consolidate all the information the “new” Internet started to offer on HP RISC, in the span of two decades OpenPA became the sole source of information for many aspects of PA-RISC and HP 9000.

When OpenPA started, HP 9000 machines were still (quite) current and PA-RISC a somewhat actively developed and marketed architecture. Both PA-RISC computers and documentation for them have become historic since, and much of the information and many anecdotes were (or are) at risk of disappearing, unless documented somewhere.

Who still knows that PA-RISC ran not only NeXTSTEP, but also Windows NT and Netware? The PA-RISC 1.0 processors and computers of the 80s had almost been forgotten by the time OpenPA started in 1999 – a whole chapter of PA-RISC had no real product names

OpenPA will try to document and archive as much of the history of PA-RISC in the colorful era of RISC and Unix workstations as possible.

Sources

Information on PA-RISC and HP 9000 on OpenPA is based on public sources and public repositories. Primary sources are HP and PA-RISC technical reference manuals, handbooks and architecture guides

from the 1990s that were published by HP in the early 2000s plus many product brochures added later.

This PA-RISC knowledge base was extended during the early OpenPA years with secondary sources such as magazine articles, news releases and publications like the HP Journal. It has been a long journey since and OpenPA transitioned from documenting then-current Unix PA-RISC workstations to an almost historical archive on the PA-RISC side of the 1990s Unix era.

PA-RISC CPU, chipset and architecture: Articles are mostly based on primary sources from HP like the great HP “External Reference Specifications” (ERS) and technical publications from HP CPU and chip design labs made available during the 2000s for HP-supported open source projects. Secondary sources in the form of articles or academic papers were used as well.

Computer systems: Information on HP 9000 and PA-RISC computers is based on primary sources from HP and vendors in the form of system user guides, technical handbooks and architecture white papers. Also used were many 1990s HP websites, marketing brochures, news articles and industry reporting.

Operating systems: Articles are based on official user and admin documentation as well as academic papers, talks, whitepapers and such. The heydays of open source, Mach, Linux and BSD research systems from the 1990s resulted in much information on public websites. As much of the operating system development on PA-RISC happened during 1990s and then early 2000s, information is getting sparse now.

Books and papers: A large body of literature exists in academic papers and conferences of the 1980s and 90s, when HP published much on Precision Architecture and RISC computers. COMPCON digests of papers contain many interesting articles– mostly deeply buried in libraries. Some museal sites also have been digitizing many old product brochures from HP and others, another valuable resource.

Archives: Websites and projects that archive and mirror Internet content have been around since the 1990s. Due to the disappearing sources, their archives of public websites have become essential today to document the RISC era. In the last few years until the 2020s, much product documentation, handbooks, guides and other information has been added to those archives as well, helping OpenPA to stay accurate and provide a complete picture of PA-RISC.

Closing remarks

For a taste of the 90s Internet, there is a fabulous archive of GeoCities on tumblr. Much HP 9000 information can be found at the HP Computer Museum as well as the Hewlett Packard section of archived brochures at 1000 BiT. The great HP-UX Workstation PA-RISC Hardware Compatibility List (mirror) from HP played a big role in the early years.

Many business and tech journals are now available at the Internet Archive, an essential resources for computing research now used as reference in most OpenPA articles.

Pictures Hewlett Packard.

Further reading

- ◇ HP UNIX Workstations and Netstations, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP Enterprise Computing Assistance Directory, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ HP Technical Documentation, Hewlett-Packard Company (1999: mirror accessed January 2024)

Wanted: Hardcopy COMPCON digests 1982-1999

OpenPA is looking for hardcopy digests of COMPCON, the Computer Conference of IEEE International from the 1980s and 1990s. Physical copies turn up only rarely and most are buried within libraries and could be retired or discarded soon.

Much PA-RISC history was presented at COMPCON conferences and many interesting articles hide in the digests of *Intellectual Leverage for the Information Society* conferences on the RISC era of the 1980s and 1990s. These articles would be welcome additions to OpenPA information on PA-RISC.

We are looking for conference proceedings of:

- ◇ COMPCON 1982 *High technology in the Information Industry*
- ◇ COMPCON 1983 *Intellectual Leverage for Information Technology*
- ◇ COMPCON 1984 *Intellectual Leverage for Driving Technologies*
- ◇ COMPCON 1985 *Technological Leverage*
- ◇ COMPCON 1986 Digest of Papers
- ◇ COMPCON 1987 *Intellectual Leverage*
- ◇ COMPCON 1989 *Intellectual Leverage*
- ◇ COMPCON 1991 *Intellectual Leverage*
- ◇ COMPCON 1992 *Intellectual Leverage*
- ◇ COMPCON 1993 *Intellectual Leverage*
- ◇ COMPCON 1994 *Intellectual Leverage*
- ◇ COMPCON 1995 *Technologies for the Information Highway*
- ◇ COMPCON 1997 *Technologies for the Information Highway*
- ◇ COMPCON 1998 Digest of Papers
- ◇ COMPCON 1999 Digest of Papers

OpenPA would be glad to take used or surplus hardcopies of COMPCON digests as they become available for our PA-RISC archive and the RISC era. 10x

PA-RISC at HOT CHIPS Conference in the 1990s

HOT CHIPS is an IEEE conference on microprocessors and microcomputers, organized yearly since 1989. Almost all cutting edge RISC and computer architectures of the 1990s were presented at HOT CHIPS over the years, and interesting PA-RISC information can be found at the conference in HP presentations between 1991 and 1999.

Some notable PA-RISC presentations at HOT CHIPS, all at

- ◇ PA-RISC Processor for Snakes Workstation, Hewlett Packard, HOT CHIPS 3 (1991)
- ◇ A 200 MFLOP HP PA-RISC Processor, Hewlett Packard, HOT CHIPS 4 (1992)
- ◇ Multiprocessor Features in a PA-RISC Processor Interface Chip, Hewlett Packard, HOT CHIPS 4 (1992)

- ◇ Hummingbird: A Low-Cost Superscalar PA-RISC Processor, Hewlett Packard, HOT CHIPS 5 (1993)
- ◇ System Design Verification of the HP735 VLSI, Hewlett Packard, HOT CHIPS 5 (1993)
- ◇ A Single-Chip Workstation Graphics System, Hewlett Packard, HOT CHIPS 5 (1993)
- ◇ *Multimedia Enhancements for PA-RISC Processors*, Hewlett Packard, HOT CHIPS 6 (1994)
- ◇ Memory Performance Features of the 64-bit PA-8000, Hewlett Packard, HOT CHIPS 7 (1995)
- ◇ A 150MHz Superscalar RISC Processor with Pseudo Vector Processing Feature, Hitachi, HOT CHIPS 7 (1995)
- ◇ The HP PA-8000 RISC CPU: A High Performance Out-of-Order Processor, Hewlett-Packard, HOT CHIPS 8 (1996)
- ◇ Effectiveness of the MAX-2 Multimedia Extensions for PA-RISC 2.0 Processors, Hewlett-Packard, HOT CHIPS 9 (1997)
- ◇ Techniques for Mitigating Memory Latency in the PA-8500 Processor, HOT CHIPS 10 (1998)

Chapter 2

PA-RISC Hardware

2.1 Overview

HP 9000 PA-RISC computers are based on HP Precision Architecture, a conservative HP RISC design from the 1980s and 1990s for Unix servers and workstations. HP's own PA-RISC processors from the early 32-bit TS-1, based on TTL, to the modern dual-core 64-bit PA-8900 in the mid-2000s.

HP designed and produced most processors in-house, as it did with the custom HP chipsets and platform designs used in HP 9000 PA-RISC servers and workstations. There were many special HP expansion cards for HP 9000 I/O buses, and again for graphics and videos HP often used inhouse PA-RISC graphics adapters.

PA-RISC computers use their own Boot Menu, the PDC boot ROM, and display error codes on LEDs and LCDs on the system front.

2.1.1 Phases

PA-RISC hardware platforms and computers were developed and marketed in phases by HP, based on technological advances, market development and the computerization since the 1980s. HP 9000 PA-RISC computers can be grouped into four periods:

Phase	Design	Processors	Chips	Used in
Phase I	Infancy: Early Architecture			
	Early	TS-1, NS-1, NS-2, PCX	SIU/SPI, CTB	<i>Early 800 servers</i>
Phase II	Growth: 32-bit 1990s			
	ASP/Viper	PA-7000, PA-7100	Viper, ASP	<i>700 workstations 800 servers 74x VME</i>
Phase III	Maturity: The heydays			
	LASI	PA-7100LC, PA-7300LC	MIOC, LASI, Wax, Dino	<i>700 workstations 74x VME</i>
	U2/UTurn	PA-7200, PA-8000, PA-8200	MMC/SMC, U2, UTurn, LASI, Wax, Dino, Cujo	<i>Visualize workstations Lettered servers</i>
	Astro	PA-8500, PA-8600, PA-8700	Astro, Elroy	<i>Visualize workstations Lettered servers</i>
	Stretch	PA-8500, PA-8600, PA-8700	DEW, Prelude, IKE, Elroy	<i>Integrity servers</i>
Phase IV	64-bit to Itanium			
	Cell	PA-8700, PA-8800PA-8900	CC, XBC, SBA, Elroy	<i>Integrity servers Superdome mainframes</i>
	ZXI	PA-8800PA-8900, Itanium 2	Pluto, Mercury	<i>Integrity servers Superdome mainframes Itanium computers</i>

2.1.2 History

PA-RISC ended with very advanced 64-bit designs in the Decline (IV) phase during EPIC Itanium. The overall HP PA-RISC and HP 9000 story is much longer, together with the equally complex history of PA-RISC operating systems.

There is also a timeline of PA-RISC releases and pricing from 1982 to the 2010s.

2.2 PA-RISC Architecture

2.2.1 Overview

PA-RISC is Hewlett Packard's Reduced Instruction Set Computing (RISC) architecture developed in the 1980s and used until the mid-2000s in Unix and industrial HP computers. The computers covered on this site, the HP 9000, are based on the Precision Architecture and PA-RISC processors and used custom HP system designs.

There were three versions of PA-RISC architecture

Table 2.2: PA-RISC Architecture Versions

Version	Bits	Instructions	Features	Processors	Years
PA-RISC 1.0	32-bit	140	Original	TS-1, NS-1, NS-2, PCX	1986-1990
PA-RISC 1.1	32-bit	190	MMU Low-cost, MAX	PA-7000, PA-7100, PA-7200, PA-7100LC, PA-7300LC	1991-1996
PA-RISC 2.0	64-bit			PA-8000, PA-8200, PA-8500, PA-8600, PA-8700, PA-8800, PA-8900	1996-2005
PA-WideWord	64-bit	VLIW/ILP	Super-parallel	PA-9000	Future

2.2.2 Precision Architecture RISC

PA-RISC is Hewlett Packard's Reduced Instruction Set Computing (RISC) architecture from the 1980s and an offspring from active HP research and development undertakings from that time. The aim of the Precision Architecture was to replace 16-bit stack-based CPUs in HP 3000 servers and Motorola 680x0 CPUs in HP's Unix systems with a common system architecture.

The PA-RISC architecture and instruction set were "built from the ground up" by HP engineers. PA-RISC was implemented almost exclusively in HP processors, from early version in TTL and NMOS in the 1980s to more modern integrated 32-bit (PA-7x00) and 64-bit (PA-8x00) RISC processors.

Overall PA-RISC was a rather conservative RISC design for the 1980s, updated until the early 2000s. HP described the Precision Architecture as the result of "years of studying" RISC:

- ◇ Reduced instruction set ("simple, efficient instructions")
- ◇ Instruction set is implemented in hardware ("hardwired") and not microcoded.
- ◇ Instruction size is fixed length and fixed format — one word (32-bit), which facilitates pipelining
- ◇ Only three addressing modes: long/short displacement and indexed.
- ◇ Load/store design: Only load and store operation access the memory, computational instructions do not.
- ◇ Single cycle operation: Many simple and frequently used instructions execute in just one cycle, more complex computation are assigned to assist processors or software algorithms.
- ◇ Optimizing compilers

The instruction set was tested widely by HP scientists on a wide range of programs with “billions of instructions” (in the 1980s!) to identify PA-RISC candidates— “only instructions that could add value were selected.”

HP added a few complementary features to “increase flexibility and performance:” Extended addressing, co- and multi-processor support and memory-mapped I/O. PA-RISC supported very wide addressing from the beginning and was designed as a SMP-capable architecture, with memory-mapped I/O simplifying the overall design.

Compared to other RISC architectures, original PA-RISC was rather simple and unspectacular—it had limited extra features but remained always at competitive speeds, especially in Floating Point and multiprocessing.

Later on, HP was the first to include multimedia extension in commercially available microprocessors, MAX-1 in the PA-7100LC and MAX-2 64-bit in the PA-8000, which allowed vector operations on two or four 16-bit subwords in 32-bit or 64-bit integer registers. HP was also slowish in bringing PA-RISC to 64-bit in the PA-8000 processors, another conservative design.

Spectrum

During development, PA-RISC was called Spectrum at HP Labs in Palo Alto, where it was “forged in laboratories based on experimental data” to achieve a simple architecture. A talk given by Joel Birnbaum laid this out in 1986.

Design objectives for Spectrum, and then PA-RISC, were: leadership in price/performance, migration path from current HP products, unified scalable architecture. Spectrum was planned to be scalable from single chips up to mainframe machines with constant compatibility for programs

In the early 1980s, when HP Labs was developing PA-RISC (Spectrum), RISC had not been commercially successful yet, caused by incompatibility with software written for previous CISC architecture. The advantages of RISC vs. CISC were hotly debated at the time, with HP doing fundamental research on performance factors. This resulted, in HP’s words, in many innovations in PA-RISC, such as a comparable path length to “conventional” machines but superior throughput.

Spectrum had 140 instructions, a fraction of then current CISC designs but more than contemporary RISC platforms— specified “really by the compiler people.” Most instructions were single-cycle with only some multi-cycle instructions required for languages such as COBOL and FORTRAN. Important for the Precision Architecture were fast control and data paths without microcode, resulting in fewer transistors needed, and high speed registers, with 32 general purpose identified as optimal.

HP designed a few “beyond RISC” features into PA-RISC: very large address space (48-bit direct addressing for 64-bit virtual), split instruction and data caches, high-bandwidth internal buses, memory mapped I/O for high-speed devices of the future, precision interrupts for real-time response and optimized I/O bus interfaces to enable easy bus converters.

As HP fabbed VLSI chips inhouse at the time (and kept doing that until the 1990s), it touted expansion possibilities of the CPU through support chips such as FPU and SMP possibilities.

PA-RISC 1.0

PA-RISC 1.0 was the first commercial implementation of HP *Spectrum* research on RISC and Precision Architecture. PA-RISC 1.0 is 32-bit with a single instruction and data bus and 140 instructions,

more than contemporary RISC designs. PA-RISC later moved to a Harvard architecture with separate instruction and data buses.

PA-RISC 1.0 has thirty-two 32-bit integer general purpose registers (GR0-GR31), seven shadow registers (SR0-SR6) for fast-interrupts and thirty-two 64-bit Floating Point registers, which could be combined to 64 32-bit and 16 128-bit. The FPU can execute Floating Point instructions simultaneously to the ALU.

Processors based on PA-RISC 1.0 were implemented in a multitude of fabrication technologies – TTL, NMOS, CMOS for the early PA-RISC CPUs during the 1980s.

Addressing in PA1.0 was 48-bit wide, later on expanded to 64-bit with the introduction of the PA-8000 line in PA-RISC 2.0.

PA-RISC 1.1

PA-RISC was extended to version 1.1 with PA-7000 CPUs in 1991 to now 190 instructions. The major change in PA-RISC 1.1 was the inclusion of a MMU (memory management unit) that enabled PA-RISC computers to use virtual memory.

Starting with the second PA-RISC 1.1 processor PA-7100, PA-RISC processors implemented superscalar instruction execution to execute multiple instructions simultaneously. 32-bit PA-RISC 1.1 processors are up to two-way superscalar, later 64-bit processors up to four-way.

Other significant developments in PA-RISC 1.1 include the PA-7100LC and PA-7300LC processors (LC for low cost), which integrated the memory and I/O controller onto the processor die, on the PA-7300LC additionally the cache controller and first-level cache.

PA-RISC 2.0

In 1996 PA-RISC was redesigned for 64-bit with PA-RISC 2.0 and the PA-8000 processor. Architectural changes were deep but PA-RISC remained compatible with 32-bit PA-RISC 1.1. PA-RISC 2.0 and the PA-8000 were actually introduced *before* the last 32-bit PA-RISC processor PA-7300LC shipped.

Main changes and features of PA-RISC 2.0:

- ◇ All registers and functional units extended to 64-bit
- ◇ Virtual address space extended to 64-bit
- ◇ Physical address space is 40-bit on PA-8000 to PA-8600 (for 1 TB of addressable physical memory) and 44-bit (16 TB memory) on PA-8700 and later
- ◇ Out-of-Order (OoO) execution with IRB (*Instruction Reorder Buffer*), which stores up to 28 computation and 28 load/store instructions and reorders execution on the fly. IRB tracks interdependencies and branch prediction outcomes and is the key part in the OoO execution capability of PA-RISC 2.0.
- ◇ FPMAC (*Floating Point Multiply Accumulate*) units

Later PA-8x00 processors of the 2000s did not introduce significant changes to PA-RISC architecture besides higher integration of large L1 caches in the PA-8600 and dual-core PA-8800 and PA-8900. Processors after the PA-8000 were mostly redesigns and extensions of that processor core.

Post-PA-RISC

HP originally started research into Instruction Level Parallel Processing (ILP) and Very Long Instruction Word (VLIW) architectures much earlier at HP Research Labs, the outcome of which it coined Explicitly Parallel Instruction Computing (EPIC) in the 1990s.

In the 1990s, HP was still planning on extending the PA-RISC architecture after 64-bit PA-RISC 2.0 into something called PA-WideWord (PA-WW) and Super Parallel Precision Architecture (SPPA), integrating research on ILP and VLIW architectures in a new set of processors beginning with PA-9000.

However, in mid-1990s on a parallel track to 64-bit PA-RISC and PA-WideWord, HP joined forces with Intel to commercialize ILP and VLIW in a brand new architecture. Both HP and Intel contributed R&D efforts and assets, resulting in what was called HP EPIC, Itanium and Intel IA64 architecture to revolutionize computing.

Eventual processors using this architecture were delayed several times and shipped only in early 2000, hindering building the Itanium platform and ecosystem and necessitating a parallel development of PA-RISC for multiple years.

Since the early-2000s HP sold two lines of Unix computers and servers in parallel—having both PA-RISC 2.0 and Itanium computers with HP-UX. These competition was apparent in the Integrity servers—with the rp servers (PA-RISC) and rx servers (Itanium) that were very similar in performance and price.

HP's post-PA-RISC designs were not the success many hoped for and HP soon after switched to standard Intel x86 fare in the late 2010s, keeping HP-UX and Itanium on life support for a few years. All the while having acquired Compaq with Digital Alpha and OpenVMS, another competing architectures.

Pre-PA-RISC

The predecessor of PA-RISC in the early 1980s was the HP FOCUS architecture from the HP 9000 Series 500. FOCUS was a stack architecture, with 230 instructions both 32 bits and 16 bits wide, a segmented memory model, and no general purpose programmer-visible registers. There are thirty-nine 32-bit registers in the CPU hardware, thirty-one internal 32-bit general purpose registers, two 32-bit ALU registers, and others.

2.2.3 PA-RISC CPU Features

Floating Point Unit (FPU)

The *Floating Point Unit* is an assist processor logically added to a system to improve the performance on floating-point operations. The processor can be on a separate chip (*e.g.*, PA-7000) or integrated onto the central CPU die (all PA-RISC CPUs upwards). The FPU executes special floating point instruction to perform arithmetic on its own set of independent registers (*register file*) and to move data between its own registers and the system's lower memory hierarchy. The FPU execution stage is pipelined. All PA-RISC FPUs contain thirty-two 64-bit registers, which can also be used as sixty-four 32-bit registers and sixteen 128-bit registers.

Memory and I/O Controller (MIOC)

The *Memory and I/O Controller* (MIOC) in the PA-7100LC and PA-7300LC processor integrates DRAM, cache and I/O controllers onto the processor die. MIOC is similar on both CPUs, with the PA-7300LC MIOC having wider data paths to L2 cache and RAM and supporting the advanced GSC+ bus over the older GSC on PA-7100LC.

MIOC's integrated memory controller requires only buffers and DRAM modules to build up complete memory subsystem. The PA-7300LC MIOC memory controller includes a Second Level Cache Controller SLC, which provides an optional L2 cache, ranging from 32 KB to 8 MB. It shares the data bus with the DRAM subsystem, so it has the same width and same optional SEDC error control.

- ◇ Execution units and internal caches attach on-chip to the MIOC
- ◇ External cache, L1 on PA-7100LC, L2 on PA-7300LC, attach to MIOC via 64-bit or 128-bit
- ◇ Memory attaches to MIOC via 64-bit on PA-7100LC or 128-bit on PA-7300LC
- ◇ GSC, the system main bus, attaches to MIOC
- ◇ Support for 4, 16, 64 and 256 Mbit modules, FPM and EDO DRAM at 3.3 or 5.0 V
- ◇ Up to 16 physical memory slots
- ◇ Support for a wide range of core frequencies

Transition Lookaside Buffer (TLB)

Translation Lookaside Buffer is a hardware structure for virtual-to-physical memory address translations which takes virtual page numbers and returns the corresponding physical page number. PA-7000 is the last PA-RISC processor with separate instruction and data TLBs, all later PA 1.1 and 2.0 CPUs use combined TLBs while older PA-RISC 1.0 processors use huge TLBs (even for today's standards):

Translation and miss handling in PA-RISC TLBs is as follows:

- ◇ *PA 1.1*: If a virtual address has to be translated to a physical address, the corresponding TLB is searched for an entry matching the Virtual Page number. If an entry is found, the 20-bit Physical Page number, delivered by the TLB, is concatenated with the original 12-bit page offset to the build up the 32-bit absolute physical address.
- ◇ *Hardware*: If the CPU implementation provides a hardware TLB miss handler, it attempts to find the virtual-to-physical translation in the *Page Table*. If successful, the translation and protection fields are inserted in the TLB. If not successful, an interruption occurs so the software miss handler can complete the translation.
- ◇ *Software*: If software TLB miss handling is implemented, a TLB miss fault interruption routine performs the translation. It inserts the translation and protection fields in the TLB and afterward restarts the interrupted routine, in which the TLB miss occurred.

Block Transition Lookaside Buffer (BTLB)

Similar to the TLB, the BTLB provides virtual-to-physical address translations. The *BTLB* however maps large address ranges rather than single pages as the TLB. These large address ranges are *block translations* and therefore stored in the *Block Translation Lookaside Buffer*. These block translations are useful for virtual address ranges that do not get paged in or out.

BTLBs were only implemented on 32-bit PA-RISC processors (PA-7x00), 64-bit PA-RISC instead implemented variable page sizes, thus any entry can be of >4k mapping.

Superscalar PA-RISC

Superscalar processors decode, dispatch and execute multiple instructions per cycle if dependencies between the instructions permit. This is possible if the instruction stream contains independent instructions. Superscalarity can be gained from a decoupled floating point unit (FPU) which executes floating point operations independently from the integer ALU. More complicated variations allow for parallel load/store operations, integer calculations and so on, which need a more complex CPU design that analyzes the instructions/branches.

Every PA-RISC processor from the PA-7100 on implements superscalar execution. Instructions proceed together through the execution pipeline, which is called *instruction bundling*. The superscalar execution is functionally transparent to the software, the effects of any given instruction are the same whether it was executed as part of a *bundle* or alone. Bundling rules are applied at run-time by the hardware; optimal performance may only be gained by proper ordering of the instructions so the processor can use its full superscalar potential. Several kinds of restrictions are placed upon the instruction bundling in PA-RISC:

- ◇ Functional unit contention
- ◇ Data dependency restrictions
- ◇ Control flow restrictions
- ◇ Special instruction restrictions

For bundling purposes instructions are divided into classes:

Table 2.3: PA-RISC superscalar instruction classes

Class	Description
FLOP	Floating point operation
LDST	Loads and stores
ALU	Integer ALU
MM	Shifts, extracts, deposits
NUL	Might nullify successor
BV	Branch Vectored (BV) local, Branch (BE) external
BR	Other branches
FSYS	FTEST and FP status/exception
SYS	System control instructions

PA-7100 superscalar capabilities

The PA-7100 is two-way superscalar with one integer ALU and one FPU.

Table 2.4: PA-7100 allowed instruction bundles

First instruction	Second instruction
ALU	+ FLOP

LDST	+ FLOP
FLOP	+ ALU/LDST/Branch

PA-7100LC/PA-7300LC superscalar capabilities

PA-7100LC/PA-7300LC are 2-way superscalar with two integer ALUs and one FPU. Only one of ALUs is capable to handle loads, stores and shifts.

Table 2.5: PA-7100LC/PA-7300LC allowed instruction bundles

First instruction	Second instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP
SYS	Never bundled

Besides from these bundles, *LDST + LDST* bundles are under certain circumstances also possible, called *double word load/store*. Several kinds of instructions cannot be bundled together because of data dependencies:

- ◇ An instruction that modifies a register will not be bundled with another instruction that takes this register as operand. Exception: a *FLOP* can be bundled with a FP store of the *FLOP*'s result register.
- ◇ A FP load to one word of a doubleword register will not be bundled with a *FLOP* that uses the other doubleword of this register.
- ◇ A *FLOP* will not be bundled with a FP load if both instructions have the same target register.
- ◇ An instruction that could set the carry/borrow bits will not be bundled with an instruction that uses carry/borrow bits.
- ◇ An instruction which is in the delay slot of a branch is never bundled with other instructions.
- ◇ An instruction which is at an odd word address and executed as a target of a taken branch is never bundled.
- ◇ An instruction which might nullify its successor is never bundled with this successor. Only if the successor is a *FLOP* instruction this bundle is allowed.

PA-7200 superscalar capabilities

PA-7200 is 2-way superscalar processor with two integer ALUs and one FPU. Similar to PA-7100LC, shift-merge and test condition units are not duplicated in the second ALU. To support the superscalar capabilities one additional write port and two additional read ports were added to the general registers (GR*).

Table 2.6: PA-7100LC/PA-7300LC allowed instruction bundles

First instruction	Second instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP

PA-8x00 superscalar capabilities

To be described.

2.2.4 Multimedia Acceleration MAX-1 and MAX-2

MAX-1 (32-bit)

MAX-1 are the original multimedia extensions from the 1990s introduced with the HP PA-7100LC processor and later also the PA-7300LC. The aim from HP in its design was to enable contemporary workstations with these CPUs to provide real-time MPEG video decompression and playback at a rate of 30 frames/second without the need for a special DSP (digital signal processing) chip, not an easy feat.

The HP design process for the PA-7100LC processor in the early 1990s included for the first time multimedia benchmarks for analyzing optimizations in the instruction set design.

The actual implementation used a small set of SIMD-MIMD instructions to facilitate the application of instructions on bundled subword data. Since these instructions use the same data paths and execution units within the processor as the regular instructions, the design team termed this *intrinsic signal processing* (ISP).

Sticking to conventional RISC principles, the design team decided against adding complex special-purpose instructions to the design but opted for the elegant use of the existing facilities in the CPU, which were slightly modified to understand new, packed subword data.

In 1994, the MAX-1 extensions made their way into the final PA-7100LC product and as such were the first SIMD instructions found in a general microprocessor. Less than 0.2 percent of the processor silicon area had to be used for MAX-1 additions and modifications, while allowing a very significant performance boost in affected applications.

As an example, the then-highend HP 9000 735/99 workstation with a 99 MHz processes and 512 KB cache achieved 18.7 FPS at MPEG decompression benchmarks—the new entry-level 712 workstation at 60 MHz and 64 KB cache achieved 26 FPS, an impressive feat for the time an 1990s information technology.

New MAX-1 multimedia instructions include: parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average.

MAX-2 (64-bit)

With the introduction of the new 64-bit PA-RISC 2.0 architecture in 1996 HP unveiled a new set of multimedia-oriented instructions aimed at using the processor's resources more effectively for sub-word

data. The basic components of the contemporary multimedia data were often represented as 8, 12 or 16-bit integers, for example audio sampling and pixel color depth.

Doing arithmetic with data of this length would waste an considerable amount of the processor's execution capacities, a simple addition of 16-bit data would only use one quarter of the 64-bit wide integer units datapath. To remedy this situation, MAX allows for packing of these *subword data* into larger words near the processor's natural word width (64-bit on PA-RISC 2.0 processors) and using parallel instructions on them. An example would be four 16-bit additions by the 64-bit adder on four 16-bit packed subwords.

The basic functionality from the earlier 32-bit MAX-1 was taken over and four more instructions added for MAX-2. Additionally, due to the wider integer registers (now 64-bit) more subwords can be packed in one cycle, doubling the effective speed of these multimedia instructions. The MAX-2 multimedia instructions include (new in MAX-2 are in **bold**): parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average, **parallel shift right**, **parallel shift left**, **mix** and **permute**.

MAX-2 debuted 1996 with the PA-8000 processor and later featured on all subsequent PA-RISC 2.0 processors (PA-8x00). In contrast to contemporary multimedia extensions, MAX-2 required only very little die space (0.1 percent on the PA-8000).

2.2.5 Further reading

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- ◇ PA-RISC 1.1 Architecture and Instruction Set Reference Manual (.pdf) Hewlett-Packard Company (February 1994, third edition. Accessed May 2009) **parisc linux**
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- ◇ Great Microprocessors of the Past and Present, John Bayko (June 2001/V 12.1.1: BURKS. Accessed 28 Dec 2007)
- ◇ A Closer Look at HP PA-RISC, MPE/iX 5.0 Documentation, Hewlett Packard (3kranger.com archive)
- ◇ Single Instruction Multiple Data, Multiple Instruction Multiple Data (MIMD), see for example the SIMD Wikipedia article and MIMD Wikipedia article
- ◇ Accelerating Multimedia with Enhanced Microprocessor (PDF, 2.4 MB) Discussion of the MAX-1 instructions. Ruby Lee, April 1995, IEEE Micro, Volume 15 Number 2.
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- ◇ The PA-7300LC: the first “System on a Chip” Tom Meyer (1996: Presentation for Microprocessor Forum 1995)
- ◇ Instruction-Level Parallel Processing, Joseph A. Fisher and Ramakrishna Rau, *Science* (HP 1991)
- ◇ Historical background for EPIC instruction set architectures, Mark Smotherman, Clemson University (2002, updated 2023)

2.3 PA-RISC Processors

2.3.1 Overview

HP PA-RISC processors are based on a RISC architecture developed by HP in the 1980s and used in HP computers from the 1980s to the 2000s. There are three versions of PA-RISC architecture and processors: 32-bit PA-RISC 1.0 in the 1980s, 32-bit PA-RISC 1.1 in the 90s and the final 64-bit PA-RISC 2.0 until the 2000s.

The following PA-RISC processors have been designed by HP in its VLSI Technology Center (VTC) and Systems & VLSI Technology Operation (SVTO) since 1986.

Table 2.7: HP PA-RISC processors overview

CPU	Architecture	Year	FETs	Clock up to	Cache max	Bus	Scalar	SMP	Units
FOCUS	FOCUS 32-bit stack	1982	450k NMOS	18 MHz	16 KB external	Custom	1-way	yes	INT FPU
TS-1	PA-RISC 1.0 32-bit RISC	1986	TTL	8 MHz	128 KB external	Custom	1-way		INT FPU
NS-1	PA-RISC 1.0 32-bit RISC	1987	144k NMOS	30 MHz	128 KB external	SMB	1-way		INT FPU
PRISM Apollo	PRISM 32-bit VLIW	1988	?	18 MHz	196 KB external	X-bus	3-wide	yes	INT FP
NS-2	PA-RISC 1.0 32-bit RISC	1989	183k NMOS	27.5 MHz	1 MB external	SMB	1-way	yes	INT FPU
PCX	PA-RISC 1.0 32-bit RISC	1990	196k	50 MHz	1 MB external	SMB	1-way	yes	INT FPU
PA-7000	PA-RISC 1.1a 32-bit RISC	1991	577k	66 MHz	512 KB external	PBus	1-way		INT FPU
PA-7100 PA-7150	PA-RISC 1.1b 32-bit RISC	1992	850k	125 MHz	3 MB external	PBus	2-way	yes	INT FP
PA-7100LC	PA-RISC 1.1c 32-bit RISC	1994	900k	100 MHz	1 KB 2 MB L2 external	GSC	2-way		2 INT FP MAX-1 MIOC
PA-7200	PA-RISC 1.1d 32-bit RISC	1995	1.3M	140 MHz	2 KB 3 MB L2 external	Runway	2-way	yes	2 INT FP
PA-7300LC	PA-RISC 1.1e 32-bit RISC	1996	9.2M	180 MHz	128 KB on-chip 8 MB L2 external	GSC	2-way		2 INT FP MAX-1 MIOC
PA-8000	PA-RISC 2.0 64-bit RISC	1996	3.8M	230 MHz	2 MB external	Runway	4-way	yes	4 INT 4 FP 2 L/S MAX-2
PA-8200	PA-RISC 2.0 64-bit RISC	1997	4.5M	300 MHz	4 MB external	Runway	4-way	yes	4 INT 4 FP 2 L/S MAX-2
PA-8500	PA-RISC 2.0 64-bit RISC	1998	140M	440 MHz	1.5 MB on-chip	Runway	4-way	yes	4 INT 4 FP 2 L/S MAX-2

PA-8600	PA-RISC 2.0 64-bit RISC	2000	140M	550 MHz	1.5 MB on-chip	Runway	4-way	yes	4 INT 4 FP 2 L/S MAX-2
PA-8700	PA-RISC 2.0 64-bit RISC	2001	186M	875 MHz	2.25 MB on-chip	Runway	4-way	yes	4 INT 4 FP 2 L/S MAX-2
PA-8800 dual-core	PA-RISC 2.0 64-bit RISC	2004	300M	1 GHz	2×1.5 MB on-chip 32 MB L2 external	Itanium 2	2×4-way	yes	2 cores 4 INT 4 FP 2 L/S MAX-2
PA-8900 dual-core	PA-RISC 2.0 64-bit RISC	2005	317M	1.1 GHz	2×1.5 MB on-chip 64 MB L2 external	Itanium 2	2×4-way	yes	2 cores 4 INT 4 FP 2 L/S MAX-2
PA-9000	PA- WideWord 64-bit VLIW	dropped		Explicitly Parallel Instruction Computing (EPIC)					

Several third-party PA-RISC CPUs were developed during the 1990s, some in the PA-RISC PRO consortium, used in Asian PA-RISC OEM computers or integrated appliances.

Table 2.8: Other PA-RISC processors overview

CPU	Architecture	Year	FETs	Clock	Cache	Bus	Scalar	Units	I/O
Amiga Hombre	PA-RISC 1.1 32-bit RISC	1995	?	125 MHz	?	64-bit	1-way	INT	multiple
Hitachi PA/50L	PA-RISC 1.1 32-bit RISC	1993	1.2M	33 MHz	12 KB	?	1-way	INT FP	
Hitachi PA/50M	PA-RISC 1.1 32-bit RISC	1993	1.2M	60 MHz	12 KB	?	1-way	INT FP	
Hitachi HARP-1	PA-RISC 1.1 32-bit RISC	1994	2.8M	120 MHz	24 KB 1 MB L2	?	2-way	2 INT FP	
Hitachi HARP-1E	PA-RISC 1.1 32-bit RISC	1995	4.5M	150 MHz	32 KB 8 MB L2	?	2-way	2 INT FP Vector	
Winbond W89K	PA-RISC 1.1 Lo 32-bit RISC	1994	1.1M	33/66 MHz	4 KB	i486	1-way	INT	
Winbond W90210 W90215	PA-RISC 1.1 Lo 32-bit RISC	1997	?	33/66 MHz	12 KB	i486	1-way	INT MAX- 1	multiple
Winbond W90220 W90221	PA-RISC 1.1 Lo 32-bit RISC	1999	?	150 MHz	8 KB	i486	1-way	INT DSP MAX- 1	multiple
Oki OP32	PA-RISC 1.1 32-bit RISC	1994	1.1M	33 MHz	?	?	1-way	INT	multiple

2.3.2 Early PA-RISC Processors

The first PA-RISC processors were designed by HP and used in mid to late-1980s in early HP 9000/800 servers and HP 3000 MPE/iX systems. These 32-bit RISC processors were mostly multi-chip implementations with separate chips forming the central processing unit, contrary to the mostly single-chip post-PA-7000 processors from the 1990s. Early PA-RISC CPUs were first based on TTL manufacturing, then NMOS-III and finally CMOS26B. An interesting aspect is their huge TLB size—from 2048 to 16384 entries while successors and competitors had sizes typically in the low to mid hundreds.

Early designs had clock speeds from 8 MHz up to 50 MHz in later versions, with 128 to 512 MB main memory. System designs were mostly based on the System Main Bus (SMB), as used in the early HP 9000 800 servers.

Naming is not always coherent as some sources refer to the processors as TS-1, NS-1, NS-2 and PCX while others call the same processors PN-5, PN-7, PN-10, CMOS26b. Generally, sources and documentation on these pre-Internet PA-RISC processors is rather sparse to non-existent, adding to the slight unclearities.

2.3.3 TS-1 PA-RISC Processor

Overview

The TS-1 was the first PA-RISC production processor, introduced in 1986. It integrated version 1.0 of PA-RISC on six 8.4×11.3" boards of TTL and was used in the first PA-RISC computers shipped by HP.

The TS-1 processor used in the HP 9000 840 is implemented in several boards for processing units, processor pipeline, a 4096-entry TLB and 128 KB L1 cache, divided into 64 KB for each data and instruction. The TTL boards measure 8.4×11.3" with SRAMs/PALs and about 150 ICs each. HP moved to NMOS with the next generation CPUs before settling with CMOS from the 90s on.

Details

- ◇ PA-RISC version 1.0 32-bit, three-stage pipeline
- ◇ The CPU consists of six separate boards:
 1. I-unit Instruction Unit
 2. Register File Board, contains general and control registers
 3. E-unit Execution Unit
 4. TLB translation lookaside buffer with 4096 entries for 2 KB pages
 5. Cache controller with split instruction and data caches of 64 KB each
 6. FPC floating-point coprocessor, handles FP operations parallel to the CPU/ALU (ADD/MUL/DIV chip was taken over from HP 9000/550 FOCUS)
- ◇ TLB off-chip, direct-mapped, 4096 entries
- ◇ Cache 128 KB offchip L1 direct-mapped/one-way associative
- ◇ Physical address space of 27-bit, 128 MB main memory could be addressed
- ◇ Clock speed 8 MHz

- ◇ Six or five printed circuit boards, implemented in FAST TTL and 25ns/35ns SRAMs/PALs, with each about 150 ICs
- ◇ Pictures of TS-1 CPU boards at Computermuseum University Stuttgart

Used in

- ◇ HP 9000 840 servers, the first PA-RISC computers.

2.3.4 NS-1 PA-RISC Processor

Overview

The first implementation of PA-RISC in a NMOS fabrication process, NS-1, followed in 1987 shortly after the original TTL-based TS-1. The NS-1 processor is integrated on a single circuit board (two on 825 servers) with the CPU as single NMOS-III chip supplemented by external support chips.

Details

- ◇ PA-RISC version 1.0 32-bit, three-stage pipeline
- ◇ Single CPU with eight support VLSI chips
 1. SIU system interface unit attaches the CPU to the SMB main bus
 2. CCU cache controller units CCU₀ and CCU₁ attach to external cache
 3. TCU TLB controller unit attaches to the external TLB
 4. MIU math interface unit with three third-party FP chips ADD, MUL and DIV
- ◇ TLB off-chip with 2048 to 4096 entries
- ◇ L1 cache 16 KB to 128 KB, unified and off-chip
- ◇ Physical address space of 29-bit, 512 MB main memory could be addressed
- ◇ CPU attaches via System Main Bus SMB to memory and I/O controllers, 64-bit bus
- ◇ Clock speed 25-30 MHz
- ◇ One circuit board, two boards on HP 9000/825
- ◇ 144,000 FETs, implemented in NMOS-III 1.7µm in a 272-pin ceramic PGA package
- ◇ Picture: NS-1 25 MHz, HP 825 computer, Wikipedia

Used in

- ◇ HP 9000 825, 835, 850 servers

2.3.5 NS-2 PA-RISC Processor

Overview

The final NMOS PA-RISC processor was the NS-2, a tweaked follow-on to the NS-1 introduced in 1989-90 with from three to five stages increased pipeline, new TLB and cache controllers and significantly larger caches and TLB.

The NS-2 is implemented on one circuit board with the CPU as a single NMOS-III and seven other VLSI chips. The bus structure connecting these chips was updated and simplified, with the CPU having private connections to the cache and TLB controllers, for which the NS-1 CPU had to use the shared cache bus.

Details

- ◇ PA-RISC version 1.0 32-bit, five-stage pipeline
- ◇ CPU is a single chip with seven VLSI support chips
 1. SIU system interface unit, attaches the CPU to the SMB main bus
 2. CCU cache controller units ICCU and DCCU, attach to external cache chips
 3. TCU TLB controller unit, attaches to external TLB chips
 4. FPC floating point controller and two third-party FP chips ADD, MULTI
- ◇ TLB off-chip, 16384 entries
- ◇ Cache up to 1024 KB L1, split into instruction and data, off-chip
- ◇ Physical address space of 29-bit, 512 MB main memory could be addressed
- ◇ CPU attaches via System Main Bus SMB to memory and I/O controllers, synchronous, pipelined 64-bit bus
- ◇ Clock speed 27.5 or 30 MHz, power dissipation of 26W
- ◇ One circuit board, CPU implemented in NMOS-III, 183,000 FETs, 1.5µNMOS-III, die size 14.0×14.0 mm² die, packaged in 408-pin PGA

Used in

- ◇ HP 9000/822 and 832
- ◇ HP 9000/845, 855, 860

2.3.6 PCX (CMOS26B) PA-RISC Processor

Overview

The last PA-RISC 1.0 design was the PCX, introduced 1990 and the first PA-RISC processor fabricated in a CMOS process. It implemented the PA-RISC NS-1/NS-2 design and several of the processor functions previously supplied on external VLSI chips onto a single CPU chip. PCX was possibly the HP *Stirling* processor.

PCX was supplemented by external support chips, including three cache multiplexers, SPI main bus to processor interface, floating point coprocessor and two FP chips for MUL/DIV and ADD/SUB. The successor to PCX was the PA-RISC 1.1 PCX-S processor (or PA-7000), which integrated most processor logic minus the FPU onto a single die/chip

- ◇ PA-RISC version 1.0 32-bit
- ◇ First multi-processor-capable PA-RISC CPU, up to four-way SMP
- ◇ Seven external supported chips
- ◇ External FPU (apparently ECL logic)
- ◇ TLB on-chip with 8192 entries
- ◇ Cache up to 1 MB L1, split into instruction and data, off-chip, asymmetrical 1:2, some systems used up to 4 MB (890)
- ◇ Physical address space of 29-bit, 512 MB main memory could be addressed
- ◇ CPU attaches via System Main Bus SMB to memory and I/O controllers, 64-bit bus
- ◇ Clock speed up to 50 MHz or 60 MHz (some sources mentioned 90 MHz)
- ◇ One circuit board, 196,000 FETs, 1.0μ(micron), implemented in three-level CMOS26B
- ◇ CPU is a single chip with seven VLSI support chips for memory/bus interfaces and I/O

Used in

- ◇ HP 9000/808, 815 servers
- ◇ HP 9000/842, 852, 865, 870 servers
- ◇ HP 9000 890 mainframe

Some sources mention a “CS-1” PA-RISC 1.0 processor — CS would point to CMOS design but performance figures and diagrams do not really match up with the CMOS26B/PCX here.

Other sources point to a (prototyped?) evolution of the last PA-RISC 1.0 CPU in CMOS— with up to 60 MHz (90 MHz), 4 MB L1 cache and PMB interface in a 408-pin PGA with 1.4×1.4cm die and 479k transistors— which in turn is eerily close to the PA-7000 processor.

2.3.7 Documentation

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Pictures Hewlett Packard, scans from product brochures, from hpmuseum.net and 100obit.it

2.3.8 PA-7000 PA-RISC Processor

PA-7000 (PCX-S) is a 32-bit processor with PA-RISC 1.1 architecture, introduced by HP in 1991. It integrated a MMU for virtual memory management, a first for PA-RISC. PA-7000 were designed for and first used in HP 9000 700 workstations, and only later in some HP 9000 800 servers. The HP processor was a multi-chip implementation fabricated in HP's own CMOS26B process with an external FPU (TI EPIC-2).

After PA-RISC 1.0 processors from the 1980s were mostly geared towards transaction processing and multi-user environments, the PA-7000 was designed to extend PA-RISC "down to low cost desktop workstation systems." The PA-7000 design process used existing technologies but implemented the first extension to PA-RISC architecture and collaborated with Texas Instruments for the FPU, a first for HP.

PA-7000 leveraged previous PCX PA-RISC design for the computing core, extending it to PA-RISC 1.1.

Graphics requirements were integrated into the design process of the PA-7000 processor, memory and system buses, as PA-RISC computers were used frequently for 2D/3D design in the 90s. Performance features for graphics support included: Block TLB entry for frame buffer, several FP and graphics instructions, data cache prefetch, and register and load/store features.

Functional units

The PA-7000 is a 32-bit PA-RISC processor, implementing version 1.1a of the PA-RISC architecture. It is single-processor only and one-way scalar.

There are two functional units in two VLSI chips in the PA-7000: one Integer ALU and one external Floating Point unit (FPU or FPC), co-developed with Texas Instruments. The PA-7000 CPU has a five-stage pipeline.

PA-7000 have a Translation Lookaside Buffer (TLB) with 192 entries (instruction and data), fully associative for virtual-to-physical memory address translations and a Block Translation Lookaside Buffer (BTLB) with 8 entries for virtual-to-physical page translations.

Cache and memory

PA-7000 use off-chip L1 caches, quite large for the time: up to 256 KB instruction and 256 KB data caches in TTL SRAMs, and no L2 caches. Cache data rate is 264 MB/s for instruction (32-bit) and 528 MB/s for data caches (64-bit) at 66 MHz clock.

Memory and I/O controller (MIOC) for accessing the memory and main buses is external on PA-7000. Address space 32-bit physical, 48-bit virtual.

Speed and buses

PA-7000 processors were fabbed with up to 66 MHz clock speed, on 5.0 V core voltage. They attach to the PBus processor bus, with 32-bit from processor to Memory and I/O Controller (MIOC) for up to 265 MB/s.

Physical

Fabricated by HP, PA-7000 have a 14.2×14.2 mm² die with 577,000 transistors (FETs) in a 1.0 μ m, 2-layer CMOS_{26B} process and packaged in 408-pin CPGA. The external FPU was fabbed as a 13.0×13.0 mm² die with 640,000 transistors (FETs) in 0.8 μ m, Texas Instruments EPIC-2 process, packaged in 207-pin CPGA.

The CPU draws 8W power at 66 MHz.

Performance

HP PA-7000 PA-RISC processors (1991) were average RISC performers of the early 1990s with roughly the same performance as MIPS R3000A (1992), Motorola 88100 (1988) and SPARC (1991 implementations) but slightly slower than IBM POWER1 (1990), Sun SuperSPARC (1992) and MIPS R4000 (1991) at similar clocks.

Compared to personal computers of that era, PA-7000 were faster than Intel 486DX2 (1992) and level with later Pentium P5 (1993) at the same frequencies, but significantly stronger in floating point than both.

Used in

- ◇ HP 9000 705, 710, 720, 730, 750 workstations
- ◇ HP 9000 F10, F20, F30, G30, G40, H20, H30, H40, I30, I40 servers
- ◇ Mitsubishi ME/R7200, ME/S7200, ME/R7300, ME/S7300, ME/R7500, ME/S7500

Documentation

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2. *Évolution des gammes de processeurs MIPS, DEC Alpha, PowerPC, SPARC, x86 et PA-RISC* André Seznec and Thierry Lafage (INRIA: June 1997)
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 - ◇ *Midrange PA-RISC Workstations with Price/Performance Leadership*, page 6 (Andrew J. DeBaets and Kathleen M. Wheeler)
 - ◇ *VLSI Circuits for Low-End and Midrange PA-RISC Computers*, page 12 (Craig A. Gleason et al.)
4. PA-RISC Processor for Snakes Workstation, Charles Kohlhardt, (1991: Hewlett Packard. Proceedings of IEEE Hot Chips III)

2.3.9 PA-7100 PA-RISC Processor

PA-7100 is a 32-bit PA-RISC processors, released by HP in 1992. It was the first PA-RISC processor to integrate the integer ALU and floating-point FPU on a single die. The design of the integer units is close to the PA-7000 but modified to scale to higher clock speeds.

The previously external FPU was a new HP design and moved by the design team on chip, taking up about one third of the transistor count. The link between the PA-7100 and its instruction cache was doubled in width compared to the PA-7000.

PA-7100 is the first superscalar PA-RISC processor and can issue two separate instructions at a time.

PA-7150 is a PA-7100 with tweaks to the core and cache subsystem to allow clock frequencies up to 125 MHz. Both were a mainstay in PA-RISC growth in the Unix market of the early-1990s with HP 9000 computers.

Functional units

The PA-7100 is a 32-bit PA-RISC processor, implementing version 1.1b of the PA-RISC architecture. It is multi-processor capable (SMP) and two-way superscalar, so it can decode, dispatch and execute two instructions per cycle (one CPU, one FPU).

There are two integrated functional units in the PA-7100: one Integer ALU and one Floating Point unit (FPU). The PA-7100 CPU has a five-stage pipeline.

PA-7100 have a three instruction queue and Translation Lookaside Buffer (TLB) with 120 entries, fully associative for virtual-to-physical memory address translations, smaller than on the PA-7000 processor. They also have a Block Translation Lookaside Buffer (BTLB) with 16 entries for virtual-to-physical page translations.

Cache and memory

PA-7100 have only off-chip L1 caches of up to 1 MB instruction and 2 MB data caches, which was unusually large for the time. Cache is implemented in asynchronous standard SRAMs (9ns at 100 MHz), and there is no L2 cache. Cache controller is on-chip, cache access is 64-bit wide.

Memory and I/O controller (HP Viper) to access the memory and main buses is external and off-chip on PA-7100. Address space 32-bit physical, 48-bit virtual (segmented).

Speed and buses

PA-7100 processors were fabbed with up to 100 MHz, PA-7150 up to 125 MHz clock speed, on 5.0 V core voltage. They attach to the PBus processor bus with 32-bit from processor to Memory and I/O Controller (MIOC).

Multi-processor systems could be designed with two strategies: either two PA-7100s attach to a shared PBus and one Viper Memory and I/O Controller ("low cost 2-way MP"), or each PA-7100 is attached to its own MIOC, which in turn is attached to a shared memory and I/O bus with the other PA-7100/MIOCs.

Physical

Fabricated by HP, PA-7100 have a 14.0×14.0 mm die with 850,000 transistors (FETs), fabbed in a 0.8μ, 3-layer HP CMOS26B (metal aluminium) process and packaged in 504-pin ceramic PGA. They draw 30W power at 100 MHz (or 20W in earlier sources).

Performance

HP PA-7100 PA-RISC processors were rather fast microprocessors for their time in 1992, on par with their RISC competition and beating even newer processors in floating point. At the same clock, PA-7100 were almost level with Pentium P54C (1994) and MIPS R4400SC (1992) but significantly faster in floating point, SPEC95.

They were significantly (almost twice) faster than DEC Alpha 21064 (1992) at 100 MHz, slightly faster than IBM PowerPC 604 (1994) but slower than higher-clocked Intel Pentium Pro (1995).

Used in

PA-7100 processors were used in the majority of early/mid-1990s HP 9000 workstations and servers, mostly for technical computing.

- ◇ HP 9000 715, 725, 735, 755, 742i, 745i, 747i workstations
- ◇ HP 9000 G50, G60, G70, H50, H60, H70, I50, I60, I70 servers
- ◇ HP 9000 T500, T520 mainframes
- ◇ Convex SPP1000/CD, SPP1000/XA mainframes
- ◇ Hitachi 3050RX 220, 230, 310S, 320, 330, 430, 440, 9000V V735/I25, VT500 workstations
- ◇ Stratus Continuum 610S, 610, 615S, 615, 620, 625, 1220, 1225, 1245 mainframes

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4. PA-7150 PA-RISC Processor (Hewlett Packard: April 1997)

2.3.10 PA-7100LC PA-RISC Processor

PA-7100LC is a 32-bit PA-RISC processor introduced by HP in 1994, designed as a single-chip solution for low-cost systems ("LC") with the performance of comparable workstations and servers. The CPU core of the PA-7100LC is close to the earlier 32-bit PA-7100 RISC processor, but integrated FPU, memory controller and first-level cache onto a single chip with main system bus attachment.

HP added support for bi-endian byte ordering for the first time to PA-RISC with the PA-7100LC, ostensibly for supporting a wider range of "non-Unix" operating systems, like Windows NT and others.

PA-7100LC processors used HP MAX-1 multimedia extensions for 1990s "multimedia" applications like MPEG audio and video decoding, as one of the first architectures and processor to do so.

PA-7100LC processor were successfully used by HP as integrated 32-bit RISC CPUs in a large range of lower-cost HP Unix workstations in the mid-1990s. The successor of the PA-7100LC is the similar PA-7300LC processor, much improved and released two years later.

Functional units

PA-7100LC implements 32-bit PA-RISC version 1.1c, it is single-processor only and two-way super-scalar, thus can decode, dispatch and execute multiple instructions per cycle. Only the first ALU can handle loads, stores and shifts which can only be paired with simple math operations, like integer addition or multiplication.

There are three integrated functional units in the PA-7100LC: two Integer ALUs and one Floating Point unit (FPU) plus MAX-1 multimedia extensions for multimedia applications. The PA-7100LC CPU has a five-stage pipeline.

PA-7100LC have a three instruction queue and Hardware *static* branch prediction.

The Translation Lookaside Buffer (TLB) has 64 entries, is fully associative, translates virtual-to-physical memory addresses, the Block Translation Lookaside Buffer (BTLB) with 8 entries translates pages (BATC, Block Address Translation Cache).

Cache and memory

PA-7100LC have an on-chip L1 cache of 1 KB on-chip for instructions, prefetched from the off-chip cache. Main cache is off-chip, a combined L1 cache up to 2 MB direct mapped, asynchronous SRAMs. The memory and I/O controller (MIOC) is integrated in PA-7100LC onto the die, for direct DRAM memory and cache interface.

The PA-7100LC supports both little-endian and big-endian ordering for more operating system options, a PA-RISC first. It supports 48-bit virtual addresses and up to 4 GB of physical memory, with non-cached memory pages as another first.

Speed and buses

PA-7100LC processors were fabbed with up to 100 MHz clock speed, on 3V core voltage. They directly attach to the GSC main system bus with 32-bit from processor to graphics I/O devices. Memory and caches buses are 64-bit, controlled by the on-chip MIOC, with up 480 to 600 MB/s datarate, depending on clock.

Physical

Fabricated by HP, PA-7100 had a 14.2×14.2 mm die with 900,000 transistors (FETs), fabbed in a 0.75µm, 3-layer HP aluminium process packaged in a 432-pin PGA.

Performance

HP PA-7100LC PA-RISC were pretty fast low-cost microprocessors in 1994, on par with RISC and PC competition of their time. At the same clock, PA-7100LC were in the ballpark of IBM PowerPC 604 (1994) and beat Pentium P54C (1994) and MIPS R4400SC (1992) in SPEC92 scores. They were much stronger in floating point.

As MPR put it, PA-7100LC were significantly faster “than the PowerPC 601 and dramatically faster than the TI microSPARC,” and had “far better FP performance” than Sun’s microSPARC II and outran “the fastest SuperSPARC chip” in SPEC92 scores.

Used in

PA-7100LC processors were used in the mainstay of more affordable HP 9000 Unix workstations of the mid-1990s and a few serves and industrial control systems.

- ◇ HP 9000 712, 715, 725 workstations
- ◇ HP 9000 743i, 748i VME and V743 VXI workstation
- ◇ HP 9000 D200, D210, D300, D310 servers
- ◇ HP 9000 E25, E35, E45, E55 servers
- ◇ Hitachi 3050RX 225, 235, 255, 535, e9000V V715, V715Tiny, VE25, VE35, VE45, VE55 workstations
- ◇ SAIC Galaxy 1100 portable workstations

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2.3.11 PA-7200 PA-RISC Processor

PA-7200 is a 32-bit PA-RISC processor, released by HP in early 1995. It completely revised the PA-7100 processor core, leveraging only the FPU. As two-way superscalar processor, PA-7200 can dispatch and execute two separate instructions at a time to its functional units. In contrast to PA-7100, the newer PA-7200 has two integer ALUs and can execute two integer operations simultaneously.

Other changes in the PA-7200 include a redesigned cache which retained the general PA-RISC cache layout with large off-chip L1 caches at processor clock, but changed some of the architecture. PA-7200 use the 64-bit Runway processor bus, carried on to later 64-bit PA-8000 processors.

HP targeted PA-7200 processors towards high-performance general-purpose applications, but designed them also for specialized applications with large working sets which could take advantage of the high-bandwidth bus interface. It was a pretty fast mid-1990s RISC microprocessor.

PA-7200 were expensive to fabricate and were used in only few 32-bit HP 9000 workstations in the mid-1990s before the 64-bit PA-8000 was introduced a year later.

Functional units

The PA-7200 is a 32-bit PA-RISC processor and implements version 1.1d of PA-RISC architecture. It is multi-processor capable (SMP) and two-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are three integrated functional units in the PA-7200: two Integer ALUs and one Floating Point unit (FPU). The PA-7200 CPU has a five-stage pipeline and a three instruction queue and Hardware *static* branch prediction.

The Translation Lookaside Buffer (TLB) with 120 entries, fully associative, translates virtual-to-physical memory addresses, the Block Translation Lookaside Buffer (BTLB) with 16 entries translates pages (BATC, Block Address Translation Cache).

Cache and memory

PA-7200 have, in the PA-RISC tradition, large off-chip caches at processor speed. There is a 2 KB on-chip “assist” on-chip cache, fully associative, holds 64 32-Byte cache lines. Main L1 cache is up to 1 MB instruction and 2 MB data, off-chip in asynchronous SRAMs with one cycle latency. There is no L2 cache.

Memory and I/O controller (MIOC) for accessing the memory and main buses is external and off-chip on PA-7200.

The PA-7200 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-7200 processors were fabbed with up to 140 MHz clock speed at 4.4 V core and 3.3 V I/O voltage. They attach to the Runway system interface, 64-bit, 120 MHz, 960 MB/s peak bandwidth.

For multiprocessing, PA-7200 have a glueless interface for up to four CPUs in SMP on same Runway processor bus.

Physical

Fabricated by HP, PA-7200 were a 14.0×15.0 mm die with 1,300,000 transistors (FETs), fabbed in a 0.55μ, 3-layer HP CMOS14A process and packaged in 540-pin ceramic PGA. They draw 29W power at 140 MHz.

Performance

HP PA-7200 PA-RISC were very strong microprocessors for 1995, usually above their RISC competition in technical computing. At the same clock, PA-7200 were much faster than IBM PowerPC 604 (1994), Pentium P54C (1994) and MIPS R5000 (1996), with almost twice the performance in floating point.

PA-7200 were almost equal to higher-clocker Pentium Pro (1995) and UltraSPARC (1995) and not far from Digital Alpha 21164 (1996) at significantly higher clocks.

Used in

PA-7200 processors were used in a few mid-1990s HP 9000 technical workstations, before HP switched to 64-bit and Visualize branding, plus a few servers.

- ◇ HP 9000 C100, C110 workstations
- ◇ HP 9000 D250, D260, D350, D360 servers
- ◇ HP 9000 J200, J210 workstations
- ◇ HP 9000 K100, K200, K210, K220, K400, K410, K420 servers
- ◇ Convex SPP1200/CD, SPP1200/XA, SPP1600/CD, SPP1600/XA mainframes
- ◇ Hitachi 9000V VQ200, VQ210, VR100, VR200, VR400 servers

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2.3.12 PA-7300LC PA-RISC Processor

The PA-7300LC is an integrated, 32-bit PA-RISC processor, released in 1996 and used in many mid- to late-1990s integrated HP Visualize workstations. PA-7300LC was a close successor “low-cost” to the earlier, highly-integrated PA-7100LC CPU, with several enhancements:

1. Large on-chip L1 caches, in contrast to the small L1 on-chip “assist” caches of the PA-7100LC and PA-7200
2. Integrated L2 cache controller in the on-chip Memory and I/O Controller (MIOC)
3. Improved bus interface with faster GSC+ bus variant for up to 160MB/s
4. Faster memory interface

The contemporary process technologies made it finally possible for HP to include a large L1 cache on the CPU die, breaking a long-standing HP tradition of large and off-chip L1 caches.

PA-7300LC was the final 32-bit, PA-RISC version 1.1 processor after the high-performance PA-7200. The first HP 64-bit PA-RISC 2.0 processor, the PA-8000, was introduced in the same timeframe.

HP used the PA-7300LC processor to close the gap on lower price-point workstations at the bottom of its product lineup like A180 servers and B-Class workstations.

Functional units

PA-7300LC is a 32-bit PA-RISC processor, implementing PA-RISC version 1.1c. It is single-processor only and two-way superscalar, so it can decode, dispatch and execute two instructions per cycle. As the PA-7100LC, only the first ALU can handle loads, stores and shifts which can only be paired with simple math operations, like integer addition or multiplication.

There are three integrated functional units in PA-7300LC: two Integer ALUs and one Floating Point unit (FPU) plus MAX-1 multimedia extensions for multimedia applications. The PA-7300LC CPU has a five-stage pipeline.

The Translation Lookaside Buffer (TLB) has 96 unified instruction and data entries and translates virtual-to-physical memory addresses, the Block Translation Lookaside Buffer (BTLB) with 8 entries translates pages.

Cache and memory

PA-7300LC processors have an on-chip L1 cache of 64 KB/64 KB instruction and data on-chip, each two-way set associative, virtually indexed, cache line size of 32 Byte. An optional L2 cache is off-chip with up to 8192 KB unified, write-through, direct mapped, physically indexed and physically tagged. There is no hashing for both instruction and data caches.

The memory and I/O controller (MIOC) is integrated in PA-7300LC onto the die, for direct DRAM memory and cache interface. Up to 3.75 GB memory is supported.

PA-7300LC moved the instruction prefetch buffer from memory controller to L1 instruction cache, allowing prefetch hits without penalty. The instruction lookaside buffer (ILAB) has four entries for bypassing instructions from MIOC to execution.

The PA-7300LC is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-7300LC processors were fabbed with up to 180 MHz clock speed, on 3.3 V core voltage. They directly attach to the GSC+ main system bus with 32-bit from processor to graphics I/O devices, maximum clock 40 MHz with 160 MB/s Caches have a 64-bit datapath to the execution units, 256-bit datapath to main memory, memory has a 128-bit datapath.

Physical

Fabricated by HP, PA-7300LC had a 15.3×17.0 mm² die with 9,200,000 transistors (FETs), fabbed in a 0.5 μ m, 4-layer HP CMOS14C process packaged in a 464-pin ceramic PGA.

Performance

HP PA-7300LC PA-RISC were performant low-cost microprocessors, on par with RISC and PC competition in 1996. At the same clock, PA-7300LC were slightly faster than Sun UltraSPARC (1995), Pentium Pro (1995) and PowerPC 604e (1996), in SPEC95 scores. Floating point results were weaker.

In comparison, MIPS R10000 (1996) and Pentium II (1997) processors beat PA-7300LC only at higher clock rates. The 64-bit PA-8000 follow-on PA-RISC processors from HP were about 30% faster, at the same clock.

PA-7300LC were significantly faster than their PA-7100LC predecessors and slightly faster than the more expensive but much more expandable PA-7200.

Used in

PA-7300LC processors were used in a few late-1990s HP 9000 workstations and servers, when technical computing was already moving to 64-bit. Systems with PA-7300LC were a medium-performance low-cost option for HP 9000 Unix customers.

- ◇ HP 9000 744, 745, 748 VME workstations
- ◇ HP 9000 A180, A180C servers
- ◇ HP 9000 B132L, B132L+, B160L, B180L+ workstations
- ◇ HP 9000 C132L, C160L workstations
- ◇ HP 9000 D220, D230, D320, D330 servers
- ◇ RDI PrecisionBook laptop
- ◇ Hitachi 3050RX 255, 355E, 365 workstations
- ◇ HP Agilent 16600A, 16700A, 16700B, 16702A and 16702B series logic analyzers

Documentation

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2. The PA-7300LC: the first “System on a Chip” Tom Meyer (1996: Presentation for Microprocessor Forum 1995)
3. The PA 7300LC Microprocessor: A Highly Integrated System on a Chip (PDF, 50 KB) Terry W. Blanchard and Paul G. Tobin (June 1997: Hewlett-Packard Journal)
4. PA7300LC Integrates Cache for Cost/Performance, HP Technical Computing (1997)
5. INTEGRATED PA-7300LC POWERS HP MIDRANGE, MICROPROCESSOR REPORT (VOL.9 NO.15, 1995, HP reprinting)

2.3.13 PA-8000 PA-RISC Processor

PA-8000 was the first 64-bit PA-RISC 2.0 processor by HP, released in 1996. It included out of order execution capabilities, 64-bit integer registers and functional units and a flat 64-bit virtual address space for the first time in PA-RISC.

PA-8000 processors had a completely redesigned core and microarchitecture with ten functional units, a large out-of-order dispatch window and (still) no on-chip caches. Other PA-8000 new features are fast TLB insert and memory prefetch instructions, support for variable sized pages, branch prediction hinting and new floating point units (FPMAC).

The key feature in PA-8000 and PA-RISC 2.0 processors is the Instruction Reorder Buffer (IRB), which performs instruction scheduling in hardware, independent of compiler or software. IRB can store up to 28 computation and 28 load/store instructions, tracks interdependencies between these instructions and allows execution as soon as ready.

All later PA-RISC processors until the PA-8900 are heavily based on the PA-8000 CPU core with only slight extensions plus much bigger caches.

Functional units

The PA-8000 is a 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute four instructions per cycle.

There are ten integrated functional units in the PA-8000: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units, two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The new Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 96 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 256 entries, the Branch History Table (BHT) 256 entries.

Cache and memory

PA-8000 have only large L1 off-chip caches, keeping the PA-RISC tradition. Main L1 cache is up to 1 MB instruction and 1 MB data, off-chip in synchronous 150 MHz 1 Mb SRAMs with one cycle latency. Apparently, the theoretical L1 maximum is 4MB/4MB. There is no L2 cache.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 1 TB with 40-bit physical addresses.

The PA-8000 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8000 processors were fabbed with up to 180 MHz clock speed at 3.3 V core voltage. They attach to Runway bus, 64-bit, 120 MHz, 960 MB/s peak bandwidth.

PA-8000 support glueless multiprocessing interface (four-way MP) on the same Runway bus.

Physical

Fabricated by HP, PA-8000 have a 17.7×19.1 mm die with 3,800,000 transistors (FETs), fabbed in a 0.5μ, 5-layer metal HP CMOS process and packaged in 1,085-pin flip-chip LGA.

Performance

HP PA-8000 PA-RISC were very fast 64-bit microprocessors in 1996, above their RISC competition for technical computing. PA-8000 were faster than IBM PowerPC 604e (1996), Pentium Pro (1995), Pentium II (1997) and MIPS R10000 (1996) at similar to higher clocks speeds, and much stronger in floating point.

PA-8000 were almost par with Pentium II (1997) and UltraSPARC Ii (1997) sold at significantly higher clocks. They were more than 2x faster at the same clock than 32-bit PA-7200 and PA-7300LC predecessors.

Used in

PA-8000 processors were used by many late-1990s HP Visualize technical workstations and HP 9000 servers, after HP switched to 64-bit computing.

- ◇ HP Visualize C160, C180 workstations
- ◇ HP 9000 D270, D280, D370, D380 servers
- ◇ HP Visualize J280, J282 workstations
- ◇ HP 9000 K250, K260, K450, K460 servers
- ◇ HP 9000 R380 servers
- ◇ HP 9000 T600 mainframes
- ◇ HP/Convex SPP2000 (S-Class/X-Class) mainframes
- ◇ NEC TX7/D280, TX7/K370, TX7/P590 servers
- ◇ Stratus Continuum 628, 1228 mainframes

Documentation

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2. PA-8000 Combines Complexity and Speed Linley Gwennap (1994: Microprocessor Report, Volume 8 Number 15)
3. Four-Way Superscalar PA-RISC Processors (.pdf) Anne P. Scott et al (August 1997: Hewlett-Packard Journal)
4. The HP PA-8000 RISC CPU A High Performance Out-of-Order Processor, Ashok Kumar (August 1996: IEEE Hot Chips VIII)
5. PA-8000 Mid-Range and High-End Systems, HP Technical Computing (1997)

6. The HP PA-8000 RISC CPU presentation, Ashok Kumar, HP (1996: IEEE Hot Chips VIII conference)
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2.3.14 PA-8200 PA-RISC Processor

PA-8200 is a 64-bit PA-RISC processor from HP that extended the original 64-bit PA-8000 RISC design in 1997, soon after the original release. Several aspects of the PA-8000 were improved: branch prediction, TLB miss rates and cache sizes.

PA-8200 were designed to offer improved performance and compatibility with existing applications in a short time to market. The availability of new 4 Mb SRAMs with faster access times allowed for increased CPU speed and larger caches. Other “high benefit, low risk” improvements include an increase of BHT and TLB.

PA-8200 was followed by the PA-8500, released a year later in 1998, functionally similar but with large on-chip caches, breaking a long HP PA-RISC tradition.

Functional units

PA-8200 is a 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are ten integrated functional units in the PA-8200: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units, two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 120 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 1024 entries.

Cache and memory

PA-8200 have, in the PA-RISC tradition, large L1 off-chip caches. Main L1 cache is up to 2 MB instruction and 2 MB data, off-chip in synchronous 200 MHz 4 Mb SRAMs with one cycle latency. Caches are direct-mapped and dual-ported. No L2 cache.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 1 TB with 40-bit physical addresses.

The PA-8200 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8200 processors were fabbed with up to 300 MHz clock speed at 3.3 V core voltage. They attach to Runway bus, 64-bit, 120 MHz, 960 MB/s peak bandwidth.

PA-8200 support glueless multiprocessing interface (SMP) on the same Runway bus.

Physical

Fabricated by HP, PA-8200 have a 17.7×19.6 mm die with 4,500,000 transistors (FETs) in a 0.5μ, 5-layer metal CMOS_{14C} process, packaged in 1,085-pin flip-chip LGA.

Performance

HP PA-8200 PA-RISC were very fast 64-bit microprocessors in 1997, above their RISC competition for technical computing. PA-8200 were significantly faster than Pentium II (1997), UltraSPARC III (1997) and Digital Alpha 21164A (1996) that had almost twice the clockspeed. Newer MIPS R10000 (1996/1997) with large caches were only slightly slower than PA-8200.

PA-8200 were only slightly faster than the 64-bit PA-8000, released a year earlier (1996) with slightly lower clock.

Used in

PA-8000 processors were used in few late-1990s HP Visualize technical workstations and some HP 9000 servers, for the top models and as an upgrade to PA-8000.

- ◇ HP Visualize C200, C240 workstations
- ◇ HP 9000 D390 servers
- ◇ HP Visualize J2240 workstations
- ◇ HP 9000 K370, K380, K570, K580 servers
- ◇ HP 9000 R390 servers
- ◇ HP 9000 V2200, V2250 mainframes
- ◇ HP 9000 NEC TX7/V2200 mainframes

Documentation

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 - ◇ *The Evolving RISC Landscape*, Linley Gwennap (MDR), Microprocessor Forum 1997
 - ◇ *PA-8500: Scaling the PA-8200 with a Large Integrated Cache*, Bill Queen (HP), Microprocessor Forum 1997

2.3.15 PA-8500 PA-RISC Processor

The PA-8500 64-bit PA-RISC processor, released in 1998, is the evolution of the PA-8000 and PA-8200 processors, leveraging their processing core but adding large on-die L1 caches. HP released these earlier 64-bit CPUs only in 1996 and 1997.

PA-8500 broke with the long-standing HP tradition of keeping large L1 caches off-chip and was called “High Speed SRAM with an Integrated CPU.” Earlier 32-bit PA-7300LC processors already included on-chip L1 caches as a first, albeit much smaller.

HP’s SVTO design team added no other significant changes to the PA-RISC 64-bit processing core and central IRB, besides small increases to TLB (120 to 160) and BHT (1024 to 2048) and clock up to 300MHz.

PA-8500 won the Microprocessor Report’s “Best RISC Processor” award in 1999, at a time when PA-RISC was already planned to be decommissioned for Itanium (“when it is destined for the scrap heap”).

Functional units

PA-8500 is a 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are ten integrated functional units in the PA-8500: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units (FPMAC), two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 160 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 1024 entries.

Cache and memory

PA-8500 have, breaking a PA-RISC tradition, large L1 on-chip caches. Main L1 cache is 0.5 MB instruction and 1 MB data, on-chip, each 4-way set associative.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 1 TB with 40-bit physical addresses.

The PA-8500 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8500 processors were fabbed with up to 440 MHz clock speed at 2.0 V core voltage. They attach to Runway DDR bus, 64-bit, 125 MHz, 2 GB/s peak bandwidth.

Physical

Fabricated by Intel, PA-8500 have a 21.3×22.0 mm die with 140,000,000 transistors (FETs) in a 0.25μ, 5-layer aluminium CMOS process, packaged in 544 LGA.

Picture: PA-8500 and backside on HP Visualize C360 workstation, Wikipedia.

Performance

HP PA-8500 PA-RISC were some of the fastest 64-bit microprocessors in 1998. They were significantly faster than Pentium II (1997), Pentium III (1999) and Digital Alpha 21264 (1998) at the same or higher clock speed. IBM POWER3 (1998) and UltraSPARC Ili (1997) were almost on par at the same clock. SGI MIPS R12000 (1998) was slower than PA-8500 and only sold at lower frequencies.

PA-8500 was shipped with higher clock speeds than earlier 64-bit PA-8200 (1997) and a bit faster in integer and significantly faster in floating point. Notably, it won the Microprocessor Report's "Best RISC Processor" in 1999, "when it is destined for the scrap heap." (i.e. decommissioned for Itanium)

Used in

PA-8500 processors were used in high-end HP Visualize workstations and HP Integrity servers of the very late 1990s and early 2000s.

- ◇ HP 9000 A400-44 (rp2400), A500-44 (rp2450) servers
- ◇ HP Visualize B1000, B2000 workstations
- ◇ HP Visualize C360, C3000 workstations
- ◇ HP Visualize J5000, J7000 workstations
- ◇ HP 9000 L1000-36, L1000-44 (rp5400), L2000-36, L2000-44 (rp5450) servers
- ◇ HP 9000 N4000-36, N4000-44 (rp7400) servers
- ◇ HP 9000 V2500 mainframes
- ◇ Stratus Continuum 419, 429, 616S, 616, 619, 629, 1219, 1229 mainframes

Documentation

- ◇ HP Pumps Up PA-8x00 Family, Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14)
- ◇ A 500 MHz 1.5 MByte Cache with On-Chip CPU, Jonathan Lachman and J. Michael Hill (1997: ISSCC) **parisc linux**
- ◇ PA-8500: The Continuing Evolution of the PA-8000 Family, Gregg Lesartre and Doug Hunt (1997: Proceedings of CompCon, IEEE CS Press)
- ◇ Microprocessor Forum 1997 Conference Proceedings, (October 1997: MicroDesign Resources)
 - *The Evolving RISC Landscape*, Linley Gwennap (MDR), Microprocessor Forum 1997
 - *PA-8500: Scaling the PA-8200 with a Large Integrated Cache*, Bill Queen (HP), Microprocessor Forum 1997

- ◇ ALPHA WILL EXIT THE YEAR IN POLE POSITION (AGAIN), Computer Business Review (1999) techmonitor.ai

2.3.16 PA-8600 PA-RISC Processor

The PA-8600 is an 64-bit HP PA-RISC processor from HP, released in 2000 and based on a modified PA-8500 (1998) in a new manufacturing process to achieve higher clock speeds. Released shortly after the PA-8500, the PA-8600 was offered by HP as direct upgrade path for many HP 9000 servers and workstations for up to 550 MHz clock speed, utilizing the newer HP Runway+ DDR bus.

PA-8600 are basically uptuned PA-8500 processors, rated for higher clock speeds and a modified manufacturing process at Intel, HP's fabrication partner for a while in the 2000s before switching to IBM with the enhanced PA-8700 RISC CPU.

Functional units

PA-8600 is a 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are ten integrated functional units in the PA-8600: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units (FPMAC), two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 160 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 2048 entries.

Cache and memory

PA-8600 have large L1 on-chip caches, like PA-8500 for the first time before. Main L1 cache is 0.5 MB instruction and 1 MB data, on-chip, each 4-way set associative, with quasi LRU replacement policy for instruction cache.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 1 TB with 40-bit physical addresses.

The PA-8600 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8600 processors were fabbed with up to 550 MHz clock speed at 2.0 V core voltage. They attach to Runway DDR bus, 64-bit, 125 MHz, 2 GB/s peak bandwidth.

Physical

Fabricated by Intel, PA-8600 have a 21.3×22.0 mm² die with 140,000,000 transistors (FETs) in a 0.25μm, 5-layer metal CMOS process, packaged in 544 LGA.

Performance

HP PA-8600 PA-RISC were fast 64-bit microprocessors of the early millenium (2000) and followed the PA-8500 performance-wise with slightly higher frequencies. The PA-8600 were in the same ballpark as higher clocked UltraSPARC III (2001), Pentium III Xeon (1999) and faster than Digital Alpha 21264 (1998). Performance was even with IBM RS64-VI (2000) and MIPS R14000 (2001) RISC processors at similar clock, while the newer Digital Alpha 21364 (2001) was faster with higher frequencies.

PA-8600 was notably faster than the first Itanium Merced (2001) from HP and Intel at higher clock-rates, which in turn were much stronger in floating point (50%).

Used in

PA-8600 processors were used in high-end HP Visualize workstations and HP Integrity servers of the very late 1990s and early 2000s.

- ◇ HP 9000 A400-5X (rp2400), A500-5X (rp2450) servers
- ◇ HP Visualize B2000 (some), B2600 workstations
- ◇ HP Visualize C3600 workstations
- ◇ HP Visualize J5600, J6000, J7600 workstations
- ◇ HP Visualize L1000-5X (rp5400), L2000-5X (rp5450), L1500-5X (rp5430), L3000-5X (rp5470)
- ◇ HP 9000 N4000-5X (rp7400) servers
- ◇ HP 9000 V2600 mainframes
- ◇ HP 9000 Superdome mainframes (SD16000, SD32000, SD64000)
- ◇ NEC NX7000/L1000, NX7000/L2000, NX7000/L3000 servers
- ◇ Stratus Continuum 439, 449, 651-2, 652-2, 1251-2, 1252-2 mainframes

Documentation

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2. HP UNVEILS PA-8600 CHIP DETAILS, Hewlett Packard, March 1999
3. A 600 MHz 64 b PA-RISC microprocessor, K.A. Hurd, 2000 IEEE International Solid-State Circuits Conference

2.3.17 PA-8700 PA-RISC Processor

PA-8700 is an 64-bit HP PA-RISC processor from HP, released in 2001. It is based on an enhanced PA-8500 PA-RISC core with several modifications. As with other PA-8x00 processors, the PA-8700 central logic core is close to the original 64-bit PA-8000 from 1997. PA-8700 integrated significant larger on-chip L1 cache (2.25 MB) and TLB (240) compared to predecessors PA-8600 (1.5 MB and 160).

PA-8700 was the last conventional PA-RISC 2.0 processor, before the move to dual-core PA-8800 and PA-8900. Released in 2001, PA-8700 were a stop-gap measure by HP while waiting for Itanium processor to ship – originally planned for 1999. As MPR put it, “HP is developing a processor called the PA-8700 to extend its current RISC line, tiding over customers until Merced systems are available.”

PA-8700 were followed by dual-core PA-8800 processors, the end of the line for PA-RISC in 2004. The 875 MHz version of PA-8700 was called PA-8700+, both were used in top-range 64-bit PA-RISC workstations and many servers of the early 2000s.

HP switched to a new manufacturing partner and brand-new process with PA-8700, moving from Intel to IBM fabs using silicon-on-insulator (SOI) and 0.18 μ m. This helped increase the CPU clock speed to 875 MHz. At its time, PA-8700 was one of the largest commercial processors and one of the first manufactured in SoI.

Functional units

PA-8700 is a 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are ten integrated functional units in the PA-8700: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units (FPMAC), two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 240 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 2048 entries.

Cache and memory

PA-8700 have very large L1 on-chip caches. Main L1 cache is 0.75 MB instruction and 1.5 MB data, on-chip, each 4-way set associative, with quasi LRU replacement policy for instruction and data cache and data pre-fetching capability

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 16 TB with 44-bit physical addresses.

The PA-8700 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8700 processors were fabbed with up to 750 MHz and 875 MHz (PA-8750+) clock speed at 1.5 V core voltage. They attach to Runway DDR bus, 64-bit, 125 MHz, 2 GB/s peak bandwidth.

Physical

Fabricated by IBM, PA-8700 have a 16.0×19.0 mm die with 186,000,000 transistors (FETs) in a 0.18µm 7-layer Silicon-on-Insulator CMOS process, packaged in 544 LGA.

Performance

HP PA-8700 PA-RISC (2001) were still fast 64-bit CPUs in the early 2000s when competitors started increasing clock speeds for more performance. PA-8700 were ballpark as higher clocked as higher clocked UltraSPARC III (2001), Alpha 21364 (2001) and IBM POWER4+ (2003), faster than Pentium III Xeon (1999) and almost even with MIPS R14000 (2001).

The first Itanium Merced (2001) from HP and Intel was notably much slower than PA-8700 in integer but on par in floating point, while the second generation Itanium McKinley (2002) was faster with more than double the floating point performance.

Used in

PA-8700 processors were used in high-end HP Unix workstations and especially servers of the early 2000s.

- ◇ HP 9000 A400-6X (rp2430), A500-6X, A500-7X (rp2470), rp2405 servers
- ◇ HP Visualize C3650, C3700, C3750 workstations
- ◇ HP Visualize J6700 workstations
- ◇ HP Integrity L1500-6X, L1500-7X, L1500-8X (rp5430), L3000-6X, L3000-7X, L3000-8X (rp5470) servers
- ◇ HP 9000 N4000-6X, N4000-7X (rp7400) servers
- ◇ HP Integrity N4000-6X, N4000-7X, N4000-8X (rp7405, rp7410) servers
- ◇ HP 9000 Superdome mainframes (SD16000, SD32000, SD64000)

Documentation

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2.3.18 PA-8800 PA-RISC Processor

The dual-core PA-8800 Mako processor, introduced in 2004, is a PA-RISC 2.0 64-bit processor from HP that integrated two separate PA-8700 cores on a single die with very large off-die L2 caches. The clock speed was only increased slightly from 875 MHz on PA-8700 to 1 GHz on PA-8800, while the processor bus interface was redesigned to use the fast Itanium 2 bus.

Mako was supposed to breathe fresh life in the PA-RISC line, though it had strong internal competition from Itanium, a VLIW development from HP and Intel. PA-8800 was (almost) end of the line for PA-RISC and thus was not marketed much. Most systems with PA-8800 used the HP zx1 chipset and could be upgraded to Itanium 2 IA64 processors.

PA-8800 was at the time of release one of the largest commercial processor chips ever, followed by the mysterious PA-8900 processor in 2005.

Functional units

PA-8800 is a dual-core 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are two separate cores with each ten integrated functional units in the PA-8800: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units (FPMAC), two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer per core for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 240 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 2048 entries – all per core.

Cache and memory

PA-8800 have on-chip L1 caches and very large off-chip L2 caches. Main L1 cache is 0.75 MB instruction and 0.75 MB data on-chip, per core, each 4-way set associative. L2 cache is 32 MB off-chip with four 8 MB DDR-ESRAM chips, shared between the cores, L2 controller is on-chip.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 16 TB with 44-bit physical addresses.

The PA-8800 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8800 processors were fabbed with up to 1 GHz clock speed at 1.5 V core voltage. They attach to Itanium processor bus, 128-bit, 200 MHz, 6.4 GB/s bandwidth.

Cache speed to L2 is 300 MHz clock with 2.7 GB/s data rate per ESRAM (four).

Physical

Fabricated by IBM, PA-8800 have a 23.6×15.5 mm die with 300,000,000 transistors (FETs) in a 0.13µm 8-layer Silicon-on-Insulator CMOS process. IBM used a similar process for its IBM POWER4 processors.

Performance

HP PA-8800 PA-RISC were (almost) last of the line of 64-bit PA-RISC processors, the dual-core integration the last development step to increase the performance of the original PA-8000 core. Few formal SPEC benchmark scores exist for PA-8800.

PA-8800 was a very fast RISC processor when released in 2004 and much faster at the same clockspeed than Alpha 21364 (2001), IBM POWER4+ (2003), Itanium McKinley (2002). It was in the same ballpark as AMD Athlon XP (2002), Intel Xeon DP (2003) and Pentium 4 Prescott (2003) at much higher (more than double) the frequencies.

Used in

PA-8800 processors were used in the last PA-RISC-powered HP Unix workstations and servers in the mid-2000s, when HP planned Itanium processors for high-end models.

- ◇ HP C8000 workstations
- ◇ HP 9000 L1500-9X (rp5430), L2000-9X (rp5450) servers
- ◇ HP Integrity N4000-9X (rp7405, rp7410) servers
- ◇ HP Integrity rp3410, rp3440 servers
- ◇ HP Integrity rp4410, rp4440 servers
- ◇ HP Integrity rp7420 servers
- ◇ HP Integrity rp8400, rp8410, rp8420 servers
- ◇ HP Integrity Superdome mainframes (SD16A, SD32A, SD64A)

Documentation

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2.3.19 PA-8900 PA-RISC Processor

PA-8900 is a slightly tweaked PA-8800 PA-RISC 64-bit processor with increased cache (L2) and higher clock speed of 1.1 GHz. It was released by HP in 2005, only one year after PA-8800 as the last PA-RISC processor in RISC lineup. There were no more PA-RISC processors and products after PA-8900 and the HP c8000 workstation with dual PA-8900 was the pinnacle of PA-RISC workstation computing.

HP planned to transition its Unix computers to the Itanium (IA64) platform, a VLIW architecture called EPIC by HP, that had been in joint development for more than a decade by HP and Intel. Alas Itanium was never truly successful, shipped late and was often slower than the RISC systems it was supposed to supersede.

When HP dropped its line of Itanium and Unix workstations in the mid-2000s, PA-8900-powered C8000 were one of the last and quickest HP-UX Unix workstations, only shaded by Itanium 2 zx6000 workstations. Information on the PA-8900 is limited, as was apparently its distribution in the market.

Functional units

PA-8900 is a dual-core 64-bit PA-RISC processor that implements version 2.0 of PA-RISC architecture. It is multi-processor capable (SMP) and four-way superscalar, so it can decode, dispatch and execute multiple instructions per cycle.

There are two separate cores with each ten integrated functional units in the PA-8900: two Integer ALUs, two shift/merge units, two complete load/store pipelines, Floating Point multiply/accumulate units (FPMAC), two Floating Point divide/square root units plus plus MAX-2 multimedia extensions (subword arithmetic) for multimedia applications.

The Instruction Reorder Buffer (IRB) has an 56-entry instruction queue/reorder buffer per core for instruction scheduling in hardware by the CPU.

The Translation Lookaside Buffer (TLB) with 240 entries, fully associative and dual-ported, translates virtual-to-physical memory addresses, the Branch Target Address Cache (BTAC) has 32 entries, the Branch History Table (BHT) 2048 entries – all per core.

Cache and memory

PA-8900 have on-chip L1 caches and very large off-chip L2 caches. Main L1 cache is 0.75 MB instruction and 0.75 MB data on-chip, per core, each 4-way set associative. L2 cache is 64 MB off-chip with possibly DDR-ESRAM chips, shared between the cores, L2 controller is on-chip.

Memory and I/O controller (MIOC) for accessing the memory and main buses is off-chip. Main memory is supported up to 16 TB with 44-bit physical addresses.

The PA-8900 is bi-endian with support for little-endian and big-endian ordering.

Speed and buses

PA-8900 processors were fabbed with up to 1.1 GHz clock speed at 1.5 V core voltage. They attach to Itanium processor bus, 128-bit, 200 MHz, 6.4 GB/s bandwidth.

Physical

Fabricated possibly by IBM, PA-8900 have a 23.6×15.5 mm die with 317,000,000 transistors (FETs) in a 0.13µm 8-layer Silicon-on-Insulator CMOS process.

Performance

HP PA-8900 PA-RISC were the pinnacle of 64-bit PA-RISC processor design, and improved on the PA-8800 only slightly. No formal SPEC benchmark scores exist.

PA-8900 was still a very fast RISC processor when released in 2005 and faster at the same clockspeed than Alpha 21364 (2001), IBM POWER4+ (2003) and Itanium McKinley (2002). Contemporaries such as AMD Athlon XP (2002) and Intel Xeon (2003) had similar performance at much higher frequencies, AMD Opteron (2005) was faster.

Used in

PA-8900 processors were used in the very final PA-RISC-powered HP Unix workstations and servers in the mid-2000s, when HP reserved Itanium processors for high-end models.

- ◇ HP c8000 workstations
- ◇ HP Integrity rp3410, rp3440 servers
- ◇ HP Integrity rp4410, rp4440 servers
- ◇ HP Integrity rp7440, rp8440 servers
- ◇ HP Integrity L1500-9X (rp5430), L2000-9X (rp5450) servers
- ◇ HP Integrity N4000-9X (rp7405, rp7410) servers
- ◇ HP Integrity Superdome mainframes (SD16B, SD32B, SD64B)

Documentation

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4. HP moves out of pre-Itanium era , CNET 2005

2.3.20 Third Party PA-RISC Processors

Several third-party OEMs designed PA-RISC processors for workstations and servers (Hitachi) but also for embedded systems of the 1990s like set-top boxes, TVs, device controllers and printers.

Table 2.9: Other PA-RISC processors overview

CPU	ISA	Year	Clock	Cache	Bus	Scalar	Units	Controllers
Amiga Hombre	32-bit PA 1.1	1995	125MHz	?	64-bit	1-way	INT	Memory DMA PCI I/O VGA audio Copper Blitter
Hitachi PA/50L	32-bit PA 1.1	1993	33MHz	12KB	?	1-way	INT FP	
Hitachi PA/50M	32-bit PA 1.1	1993	60MHz	12KB	?	1-way	INT FP	
Hitachi HARP-1	32-bit PA 1.1	1994	150MHz	24KB 1MB L2	?	2-way	2 INT FP <i>Vector</i>	
Hitachi HARP-1E	PA-RISC 1.1 32-bit RISC	1995	150 MHz	32 KB 8 MB L2	?	2-way	2 INT FP <i>Vector</i>	
Winbond W89K	32-bit PA 1.1	1994	33/66MHz	4KB	i486	1-way	INT	none?
Winbond W90210 W90215	32-bit PA 1.1	1997	33/66MHz	12KB	i486	1-way	INT MAX-1	DRAM DMA PCI I/O
Winbond W90220 W90221	32-bit PA 1.1	1999	150MHz	8KB	i486	1-way	INT MAC(DSP) MAX-1	DRAM DMA PCI IDE I/O VGA (W90221) TV (W90221)
OKI OP32	32-bit PA 1.1	1994	33MHz	?	?	1-way	INT	DRAM DMA

Amiga Hombre

Between 1992 and 1994, Commodore designed a new graphics chipset to power Amiga computers based on HP PA-RISC, called Hombre. The development effort apparently included HP and was based on a PA-RISC core to be available for 1995 production for a “CD-based Game Machine”, cable TV, MPEG and as a PCI-based graphics accelerator. The Hombre processor design was to be implemented in two chips:

- ◇ 32-bit PA-RISC 1.1, Integer-only

- ◇ CPU chip (Nathaniel) with 32-bit PA-RISC core: RISC integer core based on PA-7150 at 125MHz, DMA interface, audio and CD interfaces, system, display and PCI buses
- ◇ Video chip (Natalie) with graphics functions and buses
- ◇ Both were targeted for 0.6μ, 3-level metal CMOS in 3.3 V in 304-PQFP
- ◇ 50MHz system bus, 64-bit wide
- ◇ with a 5-stage pipeline and 64-bit datapath

OKI OP32 processor

OKI is a Japanese electronics manufacturer, Oki Electric Industry Co., which was part of the Precision RISC Organisation (PRO) for PA-RISC in the 1990s. OKI developed the OP32/50N, a PA-RISC processor, through its OKI Semiconductor business unit in the mid-1990s. OP32 was an embedded controller introduced in 1994, based on a 32-bit PA-RISC design with integrated DRAM and DMA controllers.

The OP32/50N was targeted at laser printers, Fax machines, X terminals and telecom and automotive markets, where it competed with MIPS and other custom RISC designs.

- ◇ PA-RISC version 1.1 32-bit
- ◇ 33 MHz frequency
- ◇ 14.3×14.3 mm die, 1,100,000 FETs, 0.8μ, 3-layer metal CMOS

OKI later spun off the OKI Semiconductor business unit.

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2.3.2.1 Hitachi PA-RISC Processors

Hitachi was part of the PRO consortium for PA-RISC and offered both rebadged and their own workstations with HP processors. In parallel, Hitachi also designed their own custom PA-RISC processors, the PA/50 and HARP-1.

Hitachi PA/50L and PA/50M

The Hitachi PA/50 was a family of PA-RISC 1.1 processors designed and manufactured by Hitachi, released in 1993. Two designs were developed: M with around 100 MIPS and L “low-cost” with around 55 MIPS. Hitachi used them as personal workstation processors and high-end embedded controllers in their own Hitachi workstations.

The PA/50 integrated a set of features not available at that time in other PA-RISC processors like on-chip caches, data-prefetching, a power-saving mode and SDRAM support.

- ◇ PA-RISC version 1.1 32-bit
- ◇ Built-in, pipelined FPU
- ◇ Cache 8 KB L1 instruction, 2-way set-associative, 32-byte blocks, on-chip
- ◇ Cache 4 KB L1 data, 2-way set-associative, 32-byte blocks, copy-back, on-chip
- ◇ Uncacheable memory (per page)
- ◇ TLB: 32/64-entry, 2-way set, 4K-page, each +2 additional block entries
- ◇ BTLB (256 KB-32 MB)
- ◇ Seven 32-bit shadow registers for fast interrupts
- ◇ Data-prefetching
- ◇ Non-blocking cache
- ◇ Power-saving mode, reducing frequency to 1/8
- ◇ Support for SDRAM
- ◇ PA/50L: Up to 33 MHz frequency with 3.3 V core voltage
- ◇ PA/50M: Up to 60 MHz frequency with 5.0 V core voltage
- ◇ 11.5×12.0 mm die, 1,280,000 FETs, 0.6μ(micron), 3-layer metal CMOS packaged in a 160-pin plastic QFP package

Used in

- ◇ Hitachi 3050RX 100C and , 200 workstations

Hitachi HARP-1

Hitachi HARP-1 is a PA-RISC version 1.1 compatible CPU from Hitachi, introduced in June 1994. It is apparently a larger and faster version of the PA/50 processor with not much more information available publicly. The HARP-1E supposedly included pseudo-vector processing modifications used in Hitachi vector supercomputers. L1 cache was increased to 16 KB/16 KB.

- ◇ PA-RISC version 1.1 32-bit
- ◇ Three functional units: two integer ALUs, one floating point unit (FPU) plus two shift-merge units (SMUs)
- ◇ Six-stage pipeline
- ◇ Built-in, pipelined FPU
- ◇ Built-in memory controller Memory Interface Unit, MIU
- ◇ 2-way superscalar
- ◇ Cache 8 KB L1 instruction, 1-way set-associative, 32-byte blocks, on-chip
- ◇ Cache 16 KB L1 data, 2-way set-associative, 32-byte blocks, copy-back, on-chip
- ◇ Cache 512/512 KB L2 instruction/data, off-chip
- ◇ TLB: 128/128-entry instruction/data, 1-way set
- ◇ L2 Cache bus: 128-bit data path to L2 caches with ECC
- ◇ Processor bus: 64-bit data path to main memory and I/O
- ◇ Up to 150 MHz frequency with 3.3 V core voltage, 17W power dissipation at 120 MHz
- ◇ 16.2×16.5 mm² die, 2,800,000 FETs, 0.5μ, 3-layer aluminium + 1-layer tungsten BiCMOS, packaged in 595-pin PGA

Used in

- ◇ Hitachi SR2001 supercomputers
- ◇ Hitachi SR2201 supercomputers (HARP-1E)
- ◇ Probably others

Hitachi HARP-1E

After HARP-1, there was apparently a successor processor presented by Hitachi at HOT CHIPS conference in 1995. It is unclear if that is the HARP-1E and if it was implemented or productized. The concept planned for a high-performance superscalar RISC processor, optimized for large-scale scientific calculations with high-memory throughput and high frequency.

- ◇ PA-RISC version 1.1 32-bit
- ◇ Three functional units: two integer ALUs, one floating point unit (FPU) plus two shift-merge units (SMUs)
- ◇ Six-stage pipeline
- ◇ 2-way superscalar: two instructions issues per cycle, four operations
- ◇ Vector processing PVP-SW (Pseudo-Vector Processing based on slide-windowed registers)
- ◇ Cache 16/16 KB L1 instruction/data, on-chip, direct-mapped, 32-byte blocks
- ◇ Cache 4/4 MB L2 instruction/data, on-chip?, 128-byte lines, ECC
- ◇ TLB: 256/256-entry instruction/data, direct-mapped

- ◇ BTLB: 8k-entry 2-way set associative
- ◇ Branch History Table (BHT) 1024-entry
- ◇ Up to 150 MHz frequency with 2.5 V core voltage, 13 W power dissipation
- ◇ 15.7×15.7 mm die, 4,500,000 FETs, 0.3µm-layer metal CMOS, packaged in 1672-pin PGA

Used in

- ◇ Not sure

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2.3.22 Winbond PA-RISC Processors

Winbond W89K

Winbond W89K is an embedded 32-bit PA-RISC controller chip, introduced in Spring 1994 and pin-compatible with Intel 80486DX. W89K were designated embedded processors for appliances and integrated devices. To ease development, W89K could be used as a drop-in replacement for i486 CPUs in mid-1990s PCs, together with Winbond BIOS replacement.

Rationale was to allow hardware developers utilize existing i486 mainboards and components for a shorter product development process. W89K is a level 0 PA-RISC 1.1 implementation: a 32-bit PA-RISC processor without virtual addressing.

- ◇ PA-RISC version 1.1 32-bit, level 0
- ◇ No virtual addressing: no MMU
- ◇ Five-stage pipeline
- ◇ One functional unit: one 32-bit integer ALU
- ◇ Cache 2 KB/2 KB L1 on-chip instruction/data
- ◇ 80486 Intel bus interface
- ◇ 33 MHz and 66 MHz clock speeds were available, with the latter apparently having been achieved with a clock-doubling also used in the Intel's 80486DX/2
- ◇ On-chip JTAG support
- ◇ 14.3×14.3 mm die, 1,100,000 FETs, 0.8μ, 3-layer metal CMOS

Winbond W90210/215

Shortly after the W89K, Winbond introduced more sophisticated PA-RISC processors in 1997 with the W90K line of embedded controllers. W90210F are 32-bit PA-RISC 1.1 implementations and integrated many external I/O components on the chip—DRAM and DMA controllers, PCI bridge and various I/O ports.

As its predecessor, Winbond W90210F implemented PA-RISC 1.1 level 0 without virtual addressing. They were used in various “Internet appliances”: set-top boxes, TV sets, DVD players, PDAs, photo frames, VoIP devices, and for industrial automation. W90215 were identical to W90210 but did not include license rights for the embedded operating system and thus cheaper.

- ◇ PA-RISC version 1.1 32-bit
- ◇ Level 0 implementation no virtual addressing: no MMU
- ◇ Five-stage pipeline
- ◇ One functional unit: one 32-bit integer ALU
- ◇ Cache 4 KB L1 instruction, direct mapped, 32-byte blocks, 256 entries
- ◇ Cache 8 KB L1 data, 2-way set-associative, 32-byte blocks, 2×64 entries, write-back
- ◇ MAX-1 multimedia extensions for multimedia applications, like MPEG decoding
- ◇ 80486 Intel bus interface

- ◇ DRAM controller
- ◇ ROM/FLASH interface
- ◇ DMA controller 2-channel 8-bit
- ◇ PCI bridge
- ◇ Two serial ports
- ◇ Parallel port
- ◇ 33 MHz and 66 MHz clock speeds
- ◇ 208-pin PQF package

Winbond W90220 and W90221

W90220F are 32-bit PA-RISC 1.1 processors without MMU but with many integrated I/O components. On-chip were DRAM and DMA controllers, PCI bridge, IDE channels, I/O ports and, on the W90221, a graphics/TV chip. Later W90221 were apparently similar chips but with higher clock speeds, integrated (S)VGA and TV controller

- ◇ PA-RISC version 1.1 32-bit
- ◇ Level 0 implementation, no virtual addressing: no MMU
- ◇ Six-stage pipeline
- ◇ Two functional units: one 32-bit integer ALU and one 32-bit multiply-accumulate MAC module, for DSP purposes, can be used as two 16-bit modules too
- ◇ Cache 4 KB L1 instruction, direct mapped, 32-byte blocks, 256 entries
- ◇ Cache 4 KB L1 data, 4-way set-associative, write-back or write-through
- ◇ MAX-1 multimedia extensions for multimedia applications, like MPEG decoding
- ◇ 80486 Intel bus interface
- ◇ Hardware *dynamic* branch prediction
- ◇ 256-entry branch-target-buffer BTAC
- ◇ Memory controller supports DRAM, EDO-DRAM and SRAM; W90221 additionally SDRAM
- ◇ ROM/FLASH interface
- ◇ DMA controller 2-channel 8-bit
- ◇ IDE I/O controller four 16-bit channels
- ◇ W90221: VGA and TV controller W9971
- ◇ PCI bridge
- ◇ Two serial ports
- ◇ Parallel port
- ◇ Serial ICE port
- ◇ Up to 150 MHz clock speed at 3.3 V/5 V I/O and 3.3 V core

- ◇ W90221: 133 MHz clock speed with apparently 3.3 V at both I/O and core
- ◇ 0.35µsingle-poly-triple-metal CMOS
- ◇ 208-pin PQF package

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2.3.23 HP FOCUS Processor

With Frank McConnell

HP FOCUS is an early 1980s 32-bit HP custom design that predated widespread RISC usage and PA-RISC architecture. It was used in HP 9000 500 computers, the first HP 9000 series. FOCUS was a stack architecture implemented in five NMOS-III VLSI chips in 1.5 micron: CPU, I/O processor (IOP), memory controller, 128Kb RAM (16KB cache), clock driver.

FOCUS processors run at 18 MHz with “direct address range” of “500 MB” (probably 29-bit direct addressing for 512 MB). It was fabricated with 450,000 FETs, integrated with three Floating-Point chips onto one “finstrate” CPU board. The FOCUS CPU was microcoded with 9,000 38-bit microcode control stores and implemented the HP 3000 computers’ stack-based architecture in 32-bit. All internal data paths and registers are 32-bit wide. Due to heat dissipation difficulties the ICs were mounted on special printed-circuit boards called “finstrates” — the board has a 1mm copper sheet as core to which the IC substrate is epoxied directly.

The I/O Processor (IOP) executes all I/O instructions and handles the transactions from/to the eight attached HP CIO channels. It has an I/O bandwidth of 5.1 MB/s burst and 973 KB/s multiplexed. The IOP was also a microprogrammed (4,608 32-bit microcode stores) NMOS-III VLSI chip.

At least one IOP to interface with the I/O buses was needed so up to six CPUs were supported in hardware but only three in software. Up to two additional IOPs could be installed for more I/O options; each additional IOP needed an I/O expander which provided the I/O channels extension, the CIO bus.

The three finstrates boards of CPU, IOP and 256 KB RAM were installed in a 12-slot HP 9000/520 module. This allowed configurations of up to 10 MB of RAM; memory cards could be substituted to construct multiprocessor systems. CPU, IOP and memory controller communicate via memory processor bus, MPB. The 44-line, 18 MHz, 36 MB/s MPB supports up to seven (other sources mention three/three) CPUs or IOPs and fifteen memory controllers.

Architecture

FOCUS is a stack architecture with 230 instructions (both 16 and 32 bits wide), a segmented memory model, and no general purpose programmer-visible registers. There are thirty-nine 32-bit registers in the CPU hardware — thirty-one internal 32-bit general purpose registers, two 32-bit ALU registers, and others.

FOCUS has a flat address space but that is not really what most programs see: their access to memory is largely described by registers that contain the absolute memory addresses of segment boundaries. For example, instructions come from the current code segment, which is described by three registers: **P**, the program counter, which is a 32-bit register containing the absolute address of the instruction being executed; **PB**, the program base register, which is a 32-bit register containing the absolute address of the first word of the current code segment; and **PL**, the program limit register, which is a 32-bit register containing the absolute address of the last word of the current code segment.

The data segment also has base (**DB**) and limit (**DL**) registers, and so does the stack segment (**SB**, **SL**). The stack segment also has a stack pointer (**S**) and a stack marker pointer (**Q**) which points to the current procedure’s activation record on the stack.

There is also an index register, a status register, a flags register (really a sort of debugging-state register), a message register (interrupting conditions) and message mask register (which enables/disables

interrupts from the message register), a breakpoint register, and a couple of registers which are for the memory controllers to talk to the CPU.

The machine instruction set is oriented toward moving words between memory and the top of the stack, and operating on the words at the top of the stack. To take an addition of two numbers: load one, load the other, execute an **ADD** instruction, and then a store instruction if the result should be kept somewhere in memory other than on the stack.

The stack is in memory, there are (probably) some numbers of “top of stack” registers inside the processor to keep things moving relatively quickly, but these registers are not otherwise visible to the programmer.

Details

- ◇ FOCUS stack architecture, 32-bit
- ◇ Main processor consists of five VLSI chips
- ◇ Clock speed 18 MHz
- ◇ External Floating Point Unit
- ◇ I/O Processor (IOP)
- ◇ Computing units:
 1. Integer/load/store unit
 2. Floating point
- ◇ Thirty-one 32-bit integer registers, two ALU registers, plus external floating point registers
- ◇ Cache L1 16 KB instruction and data off-chip
- ◇ Up to six processors (SMP) supported in hardware, three in software (OS)
- ◇ Up to “500” MB main memory could be addressed in a single system (10 MB in reality)
- ◇ CPU attaches via MPB bus to memory, I/O, 44-bit bus, 36 Mb/s data rate
- ◇ One circuit board, CPU implemented in NMOS-III, five chips 1.5µ
- ◇ Pictures: FOCUS CPU board and rear, Wikipedia, Thomas Schanz 2013

Used in

- ◇ HP 9000 500: 520, 530, 540, 550

Documentation

1. An 18-MHz, 32-bit VLSI Microprocessor (.pdf, pp. 7-10) Kevin P. Burkhart (August 1983. Hewlett Packard Journal. Accessed January 2008) **hp museum**
2. Hewlett-Packard 9000 Series 520 Frank McConnell (1997. Accessed January 2008)

Pictures Hewlett Packard, scans from product brochures, from hpmuseum.net and 1000bit.it

2.3.24 Apollo PRISM Processor

Apollo PRISM was a RISC processor with VLIW (Very Long Instruction Word) design, developed by Apollo Computer Inc. and released in 1988. It was implemented in CMOS with eleven VLSI chips at 20 MHz clock and able to combine three instructions into one. For the time, PRISM was billed as one of the fastest RISC processors, able to support up to two four CPUs in a single system (SMP).

PRISM's processors were used in Apollo's own Domain 10000 (DN10000) computers, with a PRISM II processor already being planned and designed. After the acquisition by HP in 1989, Apollo products were integrated into the HP line up, but the PRISM II processor dropped. In 1989 HP was still communicating an upgraded PRISM processor ("DN10000TX upgrade") with streamlined architecture, higher clock, double computing power (from 22 to 44 MIPS), increased caches to be fabbed by HP's Colorado ASIC factory in 1991 in 1.0µ.

PRISM was sometimes codenamed A88K (or a88k), not to be confused with the Motorola M88K 88000 RISC processors. Parts of the PRISM architecture were later reused in PA-RISC, specifically technologies for HP's own floating-point units (FPUs).

2.3.25 PRISM Details

- ◇ Apollo PRISM RISC VLIW architecture, 32-bit
- ◇ Designed and used by Apollo Computers in 1988-89
- ◇ CPU design consists of eleven VLSI chips:
 1. IP: The Integer processor for calculations, addresses and sequencing
 2. MMU: Memory Management Unit from Toshiba
 3. FPC: Floating Point Control decodes and executes FP instructions
 4. Two FRFs: Floating Point Register File
 5. CBA: CPU Bus Address unit for the address path to cache and X-bus
 6. Two CBDs: CPU Bus Data unit for the data path to cache and X-bus
 7. SCR: Scan and Clock Resource
 8. FP ALU: from Bipolar Integrated Technology (BIT)
 9. FP MUL: also from BIT
- ◇ Two 32-bit integer registers, 32 floating point registers
- ◇ Cache L1 128 KB instruction and 64 KB data off-chip
- ◇ Shared virtual memory multiprocessing
- ◇ Up to 720 MB main memory could be addressed in a single system
- ◇ CPU attaches via X-Bus to memory, I/O and graphics, 64-bit bus, 150 Mb/s
- ◇ CPU implemented in nine chips in 1.5µVLSI CMOS plus two bipolar FP chips
- ◇ Clock speed 20 MHz (or 18.18 MHz)
- ◇ FPU from BIT (Bipolar Integrated Technologies)

Used in

- ◇ Apollo Domain DN10000 workstations
- ◇ Apollo Domain DSP10000 servers

2.3.26 PRISM₂ (DN10000TX)

- ◇ Upgrade PRISM processor designed by HP in 1991
- ◇ Apparently never marketed or productized
- ◇ Processor integrated in eighth VLSI chips instead of eleven
 1. IPU: Custom integration of IP, MMU and FPC
 2. FPU: Bipolar B2130 floating point unit
 3. Two KRF: Floating point register file
 4. Two KBD: X-bus data handling
 5. KBA:X-bus address handling
 6. SCR: clocks and testing
- ◇ Caches increased to 512/512 KB L1 (Motorola SRAMs)
- ◇ 64-bit data path (two buses) to the caches
- ◇ TLBs 32-entry primary (PTB) and 16K entries secondary (STB)
- ◇ “Second generation” Floating Point processors (BIT B2130)
- ◇ X-bus data backplane 64-bit
- ◇ Up to four-way SMP multi-processing
- ◇ Clock speed increased to 30 or 36 MHz
- ◇ Fabricated in HP’s 1.0µVLSI technology

Benchmarks

Table 2.10: Based on Dhrystone and MIPS archives; * - unsure

System	Processor	SPEC89	MIPS
Apollo DN10000	Apollo PRISM 18 MHz	19	22
Apollo DN10000	4 Apollo PRISM 18 MHz		60-100*
Apollo DN10000-TX	Apollo PRISM ₂ 36 MHz		44*

Comparison to SPEC benchmark data from other contemporary Unix computers:

Table 2.11: Based on Dhrystone archives

System	Processor	SPEC89	MIPS
HP 9000 705	PA-7000 35 MHz	34	49

Intel	i486DX2 66 MHz	25	31
Sun SPARCstation 2	SPARC 40MHz	25	28
DECstation 5000/200	MIPS R3000 25MHz	23	22
DECstation 3100	MIPS R2000 16MHz	11.8	15.1
HP 9000 425e	Motorola M68040 25MHz	10.3	18*
HP 9000 834	NS-1 PA-RISC 30 MHz	9.5	14
Intel	i386 33MHz	4.3	8
DEC VAX 11/780	KA780 3.4MHz	1.0	0.9

Documentation

1. *The DN 10000TX: a new high-performance PRISM processor*, COMPCON Spring '91 Digest of Papers, 1991
2. APOLLO COMPUTER LAUNCHES ITS 64-BIT PRISM RISC MACHINE, Tech Monitor archive, February 29, 1988
3. WHY APOLLO COMPUTER RECKONS IT HAS OUTDONE SUN IN THE RISC STAKES, Tech Monitor archive, March 14, 1988
4. Apollo CPUs, Apollo/DOMAIN Computers at zepa.net, 2003 (from 20030201)
5. HP unveils plan for new PRISM CPU, Hewlett Packard, Press Release October 1989 100obit.it

2.4 PA-RISC Performance and CPU History

2.4.1 Overview

HP developed three generations of PA-RISC processors between the 1980s and 2000s. Processors of the Precision Architecture, also called *HP-PA*, were used in many HP Unix technical computers, competing with other contemporary RISC architectures.

1. **PA-RISC 1.0** 32-bit, implemented in early 1980s processors and used in first PA-RISC servers: NS-1, NS-2 and PCX, plus the TTL TS-1 and maybe others.
2. **PA-RISC 1.1** 32-bit, used in popular HP 9000 servers and workstations from the late-1980s to 90s: PA-7000 and PA-7100 and integrated PA-7100LC and PA-7300LC.
3. **PA-RISC 2.0** 64-bit, used in many 1990s/2000s HP computers: PA-8000/PA-8200 and the updated PA-8500, PA-8600 and PA-8700 with large on-chip caches. PA-8800 and PA-8900 are dual-core, with the final PA-9000 never implemented.

HP Precision Architecture is an offspring from HP research and development in the 1980s to replace 16-bit stack-based CPUs in HP 3000 servers and Motorola CPUs in Unix systems with a common system architecture. PA-RISC platform and ISA were “built from the ground up” by HP engineers.

PA-RISC was implemented almost exclusively in HP processors in its VLSI Technology Center (VTC) and Systems & VLSI Technology Operation (SVTO), from early version in TTL and NMOS in the 1980s to integrated 32-bit and 64-bit RISC processors in the early 2000s with modern technologies.

2.4.2 PA-RISC 32-bit in the 1990s

PA-7000

HP PA-7000 PA-RISC processors (1991) were average RISC performers of the early 1990s with roughly the same performance as MIPS R3000A (1992), Motorola 88100 (1988) and SPARC (1991 implementations) but slightly slower than IBM POWER1 (1990), Sun SuperSPARC (1992) and MIPS R4000 (1991) at similar clocks.

Compared to personal computers in that era, PA-7000 were faster than Intel 486DX2 (1992) and level with later Pentium P5 (1993) at the same frequencies, but significantly stronger in floating point than both.

PA-7100

HP PA-7100 PA-RISC processors were rather fast microprocessors for their time in 1992, on par with their RISC competition and beating even newer processors in floating point. At the same clock, PA-7100 were almost level with Pentium P54C (1994) and MIPS R4400SC (1992) but significantly faster in floating point, SPEC95.

They were significantly faster than DEC Alpha 21064 (1992), slightly faster than IBM PowerPC 604 (1994) but beaten by higher-clocked Intel Pentium Pro (1995).

PA-7100LC

PA-7100LC were the first integrated PA-RISC processors, released by HP in 1994. With a simple 32-bit PA-RISC superscalar core, they integrated memory and I/O controllers onto the chip and made highly-integrated PC-like workstations possible in the mid-1990s. They carried “HP’s high-volume products” for 2.5 years.

For 1994, PA-7100LC were fast, integrated low-cost microprocessors, on par with RISC and PC architectures of the time. At the same clock, PA-7100LC were in the ballpark of IBM PowerPC 604 (1994) and beat Pentium P54C (1994) and MIPS R4400SC (1992) in SPEC92 scores. They were much stronger in floating point.

As MPR put it, PA-7100LC were significantly faster “than the PowerPC 601 and dramatically faster than the TI microSPARC,” and had “far better FP performance” than Sun’s microSPARC II and outran “the fastest SuperSPARC chip” in SPEC92 scores.

There was a long gap until 1996, when HP released the follow-on PA-7300LC, another highly integrated CPU with similar product outlook. HP missed the chance to improve production processes or increase clock speed above 100MHz, losing the competitive edge in 32-bit RISC computing in the mid-1990s.

PA-7200

HP PA-7200 PA-RISC were very strong microprocessors for 1995, usually above their RISC competition in technical computing. PA-7200 were much faster than IBM PowerPC 604 (1994), Pentium P54C (1994) and MIPS R5000 (1996) at similar frequencies with almost twice the performance in floating point.

PA-7200 were almost equal to higher-clocker Pentium Pro (1995) and UltraSPARC (1995) and not far from Digital Alpha 21164 (1996) at significantly higher clock.

PA-7300LC

HP PA-7300LC was another 32-bit integrated PA-RISC processor, released in parallel to HP’s newer 64-bit PA-8000 to “revitalize HP’s low-end and midrange systems.” It was based on the PA-7100LC core with large on-chip caches, “relatively simple by current standards” to update “high-volume products” after 2.5 years of PA-7100LC.

Due to the on-chip memory, I/O and cache controllers, PA-7300LC could be used in highly integrated systems that used the same I/O devices as the PA-7100LC, due to the same GSC main bus and system design.

Even though HP designers planned the PA-7300LC to “out-perform every processor shipping today [1995] except Digital’s 21164,” it was clear “high-end RISC chips from a number of vendors are likely to surpass the 7300LC’s performance before it debuts.” HP had a “lack of processor design resources” and its “competitive edge has ebbed after new processor introductions.”

In the end, PA-7300LC PA-RISC were solid low-cost RISC processors, on par with competing microarchitectures in 1996. At the same clock, PA-7300LC were slightly faster than Sun UltraSPARC (1995), Pentium Pro (1995) and PowerPC 604e (1996), in SPEC95 scores. Floating point results were weaker.

In comparison, MIPS R10000 (1996) and Pentium II (1997) processors beat PA-7300LC with higher clock rates. The 64-bit PA-8000 follow-on PA-RISC processors from HP were about 30% faster at the same clock.

2.4.3 PA-RISC 64-bit (90s/2000s)

HP moved PA-RISC to 64-bit with the PA-RISC 2.0 architecture, first implemented in the PA-8000 processor in 1996. PA-RISC processors and HP changed significantly during the 1990s, from design philosophy to production processes.

PA-RISC processors and chipsets for HP 9000 had been designed and fabricated by HP in its own plants and design labs for decades. From the foggy days of TTL and NMOS in the 1980s until the 64-bit PA-8200 processor in 1997, HP produced everything in house: Processors, chipsets and boards were designed and manufactured mainly in Fort Collins (Colorado), Palo Alto, and Cupertino.

Since the mid-90s, HP started to fall behind in CPU manufacturing processes – most chips were one (or more) process generations behind contemporary counterparts from other vendors. This was the result of huge investments other CPU producers poured into fabs and R&D, where HP could not keep up. The outcome was HP not being able to make more aggressive design choices while fabbing processors in its own plants.

After the PA-8200, HP looked for external fabs to implement its CPU designs and went to Intel, its partner in developing Itanium. Intel's advanced fabs made huge CPUs with very large on-chip L1 caches possible, breaking a long-standing HP tradition of no L1 on the CPU die but resulting in very high processor performance.

With PA-8700 HP moved to IBM for fabbing processors, resulting in the first PA-RISC processor on a Silicon-on-Insulator (SOI) process. The last dual-core PA-8800 and PA-8900 processors were supposedly also fabbed at IBM as the last members of the PA-RISC processor family.

PA-8000

HP PA-8000 were the first 64-bit RISC processors by HP implementing the new PA-RISC 2.0 architecture. Released in 1996 with a completely redesigned processor design, four-way superscalarity and strong out of order execution capabilities, the PA-8000 CPU core was re-used in all PA-8x00 series processors for almost a decade.

PA-RISC 2.0 PA-8000 were very fast 64-bit microprocessors in 1996, above the RISC competition for technical computing. They were faster than IBM PowerPC 604e (1996), Pentium Pro (1995), Pentium II (1997) and MIPS R10000 (1996) at similar clocks, and much stronger in floating point.

PA-8000 were almost par with Pentium II (1997) and UltraSPARC Iii (1997) sold at significantly higher clocks. They were more than 2x faster at the same clock than the 32-bit PA-7200 and PA-7300LC predecessors.

PA-8200

HP PA-8200 PA-RISC were again very fast 64-bit microprocessors in 1997, and above much of the RISC competition in technical computing. They were significantly faster than Pentium II (1997), UltraSPARC Iii (1997) and Digital Alpha 21164A (1996) that had twice the clockspeed.

Newer MIPS R10000 CPUs (1996/1997) with large caches were only slightly slower than PA-8200. PA-8200 in turn were a bit faster than the core 64-bit PA-8000, released a year earlier (1996) at lower frequencies.

PA-8500

HP PA-8500 PA-RISC were some of the fastest 64-bit microprocessors in 1998. They were significantly faster than Pentium II (1997), Pentium III (1999) and Digital Alpha 21264 (1998) at the same or higher clock speed. IBM POWER3 (1998) and UltraSPARC Ii (1997) were almost on par at the same clock. SGI MIPS R12000 (1998) was slower than PA-8500 and only sold at lower frequencies.

PA-8500 were shipped with higher clock speeds than earlier 64-bit PA-8200 (1997) and slightly faster in integer and significantly faster in floating point. Notably, PA-8500 won the Microprocessor Report's "Best RISC Processor" in 1999, "when it is destined for the scrap heap" due to Itanium arrival.

PA-8600

HP PA-8600 PA-RISC were fast 64-bit microprocessors of the early millenium (2000) and followed the PA-8500 performance-wise with improved frequencies. The PA-8600 were in the same ballpark as higher clocked UltraSPARC III (2001), Pentium III Xeon (1999) and faster than (slightly outdated) Digital Alpha 21264 (1998).

Performance was even with IBM RS64-VI (2000) and MIPS R14000 (2001) RISC processors at similar clock, while the newer Digital Alpha 21364 (2001) was faster at higher frequencies.

PA-8600 was notably faster than the first Itanium Merced (2001) from HP and Intel at higher clock-rates, which in turn were much stronger in floating point (50%).

PA-8700

HP PA-8700 was the last conventional PA-RISC 2.0 processor, before the move to dual-core PA-8800 and PA-8900. Released in 2001, PA-8700 were a stop-gap measure by HP while waiting for Itanium processor to ship – originally planned for 1999. As MPR put it, "HP is developing a processor called the PA-8700 to extend its current RISC line, tiding over customers until Merced systems are available."

HP PA-8700 PA-RISC were fast 64-bit CPUs in the early 2000s at a time when competitors started increasing clock speeds for more performance. PA-8700 were in the same ballpark as higher clocked UltraSPARC III (2001), Alpha 21364 (2001) and IBM POWER4+ (2003), faster than Pentium III Xeon (1999) and almost even with MIPS R14000 (2001).

The first Itanium Merced (2001) from HP and Intel was notably much slower than PA-8700 in integer but on par in floating point, while the second generation Itanium McKinley (2002) was faster with more than double the floating point performance.

PA-8800

When it became clear in the late-1990s that Itanium Merced processors will be significantly delayed until the early 2000s, HP decided to extend the life of PA-RISC by a few years. The plan by 1998 was to integrate two PA-8x00 64-bit cores onto a single processor with large caches: enter the PA-8800 and PA-8900 CPUs.

With this development, HP had the option to offer powerful PA-RISC processors in parallel to Itanium for “four years” to ease transition to the new IA64 architecture.

HP PA-8800 PA-RISC were last of the line of 64-bit PA-RISC processors, released in 2004. Their dual-core integration was the last PA-RISC evolutionary step to increase the performance of the original PA-8000 core. Few formal SPEC benchmark scores exist of PA-8800 and it was offered in only some niche mid-2000s PA-RISC systems.

PA-8800 was a very fast RISC processor when released in 2004 and possibly much faster at the same clockspeed than Alpha 21364 (2001), IBM POWER4+ (2003), Itanium McKinley (2002). It was in the same ballpark as AMD Athlon XP (2002), Intel Xeon DP (2003) and Pentium 4 Prescott (2003) at much higher (more than double) the frequencies.

PA-8900

HP PA-8900 PA-RISC were the pinnacle of 64-bit PA-RISC processor design (2005) and improved on the PA-8800 only slightly. No formal SPEC benchmark scores are known and PA-8900 were sold only as a slight upgrade to PA-8800-based 64-bit PA-RISC systems. This way, PA-RISC eked out a few more years on the HP lineup.

Based on PA-8800 performance figures, PA-8900 was possibly a pretty quick CPU for 2005, faster at the same clockspeed than Alpha 21364 (2001), IBM POWER4+ (2003) and Itanium McKinley (2002). Contemporaries such as AMD Athlon XP (2002) and Intel Xeon (2003) had similar performance at much higher frequencies, AMD Opteron (2005) was faster.

2.4.4 Performance and SPEC

The main competitors of PA-RISC were other Unix platform vendors with their own RISC architectures: Sun SPARC (Solaris), Digital Alpha (Tru64 and OSF), SGI with MIPS (Irix), and IBM POWER (AIX and others). In the late 1990s, Intel Pentium and P6-based successors also became serious competitors (Windows and Linux).

While PA-RISC processors were usually faster than their competition at the same clock speed, they were expensive to fabricate. Their platform, HP 9000 on PA-RISC and HP-UX, was usually exclusively priced in the 1980s and 1990s compared to other Unix vendor ecosystems.

Companies such as HP and IBM “can justify developing very-high-end processor designs, even though the unit volume will be small, because the profits per system are far higher than the profits per micro-processor chip,” as MPR put it in 1992.

PA-RISC was often used for specialized technical workloads that made use of their strengths in floating point and numerical processing, as part of an integrated HP 9000 and Unix ecosystem.

SPEC95 and SPEC2000 comparisons

Relative performance between computers and architectures can be compared by benchmark scores like the SPEC suite for scoring CPU and instruction performance. For the Unix and RISC systems covered here, SPEC95 and SPEC2000 had the greatest match, using the CPU integer (CINT) and floating point (CFP) results.

PA-RISC traditionally was a fast architecture compared to other RISCs. When others like Alpha and Intel P6 derivatives increased frequencies in the late 90s, PA-RISC stayed with comparatively lower clock

speeds. The following results are synthetic benchmarks dependant on compilers and operating systems, scores were notably higher in HP-UX 11.00 than in 10.20, for example.

Table 2.12: Typical SPEC scores of HP PA-RISC computers

Processor	Clock	Year	SPEC95int	SPEC95fp	SPEC2000int	SPEC2000fp
PA-7000	50 MHz	1991	1.20	2.00		
PA-7100	75 MHz	1992	1.53	2.46		
PA-7150	125 MHz	1992	3.97	4.61		
PA-7100LC	100 MHz	1994	3.76	4.06		
PA-7200	120 MHz	1995	6.06	8.14		
PA-7300LC	180 MHz	1996	9.22	9.43	87	60
PA-8000	180 MHz	1996	11.80	18.70		
PA-8200	200 MHz	1997	14.20	21.40		
PA-8500	440 MHz	1998	31.80	52.40	313	321
PA-8600	552 MHz	2000	42.10	64.00	432	433
PA-8700	750 MHz	2001	57.60	85.90	604	576
PA-8800	1 GHz	2004			1001	est.
PA-8900	1.1 GHz	2005				

Table 2.13: Typical SPEC scores of HP Itanium computers

Processor	Clock	Year	SPEC95int	SPEC95fp	SPEC2000int	SPEC2000fp
Itanium Merced	800 MHz	2001			365	610
Itanium McKinley	1.0 GHz	2002			807	1422
Itanium Madison	1.5 GHz	2003			1315	2106

Table 2.14: Comparison SPEC scores of other architectures

Processor	Clock	Year	SPEC95int	SPEC95fp	SPEC2000int	SPEC2000fp
Sun SuperSPARC	40 MHz	1992	1.13	1.38		
DEC Alpha 21064	100 MHz	1992	1.48	2.79		
Sun SuperSPARC II	75 MHz	1994	3.11	3.10		
IBM PowerPC 604	100 MHz	1992	3.59	3.20		
MIPS R5000	150 MHz	1996	3.97	4.20		
DEC Alpha 21064A	266 MHz	1993	4.18	6.27		
Intel Pentium	100 MHz	1994	4.04	2.35		
Intel Pentium Pro	166 MHz	1995	7.11	6.21		
DEC Alpha 21164	300 MHz	1998	7.33	12.20	161	158
IBM PowerPC 604e	166 MHz	1996	7.52	8.52		
MIPS R10000	196 MHz	1996	10.1	8.7		
Intel Pentium II	333 MHz	1997	13.0	9.4		
Sun UltraSPARC Ili	333 MHz	1997	14.1	18.3	133	126
Intel Pentium III	500 MHz	1999	20.7	14.7	231	191
MIPS R12000	400 MHz	1998	24.2	43.5?	320	319
DEC Alpha 21264	500 MHz	1998	27.3	57.7	311	382
MIPS R14000	600 MHz	2001			483	499
Sun UltraSPARC III	1 GHz	2001			511	688
IBM POWER4+	1 GHz	2003			617	862

DEC Alpha 21364	1 GHz	2001			689	975
AMD Athlon XP	2.2 GHz	2002			1080	873
Intel Xeon	2.8 GHz	2003			1249	1081
AMD Opteron 250	2.5 GHz	2004			1619	1652

SPEC92 comparisons

Table 2.15: Typical PA-RISC SPEC92 and SPEC89 scores* - approximate

Processor	Clock	Year	SPEC89	SPEC92int	SPEC92fp
NS-1	30 MHz	1987	9.5		
PRISM	18 MHz	1988	19		
PA-7000	50 MHz	1991	49	31	47
PA-7100	75 MHz	1992	107*	82	127
PA-7150	125 MHz	1992	182*	136	201
PA-7100LC	100 MHz	1994		117	144
PA-7200	120 MHz	1995		167	269
PA-7300LC	180 MHz	1996		200*	275*

Table 2.16: Based on old SPEC92 and SPEC95 archives* - unsure/unlikely

Processor	Clock	Year	SPEC89	SPEC92int	SPEC92fp
MIPS R2000	16MHz	1986	11.8	8.4	
DEC KA46 VAX	22MHz	1991	12	11.1	12.6
Motorola 68040	25MHz	1990	10.3	12.2	9.3
MIPS R3000	33MHz	1988	25	20.9	23.4
Motorola 88100	33MHz	1988	18	27.7	18.8
Intel 486DX2	66MHz	1992	25	35.8	16.1
IBM POWER	41MHz	1990	75	40.7	83.3
MIPS R4000	50MHz	1991	36	43.2	42.1
Sun SuperSPARC	40MHz	1992	71	50.2	60.2
DEC Alpha 21064	100MHz	1992	59*	74.6	95.2
Intel Pentium	75MHz	1993		89.1	68.5
PowerPC 604	100MHz	1994		128.0	120.2
DEC Alpha 21064A	266MHz	1993		198.6	262.5

Documentation

Most of the SPEC scores are from official SPEC results websites, now archived. Some scores are from vendor product pages, now also archived or lost.

- ◇ SPEC Benchmark CINT92 Summary, Netlib Performance Repository (2000)
- ◇ All of the SPECint95 Results Published by SPEC, Standard Performance Evaluation Corporation (2000)
- ◇ All of the SPECfp95 Results Published by SPEC, Standard Performance Evaluation Corporation (2000)
- ◇ SPEC CPU2000 Results, Standard Performance Evaluation Corporation (2006)

- SPECint2000
- SPECfp2000
- SPECint_rate2000
- SPECfp_rate2000
- ◇ SPEC CPU2000: Measuring CPU Performance in the New Millennium, Standard Performance Evaluation Corporation (2006, Reprinted from COMPUTER, July 2000)
- ◇ New Version of the SPEC test suite: CPU2000, Heise iX (5/2000)
- ◇ *Computer Makers Lead in High-End Processors*, Microprocessor Report (February 1992)
- ◇ INTEGRATED PA-7300LC POWERS HP MIDRANGE, MICROPROCESSOR REPORT (VOL.9 NO.15, 1995, HP reprint)
- ◇ HP SHOWS COMMITMENT TO HPC THROUGH PA-RISC ROADMAP, HPC Wire (November 1998)
- ◇ file of reported SPEC95 and SPEC92 CINT/CFP benchmark results (spectable,v), John DiMarco (December 2000, 5.208)

2.5 PA-RISC Chipsets

2.5.1 Overview

Most HP PA-RISC computers used proprietary HP chipsets and system designs. Early 32-bit workstations (HP 9000/700) and servers (HP 9000/800) from the 1990s used different chipsets. Later on, the system platforms of workstations and servers moved closer and used the same chipsets.

Table 2.17: Chipsets used in PA-RISC computers

Architecture and CPUs	Chips	Usage
Early designs	SIU/SPI	CPU bridge
<i>TS-1, NS-1, NS-2, PCX</i>	CTB	I/O bridge
ASP/Viper	Viper	Memory and I/O controller
<i>PA-7000, PA-7100</i>	ASP	I/O chipset
LASI	MIOC	Memory and I/O controller
<i>PA-7100LC, PA-7300LC</i>	LASI	I/O chipset
	Wax	EISA bridge
	Dino	PCI bridge
	Cujo	PCI-64 bridge
U2/UTurn	MMC/SMC	Memory controller
<i>PA-7200, PA-8000, PA-8200</i>	U2 or UTurn	I/O controller
	LASI	I/O chipset
	Wax	EISA bridge
	Dino	PCI bridge
	Cujo	PCI-64 bridge
Astro	Astro	Memory and I/O controller
<i>PA-8500, PA-8600, PA-8700</i>	Elroy	Bus bridge to I/O
Stretch	DEW	CPU bridge
<i>PA-8500, PA-8600, PA-8700</i>	Prelude	Memory controller
	IKE	I/O controller
	Elroy	PCI-64 bridge
Cell	CC	Memory and I/O controller
<i>PA-8700, PA-8800, PA-8900</i>	XBC	Crossbar
	SBA	I/O controller
	Elroy	PCI-64 bridge
zxi	Pluto	I/O and memory controller
<i>PA-8800, PA-8900</i>	Mercury	PCI, PCI-X, AGP bridge

Chipsets were tied to specific architectures but sometimes used in different generations of computers or implementations.

Early designs: Early 32-bit PA-RISC systems of the late 1980s used custom designs based on the SIU/SPI main bus interfaces and the SMB bus. The computing and I/O units consisted of a large number of individual chips and used CIO and HP-PB I/O buses.

ASP/Viper: Computers with 32-bit PA-7000 and PA-7100 processors mostly used the ASP chipset and Viper memory controller, with VSC CPU, GSC system and SGC and EISA expansion buses.

LASI: Developed as highly-integrated chipset and system design, many LC low-cost systems with PA-7100LC and PA-7300 LC processors used LASI and GSC as system and I/O bus.

U2/UTurn: PA-RISC computers based on 32-bit and 64-bit processors with a Runway processor interface used a U2 or UTurn system design that attached GSC- and PCI-based I/O and memory via adapters to the Runway bus.

Astro: Some PA-8500, PA-8600 and PA-8700 systems use a rope-based architecture with Astro as main system controller and Runway+ buses with I/O devices controlled by Elroy PCI bridges.

Stretch: Stretch was a 64-bit system design for midrange servers based on PA-8500 to 8700 processors, with a central system controller and links to processor and I/O controllers and PCI bridges. The main system bus is Itanium with converters for the PA-RISC processor Runway bus.

Cell: This was a crossbar chipset used in few HP 9000 Integrity servers and some Superdome models. The main design feature were individual system or processor “cells” that were interconnected by a CEC component and central crossbars.

zx1: The zx1 chipset was a HP Itanium chipset bus used in later HP 9000 and Integrity PA-RISC servers as well. It consists of two purpose-built main parts that connect the processor, memory and I/O to the Itanium system main buses: Pluto and Mercury.

2.5.2 Early designs

Early 32-bit HP RISC systems with 1980s PA-RISC processors TS-1, NS-1, NS-2 and PCX used custom HP system designs with SIU/SPI main bus interfaces and the SMB bus. Computing and I/O units in these HP PA-RISC systems consisted of many individual chips to form the central chipset and used CIO and HP-PB I/O buses.

The first PA-RISC I.O processors used external support chips to attach the CPU to memory and I/O. This functionality was later integrated into single chips and then moved to the CPU altogether.

- ◇ HP SIU or SPI system interface unit attaches the CPU to the SMB system main bus
- ◇ *NS-1 processors* Two cache controller units CCU₀ and CCU₁
- ◇ *NS-2 processors* Two CCUs cache controller units ICCU and DCCU
- ◇ *PCX processors* Three CMUX cache multiplexers
- ◇ Physical address space of 29-bit to support up to 512 MB main memory
- ◇ System Main Bus (SMB) is the central bus, to which CPU, memory and I/O buses attach with 64-bit at 25-30MHz.
- ◇ Memory is attached to the SMB main bus
- ◇ Central Bus or Midbus (CTB) attaches I/O via bus converters to SMB, 32-bit at maximum of 10 MHz
- ◇ CIO buses for I/O devices attach via adapters to CTB, 16-bit at 4 MHz, I/O expansion cards plug into CIO slots

Systems using these early designs, in various, slightly different variants:

- ◇ HP 9000 800 servers: 840, 825, 835, 850, 822, 832, 845, 855, 860, 842, 852, 865, 870.

2.5.3 ASP chipset

HP 9000 workstations and servers based on 32-bit PA-7000 and PA-7100 processors use the HP ASP chipset together with the HP Viper memory controller. Being an integrated chipset, ASP includes separate chips to provide the I/O subsystem and contains several modules from third-party vendors. Some HP 9000 800 servers use a partial implementation of ASP.

- ◇ VSC interface to system main bus, 32-bit, to the Viper memory controller
- ◇ GSC interface to main I/O bus, also sometimes called “SGC”
- ◇ NCR 53C700 8-bit Narrow single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller, and Intel 82501AD Ethernet transceiver, media auto-selection
- ◇ EISA bridge based on the Intel 82350 chipset
- ◇ Domain keyboard controller
- ◇ WD 16C552 parallel and NS 16550A compatible serial
- ◇ Intel 8042 microprocessor
- ◇ 512 KB EPROM Boot ROM, 8 KB EEPROM for storing system configuration status etc.
- ◇ 25-33 MHz chipset clock frequency on a 160-pin QFP chip

There are two variants of HP ASP for workstations: HP Coral or “Cobra I/O subsystem” is the original ASP, while HP “Hardball” is the second version ASP₂, an improved design with fast/wide SCSI and FDDI networking used in HP 9000 735 and 755 workstations:

- ◇ NCR 53C720 16-bit Fast-Wide differential SCSI-2
- ◇ AMD Formac Plus Am79C830 FDDI controller
- ◇ Stereo/CD quality audio
- ◇ Two 32-bit device data buses, a variant of GSC bus: one attaches to LAN and FDDI, the other to two SCSI controllers, audio and other I/O devices
- ◇ ASP₂ consists of two separate chips: Shortstop, main bus and memory interface, and Cutoff, the main address controller

Viper

HP Viper is the memory and I/O controller (MIOC) on HP computers with 32-bit PA-7000 and PA-7100 PA-RISC processors. Viper is similar on both platforms and sometimes counted into the HP ASP chipset, in which it was always used as memory and I/O controller.

Viper, also called memory and system bus controller (MSEC), handles all memory and I/O traffic between processor and the rest of the system.

- ◇ Viper attaches with 32-bit multiplexed address/data bus PBus to the CPU
- ◇ Memory attaches directly to Viper, with multiplexed 64-bit ECC
- ◇ VSC system main bus attaches to Viper, 32-bit on PA-7000, 64-bit on PA-7100
- ◇ I/O attaches with bus adapters to VSC bus

- ◇ Viper is also called MIOC, PMI or PIC
- ◇ On SMP systems either each CPU has its own MIOC which share a SMB bus and memory, or two CPUs share one MIOC
- ◇ Original design (MSBC): 9,5×9,5 mm die, 185,000 FETs, 0.8μ, CMOS26B in 272-pin CPGA
- ◇ Newer design: 0.8μ, CMOS26B in 408-pin PGA
- ◇ SBI system bus interface: two 100-pin QFP chips
- ◇ Low-cost version on the 705/710 workstations: two separate chips, each 7,0×7,0 mm die, 1.0μ, two-layer metal CMOS34 in 160-pin QFP

Used in

- ◇ HP 9000 705, 710, 715, 725, 720, 730, 750, 735, 755, 742i, 745i, 747i workstations
- ◇ HP 9000 Nova servers (F, G, H, I-Class)
- ◇ HP 9000 890, T500, T520 mainframes
- ◇ Mitsubishi ME/R7200, ME/S7200, ME/R7300, ME/S7300, ME/R7500, ME/S7500 workstations
- ◇ Hitachi 3050RX 220, 230, 310S, 320, 330, 430, 440, 9000V V735/125, VT500 workstations

Documentation

- ◇ Hardball I/O Subsystem, External Reference Specification (.pdf), Hewlett-Packard Company (September 1991, Version 1.1)
- ◇ High Performance PA-RISC Snakes Motherboard I/O , Hewlett-Packard 1993, **bitsavers**
- ◇ Hewlett-Packard Journal December 1992
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- ◇ Hewlett-Packard Journal August 1992
 - *Midrange PA-RISC Workstations with Price/Performance Leadership*, page 6 (Andrew J. DeBaets and Kathleen M. Wheeler)
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 - *Mechanical Design of the HP 9000 Models 720 and 730 Workstations*, page 43 (Arlen L. Roesner and John P. Hoppal)
 - *Meeting Manufacturing Challenges for PA-RISC Workstations*, page 49 (Spencer M. Ure et al.)

2.5.4 LASI chipset

HP PA-RISC PA-7100LC and PA-7300LC 32-bit systems use HP LASI, a highly integrated HP chipset, which combines many functions and I/O on a single chip, together with their on-CPU MIOC memory controller for a very integrated system design.

HP LASI was primarily designed for cost-reduction while still providing most I/O functions. It was used as the main controller in most PA-7100LC and PA-7300LC systems, while later 64-bit PA-8x00 systems used LASI for complementary I/O functions.

Primary cost reductions were achieved by integrating major I/O subsystems into a single chip, like LAN and SCSI from Intel and NCR, respectively. Some I/O systems were designed specifically for LASI. Furthermore, for integration the PA-7100LC and PA-7300LC CPUs integrate the external memory and I/O controller MIOC onto the processor with memory and cache directly attaching to it.

Details

- ◇ GSC bus interface
- ◇ Integrated Intel i82C596CA 10 Mbit Ethernet
- ◇ Integrated NCR 53C710 Fast-Narrow SE SCSI-2
- ◇ NS16550A compatible RS232
- ◇ WD16C522 compatible parallel
- ◇ PS/2 controllers
- ◇ *Harmony* CD-quality 16-bit sound
- ◇ PS/2 style keyboard and mouse devices
- ◇ 8-bit bus to connect flash EPROMs and FDD
- ◇ Bus arbitration, Interrupt controller, Real-Time clock, PLL generator for the whole I/O subsystem
- ◇ 13.2×12.0 mm die, 520,000 FETs, 0.8μ, CMOS26B in 240-pin MQUAD, 3W at 40 MHz

System design

A typical system design with one of the 32-bit LC “Low Cost” processors PA-7100LC and PA-7300LC with GSC main system bus would look like this:

1. MIOC, main memory and I/O controller, directly integrated on the CPU
 - ◇ Execution units and internal caches attach on-chip to the MIOC
 - ◇ External cache and memory attach to MIOC
2. GSC, system main bus, attaches to MIOC and I/O controllers
 - ◇ Attaches via 32-bit
 - ◇ PA-7300LC systems use extended GSC+
3. I/O adapters attach to GSC
 - ◇ LASI chipset

- ◇ Some video adapters directly attach to GSC
- ◇ I/O slots extend GSC
- ◇ Bus adapters, including EISA, VME and PCI, attach to GSC

2.5.5 Wax

HP Wax is a secondary I/O controller complimentary to the HP LASI chipset. It implements various secondary I/O functions and acts as a I/O bus to GSC adapter for different external buses as EISA, HP-HIL and HP-IB. Most systems use Wax to complement LASI with other required I/O functions that were previously implemented in diverse I/O ASICs. It is implemented in the same process and package as LASI.

- ◇ GSC bus interface with GSC+ features
- ◇ EISA bus converter, interfaces to external EISA controller: TI TACT84500
- ◇ Serial interface — NS16550A compatible RS232
- ◇ HP-HIL interface, compatible to previously separate HP HIL chip used in older workstations
- ◇ HPIB interface for instrumentation devices, needs three external chips
- ◇ Interrupt control, Timers
- ◇ 0.8 μ CMOS26B packaged in 240-pin MQUAD

Used in

- ◇ HP 9000 712, 715, 725, 743i, 745, 744, 748i workstations
- ◇ HP 9000 A180, A180C servers
- ◇ HP Visualize B132L, B132L+, B160L, B180L+
- ◇ C100, C110, C132L, C160L, C160, C180, C200, C240, C360 workstations
- ◇ HP 9000 D-Class servers
- ◇ HP 9000 E25, E35, E45, E55 servers
- ◇ HP Visualize J200, J210, J210XC, J280, J282, J2240 workstations
- ◇ HP 9000 K-Class servers
- ◇ RDI PrecisionBook 132, 160, 180 laptops
- ◇ HP 9000 R380, R390 servers
- ◇ SAIC Galaxy 1100 portables
- ◇ HP Agilent 16600A, 16700A, 16700B, 16702A and 16702B series logic analyzers

Documentation

1. 712 I/O Subsystem ERS (External Reference Specification) — “LASI ERS” Hewlett-Packard Company (February 1993, Revision 1.1) **parisc linux**

2. An I/O System on a Chip (LASI) (PDF, HP Journal 4/95)
3. External Reference Specification (ERS) for the Wax I/O ASIC Hewlett-Packard Company (May 1993, version 1.0 redacted) **parisc linux**

2.5.6 U2 and UTurn chipset

HP U2 and UTurn are chipsets used in HP PA-RISC workstations and computers. PA-RISC computers with 32-bit and 64-bit processors with Runway bus often used U2 and UTurn. U2 and UTurn are I/O adapters (IOA) and MMC/SMC their memory controllers that attach subsystems to the main Runway processor bus.

HP UTurn and U2 attach the GSC main system bus with devices and I/O via Runway bus to the CPUs. This setup allowed HP to use a standard frontend with UTurn in different PA-RISC system designs with different backends to support memory or I/O technologies.

U2 is the variant for 32-bit PA-7200 PA-RISC systems while later systems with 64-bit PA-8000 and PA-8200 processors use the UTurn follow-on.

- ◇ Runway bus interface to CPU/memory bus, 64-bit wide, 120 MHz, 960 MB/s peak bandwidth
- ◇ U2: Two GSC+/HSC I/O buses, peak bandwidth between 128 MB/s to 160 MB/s each
- ◇ UTurn: Two GSC-2 I/O buses, peak bandwidth 256 MB/s each
- ◇ Support for various frequencies on both sides on Runway and GSC
- ◇ Address translation from 32-bit GSC to 40-bit Runway addresses
- ◇ Interface to processor dependent hardware PDH on IOA A
- ◇ Hardware cache coherent I/O
- ◇ Real-time clock
- ◇ U2 is a 432-pin PGA chip, chip numbers: 1MM6-0004

A typical U2/UTurn system design and bus setup would look the following:

- ◇ Runway is the main processor and memory bus for 1-4 CPUs at 64-bit
- ◇ HP MMC is the main memory controller which attaches to Runway at 64-bit
 - Memory attaches to MMC via slave Memory Controllers SMC and Data Multiplexers, 128-bit 60 MHz data and 39-bit 60 MHz address buses
- ◇ HP U2/UTurn I/O adapters attach the system bus to the Runway processor bus at 64-bit
- ◇ GSC+, the main system bus, attach to the U2/UTurn IOAs at 32-bit
- ◇ I/O adapters and slots attach to GSC+
 - LASI chipset
 - Video adapters
 - I/O slots extend GSC
 - Bus adapters, including EISA, VME and PCI, attach to GSC+

Used in

- ◇ HP Visualize C100, C110 (U2) C160, C180 (UTurn), C200, C240, C360 (UTurn) workstations
- ◇ HP 9000 D-Class and R-Class servers
- ◇ J200, J210, J210XC (U2), HP Visualize J280, J282, J2240 (UTurn) workstations

- ◇ HP 9000 K-Class servers

MMC/SMC

Most systems with 64-bit PA-7200, PA-8000 or PA-8200 processors use a combination of HP MMC and SMC memory controllers to attach the main system memory to the Runway processor bus. I/O is controlled by the HP U2/UTurn I/O adapters on the same Runway bus.

- ◇ Master Memory Controller MMC attaches with 64-bit to the Runway processor bus and 128-bit to the memory, 960 MB/s data rate
- ◇ Up to eight Slave Memory Controllers SMCs attach to one MMC on its memory address bus. The SMCs carry the functionality to interface with specific types of DRAM.
- ◇ Data Multiplexers DMs attach the 128-bit 60 MHz data bus of the MMC to memory banks. Each two sets of memory connect with two 64-bit 30 MHz buses to the DMs.
- ◇ Physical address space of 36-bit for 32 GB main memory
- ◇ Memory address bus is shared between all SMCs of a MMC, 39-bit at 60 MHz
- ◇ Memory data bus attaches to the DMs and memory

Used in

- ◇ HP Visualize C100, C110C160, C180, C200, C240, C360 workstations
- ◇ HP 9000 D-Class servers
- ◇ HP Visualize J200, J210, J210XC, J280, J282, J2240 workstations
- ◇ HP 9000 K-Class servers

Dino/Cujo

HP Dino is the GSC to PCI bridge found in many older PCI PA-RISC workstations. This way, GSC and PCI buses did not need to be synchronized, simplifying the system design. Dino also implements a small set of I/O functions for the system. HP Cujo is a Dino bridge for 64-bit PCI.

- ◇ GSC bus interface with GSC+ feature, >40 MHz
- ◇ PCI bus interface (PCI64 on Cujo), >33 MHz
- ◇ Two PS/2 interfaces, RS-232 port
- ◇ Mapping register with 8 MB resolution
- ◇ Integrated PCI arbitration
- ◇ Integrated interrupt register
- ◇ Supports both 3.3 V and 5.0 V PCI operation

Used in

- ◇ HP 9000 743i, 745, 744, 748i VME workstations
- ◇ HP 9000 A180, A180C servers
- ◇ HP Visualize C100, C110C160, C180, C200, C240, C360 workstations
- ◇ HP 9000 D-Class and R-Class servers
- ◇ HP Visualize J200, J210, J210XC, J280, J282, J2240 workstations
- ◇ HP 9000 K-Class servers
- ◇ HP Agilent 16600A, 16700A, 16700B, 16702A and 16702B series logic analyzers

Documentation

- ◇ Visualize J200, J210 technical reference manual (URL gone)
- ◇ Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- ◇ A New Memory System Design for Commercial and Technical Computing Products (.pdf) Thomas R. Hotchkiss, Norman D. Marschke, and Richard M. McClosky (February 1996: Hewlett-Packard Journal)
- ◇ DINO ERS (External Reference Specification)—A GSC-to-PCI Bridge Hewlett-Packard Company (February 1997, Revision 3.0) **parisc linux**
- ◇ Dino 3.1 (1FC3-0004) Errata Listing Hewlett-Packard Company (September 1997) **parisc linux**

2.5.7 Astro chipset

HP Astro is a chipset for HP 64-bit PA-RISC computers, mostly used in HP Visualize workstations. It was used in PA-8500, PA-8600 and PA-8700 PA-RISC systems with “rope”-based architecture, which used Astro as main system controller and IOMMU with Runway+/Runway DDR buses and I/O devices controlled by HP Elroy PCI bridges.

Astro is the main memory and I/O controller which attaches to Runway:

- ◇ Memory attaches to Astro with a peak data rate of about 2.0 GB/s at 125 MHz
- ◇ Up to eight I/O links (ropes) with each 250 MB/s attach to Astro.
- ◇ Astro supports 120/125 MHz SDRAMs for a maximum supported memory of 40 GB
- ◇ 16-entry fully associative I/O TLB
- ◇ 16-entry fully associative coherent I/O buffer cache

Astro bus attachments:

- ◇ Runway+/Runway DDR is the main processor and memory bus: one to four CPUs attach to Runway with 64-bit, parity-protected.
- ◇ HP Elroy I/O adapters attach PCI bridges via the I/O ropes to Astro: One or two ropes per Elroy PCI bridge, then PCI slots or devices attach to Elroy bridges
- ◇ PCI buses attach to the multiple Elroy bridges, in 33 or 66 MHz, 32 or 64-bit variants. I/O devices, adapters and slots attach to PCI
- ◇ HP Pluto is the successor of Astro for Itanium-2 processors and buses; it works very similar.

Elroy

HP Elroy is a PCI bus bridge that attaches one PCI bus to one or more I/O ropes, used in HP PA-RISC computers. Elroy was often used with the HP Astro memory and I/O controller.

- ◇ Peak bandwidth of up to 500 MB/s
- ◇ Multiple Elroys can be used in a single system
- ◇ Support for *Turbo* and *Twin Turbo* slots—attached via one or two links respectively
- ◇ Support for PCI 2.1, 1X, 2X and 4X bus
- ◇ PCI data width of 32 or 64 bit
- ◇ PCI clock of 33 or 66 MHz

Used in

- ◇ HP 9000 A400 (rp2400, rp2430), rp2405, A500 (rp2450, rp2470) servers
- ◇ HP Visualize B1000, B2000, B2600 workstations
- ◇ HP Visualize C3000, C3600, C3650, C3700, C3750 workstations
- ◇ HP Visualize J5000, J5600, J6000, J6700, J7000, J7600 workstations

- ◇ HP 9000 L1000 (rp5400), L2000 (rp5450), L1500 (rp5430), L3000 (rp5470) servers
- ◇ Elroy: HP 9000 N4000 (rp7400), HP 9000 N4000 (rp7405, rp7410) servers

Documentation

1. Astro External Reference Specification Introduction
 - Astro External Reference Specification Error Handling
 - Astro External Reference Specification R2I Operations
 - Astro External Reference Specification Register Map
 - Astro External Reference Specification Runway Interface
 - Astro External Reference Specification Memory Map
 - Hewlett-Packard Company (February 2000, Revision 1.2) **parisc linux**
2. Elroy ERS (External Reference Specification) — Ropes to PCI Bridge Chip Hewlett-Packard Company (January 2000, Revision A (1.4) **parisc linux**

2.5.8 Stretch chipset

HP Stretch was a 64-bit HP PA-RISC system design for midrange servers based on PA-8500 to 8700 processors, a complicated setup with a central system controller and “links” to processor and I/O controllers and PCI bridges. The main system bus is an HP Itanium bus, with converters for the processor Runway+/Runway DDR buses. There are four main components, and the following buses used:

- ◇ HP Prelude memory controller connects the main memory to two system buses.
- ◇ HP DEW Runway ports/converters convert the system buses into Runway buses for the PA-8500 and upwards CPUs—two CPUs share one DEW.
- ◇ HP IKE I/O controllers attach PCI bridges via I/O links to the system bus.
- ◇ HP Elroy PCI bridges convert the I/O channels from IKE I/O controllers into PCI buses

Prelude

HP Prelude is the memory controller of PA-RISC systems with Stretch chipset and connects up to 16 pairs of SDRAM memory via four memory buses to two system buses. The main buses are HP Itanium buses, in preparation of the early 2000s HP shift from PA-RISC to Itanium.

Prelude consists of three VLSI chips: one address controller and two data controllers; each data controller drives two multiplexed 64-bit memory buses:

- ◇ Two system buses, each 2.1 GB/s peak with 4.3 GB/s aggregate
- ◇ Up to four memory buses, each 2.1 GB/s peak with 8.6 GB/s aggregate to the memory
- ◇ Both memory and system buses are Itanium/Merced buses at 133 MHz DDR with 64-bit width, ECC-protected
- ◇ System main buses connect to the CPU bridges (DEW) and I/O controllers (IKE)

DEW

HP DEW is the Runway CPU bridge for 64-bit PA-RISC systems using the HP Stretch chipset. It attaches the Runway-based PA-8500, PA-8600 and PA-8700 PA-RISC processors to Itanium ed system man buses. Each pair of CPUs share one DEW port converter. Common configurations include one to four DEWs for up to eight processors.

- ◇ CPU side: Runway+/Runway DDR processor bus for up to two PA-8x00 processors with peak bandwidth of 2.1 GB/s
- ◇ System side: Itanium system bus at 133 MHz, with 2.1 GB/s peak

IKE

HP IKE is the I/O controller on 64-bit PA-RISC systems with HP Stretch chipset. IKE is the central memory controller that provides one or two system buses, to which CPUs and I/O attach. Each system bus has one IKE I/O controller that connects to several I/O controllers (Elroy bridges), which in turn provide PCI buses.

The connection between IKE and each slave I/O controller is one or two 12-byte wide I/O links (I/O ropes), which can be combined into twin I/O channels for so-called *Twin-Turbo* PCI slots/buses.

- ◇ System side connects to system main bus, a Itanium bus at 133 MHz, with 2.1 GB/s peak
- ◇ I/O side attaches to up to twelve 12-byte wide 266 MB/s I/O links
- ◇ Each PCI slot has its own PCI controller and bus
- ◇ HP Elroy PCI bridges convert the I/O channels into PCI buses

Used in

The HP Stretch chipset was used only in few HP PA-RISC systems of the early 2000s.

- ◇ HP 9000 L1500 (rp5430), L3000 (rp5470) servers
- ◇ HP 9000 N4000 (rp7400) servers

Documentation

- ◇ hp server rp7400 whitepaper (URL gone)
- ◇ hp server rp5400 series entry-level UNIX servers technical whitepaper (URL gone)

2.5.9 Cell chipset

HP Cell is a crossbar chipset used in 64-bit HP PA-RISC Integrity servers and some HP Superdome mainframe computers. The central component, *Central Electronics Complex* (CEC), interconnects individual system and processor “cells” via central crossbars. Cell boards were seated in the backplane of the systems for cell-to-cell links and I/O functionality.

The HP **Cell Controller** (CC) is the central chipset at the core of each cell. It connects local processors and memory on cells to the SBA I/O links and the XBC crossbar. XBC is the crossbar ASIC that provides the main backplane function, each backplane supports up to two four cell modules. Different backplanes can be tied together through links through the XBCs with a high-bandwidth, low/latency connection.

M2 are the main HP Cell memory controllers and converters on each cell board. There are eight M2 controllers that attach in two banks to each CC. Requests and addresses are sent directly from CC to memory, with data returning through M2s.

RIO is the master I/O controller for HP Cell, also called SBA. The central I/O part of the main chipset, with one SBA reserved for each cell/CC, located on the (I/O) backplane. Each SBA provides sixteen 12-bit links called ropes to which slave I/O controllers connect, the LBAs. These LBAs are Elroy PCI bridges that convert the links from the SBA into PCI buses.

Core I/O is a card set that provides standard I/O functions and plugs into PCI-64 or special slots to provide third-party I/O functions. Distinct cards were available: MP/SCSI card and LAN/SCSI, among others.

- ◇ Two dual-channel Symbios Logic 53C1010 Ultra160 SCSI controllers
- ◇ Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- ◇ Gigabit Ethernet networking
- ◇ Console, serial and management controllers
- ◇ Fast-Ethernet DEC 21142/43 for Management LAN
- ◇ Optional second Core I/O card for redundancy or partitioning

Several buses were used in Cell: Runway+ processor bus for up to four processors at 8.0 GB/s. Memory bus to the M2, for up to two memory “banks” with 4.0 GB/s peak The SBA I/O links to the off-cell SBA have 2.0 GB/s peak, the XBC link to the crossbar for cell-to-cell communication 8.0 GB/s peak.

Used in

- ◇ N4000 (rp7405, rp7410)
- ◇ Superdome

Documentation

- ◇ hp server rp7410 whitepaper (URL gone)
- ◇ HP nPartition-capable Servers (URL gone)
- ◇ User Guide hp rp7405/7410 Servers (URL gone)

2.5.10 HP Itanium zxt chipset

HP Itanium zxt is a chipset designed for HP Itanium computers in the early 2000s. It was used by HP also in later 64-bit HP 9000 and Integrity PA-RISC servers, with some adaptations for Itanium and PA-RISC buses. HP zxt consists of two custom main parts that connect CPUs, memory and I/O to the Itanium system main buses: Pluto and Mercury.

- ◇ HP Pluto zxt memory and I/O controller (MIO) – main chipset controller

- Processor bus
- Two independent memory buses
- I/O channels (I/O ropes)

Pluto also contains memory and cache controllers. Part of the memory subsystems are sometimes the zxt SMEs scalable memory expanders that increase memory capacity and data rate through multiplexing

- ◇ HP Mercury zxt I/O adapters (IOAs) connect PCI-X/AGP slots and I/O devices to Pluto

The rest of the I/O chipset is made up of standard third-party components such as SCSI controllers, Ethernet.

Pluto

Many Itanium and PA-RISC workstations and servers use the HP Pluto memory and I/O controller (MIO) as part of the zxt chipset. Pluto is based on the Astro IOMMU, extending it for Itanium-2 processors and bus interfaces, DDR memory and faster I/O links.

- ◇ Processor bus: Itanium-2 processor bus for up to four CPUs, maximum of 200 MHz bus with 128-bits for up to 6.4 GB/s data rate.
- ◇ Two memory buses with peak 8.0 GB/s at maximum clock of 266 MHz DDR.
- ◇ I/O system based on eight separate 500 MB/s I/O links for individual PCI, PCI-X or AGP bridges. Peak aggregate I/O bandwidth is 3.2 GB/s
- ◇ Support for DDR SDRAMs
- ◇ Maximum supported memory of 16 GB to 64 GB with SME memory extender
- ◇ 16-entry I/O TLB
- ◇ 16-entry coherent I/O cache

Mercury

HP Mercury is a PCI/AGP bridge for PA-RISC and Itanium systems based on an I/O ropes architecture. It is part of the zxt chipset used on Itanium systems, based on the Elroy PCI bridge, extending it for AGP devices and faster I/O ropes. Most systems use several Mercury chips to attach PCI/AGP buses to the multiple I/O ropes. Each Mercury attaches one PCI or AGP bus to up to four 500 MB/s I/O ropes.

Mercury is often used together with the Pluto I/O and memory controller.

- ◇ Attaches to one to four (bundled) I/O ropes

- ◇ Provides one PCI, PCI-X or AGP 2.0 bus
- ◇ Multiple Mercurys can be used in a single system
- ◇ Support for PCI 2.1, also some support for PCI 2.2
- ◇ Support for PCI-X
- ◇ Support for AGP 1X, 4X and 8X
- ◇ PCI data width of 32 or 64 bit
- ◇ PCI clock of 33 or 66 MHz
- ◇ PCI-X clock of up to 133 MHz
- ◇ Up to six PCI slots
- ◇ No support for 5 V PCI

Used in

- ◇ HP Integrity rp3410, rp3440, rp4410, rp4440, rp7420 servers
- ◇ HP Integrity rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640 servers
- ◇ HP Superdome mainframes
- ◇ HP zx2000, zx6000 workstations

Documentation

- ◇ zXI mio (Memory and I/O) External Reference Specification Hewlett-Packard Company (March 2003, Revision 1.0) **parisc linux**
- ◇ HP zXI ioa ERS External Reference Specification Ropes to AGP/PCI/PCI-X Bridge (.pdf) Hewlett-Packard Company (April 2003, Revision 3.2) **parisc linux**

2.6 PA-RISC Buses

2.6.1 Overview

Many different buses and bus systems were used in PA-RISC computers. Some were custom HP designs, especially the system main buses and early I/O buses such as VSC and GSC. For I/O devices HP used some custom designs as well but made use of industry buses such as EISA, PCI and others soon.

Table 2.18: Buses used in PA-RISC computers overview

Type	Frequencymax	Width	Data rate max	Usage
System buses				
GSC	40 MHz	32-bit	160 MB/s	System bus and I/O
HSC/GSC+	40 MHz	32-bit	160 MB/s	System bus and I/O
GSC-2	40 MHz?	32-bit	256 MB/s	System bus and I/O
VSC	60 MHz	32-bit/64-bit	240 MB/s/480 MB/s	System bus
SMB	30 MHz	64-bit	?	System bus
CPU buses				
PBus	66 MHz?	64-bit	?	CPU
Runway	120 MHz	64-bit	960 MB/s	CPU
Runway+	125 MHz	64-bit	2 GB/s	CPU
Device and I/O buses				
EISA	8.3 MHz	32-bit	33 MB/s	I/O bus
SGC	25 MHz?	32-bit	100 MB/s	I/O bus
HP-PB	8 MHz	32-bit	32 MB/s	I/O bus
PCI-32	66 MHz	32-bit	266 MB/s	I/O bus
PCI-64	66 MHz	64-bit	533 MB/s	I/O bus
PCI-X	133 MHz	64-bit	1066 MB/s	I/O bus

2.6.2 GSC

The General System Connect GSC bus is the primary system and I/O bus on most of second-generation 32-bit HP 9000 workstations. GSC connects most of the I/O devices to the central system bus and chipset, with some CPUs attaching directly to it like the PA-7100LC and PA-7300LC HSC is a variant of GSC.

- ◇ 32-bit data path width
- ◇ Multiplexed address and data
- ◇ Transfer rates of up to 142-256 MB/s, depending on bus variant
- ◇ 5 V signalling voltage
- ◇ **Original GSC**, GSC-1X, with maximum clock of 40 MHz and peak data rate of 160 MB/s, used on most of the early GSC systems, mostly together with LASI as main I/O controller
- ◇ **GSC+/HSC**, Extended GSC, with a maximum clock of 40 MHz and peak data rates of 160 MB/s, 132 MB/s with 33 MHz, 144 MB/s with 36 MHz
- ◇ GSC-1.5X with additional extended write operations

- ◇ GSC-2 or GSC-2X, with a peak data rate of 256 MB/s on 64-bit systems with the UTurn I/O bridge to Runway

Expansion cards form factors

- ◇ GSC in EISA-formfactor can be GSC-1X and GSC-2X, also probably GSC-1.5X and has a 100-pin female EBBI card connector
- ◇ GIO is GSC-1X, limited to the 712 workstation with 80-pin female EBBI card connector
- ◇ HSC (High-speed System Connect) is GSC+ and used on several server systems like D-Class and K-Class. HSC are identical to GSC-M cards except different bulkhead and use 100-pin male pin and socket with groundplane.
- ◇ GSC-M “Mezzanine” is GSC-1X and used in PA-RISC VME computers. Have 100-pin male pin and socket with groundplane and are identical to HSC cards except different bulkhead

2.6.3 VSC

Viper System Connect (VSC) is the central system bus of computers with PA-7000 and PA-7100 PA-RISC processors. It connects the HP Viper central bus controller, also known as MIOC, PMI or PIC, to the memory and I/O buses. In multiprocessor configurations, each processor has its own Viper controller, which connects to a shared VSC bus with attachments to all Viper controllers, memory and I/O converters.

- ◇ 32-bit data path width on PA-7000 systems
- ◇ 64-bit data path width on PA-7100 systems
- ◇ 128-bit data path width possible, apparently only implemented in T500 servers
- ◇ Synchronous pipelined bus
- ◇ Separate data and address buses
- ◇ Memory data blocks are transferred in 16, 32 or 64 Byte blocks
- ◇ Provides cache and TLB coherency on multi-processor configurations, snoopy bus
- ◇ Various clock speeds were supported, 2/3 processor clock was common
- ◇ Maximum data rate depends on clock speed and bus width, with a common configuration of 60 MHz and 64-bit: 480 MB/s
- ◇ Apparently 3.0V signalling voltage

VSC is sometimes called SGC, the extension of VSC to graphics cards.

2.6.4 System Main Bus (SMB)

In early 1980s PA-RISC 1.0 systems, NS-1, NS-2 and PCX processors attach to the System Main Bus (SMB) via bus converters.

- ◇ 64-bit data width
- ◇ Clockspeed of maximum 25-30 MHz

- ◇ Central system bus between CPU/bus adapter, memory and I/O buses

TS-1, the first PA-RISC processor used a simpler version of this setup and directly attached the CPU to the Central Bus CTB with 32-bit at 8 MHz. Here, all the CPU, memory and I/O devices directly connect to the CTB.

2.6.5 PBus

Systems with PA-7000 or PA-7100/PA-7150 processors use the PBus processor bus between the CPU and external memory controller Viper. These systems with VSC main bus mostly use ASP chipsets for system I/O and devices. On multi-processor systems with a PA-7100 two attachment variants are possible—either shared memory controller on two processors or shared system bus with up to eight processors.

- ◇ 32-bit multiplexed address/data bus
- ◇ Runs at fixed fractions of CPU clock, 1.0, .67 and .50 of processor speed
- ◇ Two multiprocessor strategies supported on the PA-7100

CPU attachment

1. PBus is the main processor and memory bus
 - ◇ CPU attaches to PBus with 32-bit, with ECC 40-bit
2. Viper, the main memory and I/O controller attaches to PBus
 - ◇ Memory attaches to MIOC via 64-bit, with ECC 72-bit
3. VSC, the system main bus, attaches to MIOC and various I/O controllers
 - ◇ Attaches via 32-bit on PA-7000 or 64-bit on PA-7100 at MIOC
4. I/O adapters attach to VSC
 - ◇ Either ASP chipset for SGC or GSC bus systems, or HP-PB adapters for some servers

Multiprocessor attachment

1. Two-way SMP “Low Cost”: Two CPUs share a PBus and attach to the same MIOC. Memory attaches directly to MIOC, I/O attaches via VSC to MIOC.
2. Scalable MP: Each CPU has its own MIOC. All MIOCs in the system share a VSC bus, to which I/O and memory attach.

2.6.6 Runway

Runway is the system bus of newer 64-bit systems with PA-7200 and PA-8000 processors and up. It is a synchronous, split-transaction bus. PA-8500, PA-8600 and PA-8700 use an advanced version of Runway, Runway+/Runway DDR.

- ◇ 64-bit multiplexed address/data bus
- ◇ Supports cache coherency and parity protection on address/data and control signal

- ◇ Each attached device contains its own arbitrator logic
- ◇ Split transactions, up to six transactions can be pending at once
- ◇ Snooping cache coherency protocol
- ◇ 1-4 processors “glueless” multi-processing with no support chips needed
- ◇ 768 MB/s sustainable throughput, peak 960 MB/s at 120 MHz
- ◇ Three frequency options of 1.0, 0.75 and 0.67 of CPU clock
- ◇ Runway+/Runway DDR: On PA-8500, PA-8600 and PA-8700, the bus operates in DDR *double data rate*, peak data rate 2.0 GB/s

CPU attachment

Systems with PA-7200, PA-8000 and PA-8200 processors use Runway and split I/O and memory controllers—with “frontends” and “backends” to interface the CPU and its processor bus to customized bus attachments. This allowed HP to use the frontend parts of these chipsets with a variety of different system design which only required modified backend parts for new memory or I/O technologies.

1. **Runway** is the main processor and memory bus for one to four processors, 64-bit, parity-protected
2. **MMC** is the master memory controller which attaches to Runway with 64-bit (at 120 MHz at a data rate of 960 MB/s). Memory attaches to MMC via slave memory controllers (SMC) at 128-bit 60 MHz data ECC and 39-bit 60 MHz address buses
3. **U2/UTurn I/O adapters** attach the main I/O bus and system to the Runway processor bus with 64-bit. Two I/O adapters (IOAs) per U2/UTurn chip with data rate depends on Runway clock with 120 MHz and 64-bit: 960 MB/s
4. **GSC+**, the main system bus, attaches to the U2/UTurn IOAs via 32-bit at a fraction of Runway/IOA clock, mostly 40 MHz.
5. I/O adapters and slots attach to GSC+, like LASI chipset, video adapters, I/O slots and bus adapters, including EISA, VME and PCI

Runway+ DDR CPU attachments

PA-RISC 64-bit processors PA-8500, PA-8600, PA-8700 use a Runway bus with increased data rate and different I/O and memory controllers, often Astro chipset.

1. **Runway+/Runway DDR** is the main processor and memory bus for one to four processors, 64-bit, parity-protected
2. **Astro** is the main memory and I/O controller which attaches to Runway
 - ◇ Attaches to Runway+/Runway DDR with 64-bit at 125 MHz with 2.0 GB/s
 - ◇ Memory attaches to Astro with a peak data rate of 2.0 GB/s at 125 MHz
 - ◇ Up to eight I/O links or ropes with each 250 MB/s attach to Astro
3. **Elroy I/O adapters** attach PCI bridges via I/O ropes to Astro
4. **PCI**, the main I/O buses, attach to the multiple Elroy bridges

5. I/O devices, adapters and slots attach to PCI

2.6.7 EISA

Extended ISA or EISA is an device I/O and expansion bus that replaced the 1980s ISA bus in HP Unix workstations and servers. EISA buses are found in various early 32-bit workstations, either on-board or through a bus converter; this industry standard bus made it possible to use third-party, generic expansion cards such as network interfaces and SCSI controllers.

- ◇ 32-bit data path width
- ◇ 33 MB/s maximum data rate
- ◇ 8.33 MHz maximum frequency
- ◇ 5 V signalling voltage
- ◇ EISA slots also accept 8/16-bit ISA cards, downwards compatible
- ◇ 200-pin edge male card connector
- ◇ Bulkhead is left of the card

2.6.8 SGC

System Graphics Connect (SGC) is the extension of the main VSC system bus in early 32-bit HP 9000 700 workstations. Expansion cards are available in two different form factors: EISA and DIO.

- ◇ 32-bit data path width
- ◇ 100 MB/s maximum data rate
- ◇ 5 V signalling voltage
- ◇ 176-pin female pin+socket card connector in the DIO-II formfactor
- ◇ 160-pin male EBBI card connector EISA formfactor

2.6.9 HP-PB

The HP-Precision Bus HP-PB, sometimes HP/PB, is the I/O bus in many older 32-bit HP servers. Two form factors/sizes of HP-PB expansion cards were sold: single and double.

- ◇ 32-bit data path width
- ◇ 32 MB/s maximum data rate
- ◇ 8 MHz maximum frequency
- ◇ 5 V signalling voltage
- ◇ 96-pin female pin+socket card connector

2.6.10 PCI

With PCI HP changed its HP 9000 workstation and server design to an industry standard expansion and device bus. This allowed for using more off-the-shelf I/O chips and cards. Some HP PCI expansion cards for HP 9000 computers are relabeled third-party or OEM designs with PA-RISC compatible firmware and HP-UX driver.

Proper HP-UX drivers are the limiting factor for generic third-party PCI expansion cards in PA-RISC systems. In most cases drivers are only available for the HP-branded products. Open source operating systems as Linux or OpenBSD support many more devices in their PA-RISC ports.

Table 2.19: PCI buses used in PA-RISC computers overview

PCI	Clock	Width	Data ratemax	Signalling
PCI-32/33	33 MHz	32-bit	133 MB/s	3.3 V/5 V
PCI-32/66	66 MHz	32-bit	266 MB/s	3.3 V
PCI-64/33	33 MHz	64-bit	266 MB/s	3.3 V/5 V
PCI-64/66	66 MHz	64-bit	533 MB/s	3.3 V
PCI-X 64/66	66 MHz	64-bit	533 MB/s	3.3 V
PCI-X 64/100	100 MHz	64-bit	800 MB/s	3.3 V
PCI-X 64/133	133 MHz	64-bit	1066 MB/s	3.3 V

2.6.11 Documentation

- ◇ A High-Performance, Low-Cost Multiprocessor Bus for Workstations and Midrange Servers William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- ◇ An I/O System on a Chip, Thomas V. Spencer et al (April 1995, Hewlett-Packard Journal)
- ◇ HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC (pp. 188-189, 191, 198) Hewlett-Packard Company (July 1998, 14th ed.)
- ◇ Corporate Business Servers: An Alternative to Mainframes for Business Computing (.pdf) Thomas B. Alexander et al (June 1994: Hewlett-Packard Journal)

2.7 PA-RISC Graphics Adapters

2.7.1 Overview

HP 9000 and PA-RISC workstations were shipped almost exclusively with custom HP graphics adapters. HP designed a variety of video cards for different use cases, from simple 1990s 2D design to more advanced CAD/CAM, 3D modeling and advanced scientific design.

PA-RISC graphics adapters used a variety of HP video chips and GPUs, available for different buses (GSC, SGC, PCI) and form factors. Some of the more advanced cards were immensely expensive (>\$20k).

This article describes 1990s-era HP-proprietary designs for HP workstations. Full support for PA-RISC graphics cards is available only in HP-UX, with incomplete support in other and open source systems, especially for 3D and acceleration.

In some later 64-bit PA-RISC workstations, HP switched to off-the-shelf PCI video chipsets from the Intel/x86 world, customized for HP workstations. HP also shipped some of its PA-RISC video adapters with its Intel NT-based Visualize workstations.

Device	Colormax	3D	Output	Bus	Platform
GRX	8-bit gray	-	BNC	SGC	PA-RISC HP-UX
CRX	8-bit	-	BNC	SGC	PA-RISC HP-UX
Stinger (CRX)	8-bit	-	VGA	SGC	PA-RISC HP-UX
Artist (CRX)	8-bit	-	VGA	GSC	PA-RISC HP-UX
CRX-24/CRX-24Z	24-bit	(Z)	BNC/VGA	SGC	PA-RISC HP-UX
CRX-48Z	24-bit	yes	BNC/VGA	SGCGSC	PA-RISC HP-UX
HCRX-8/HCRX-8Z	8-bit	(Z)	VGA	GSC	PA-RISC HP-UX
HCRX-24/HCRX-24Z	24-bit	(Z)	VGA	GSC	PA-RISC HP-UX
Visualize-EG	8-bit	-	VGA or EVC	onboard GSCPCI	PA-RISC HP-UX
Visualize-8	8-bit	yes	VGA or EVC	GSC	PA-RISC HP-UX
Visualize-24	24-bit	yes	VGA or EVC	GSC	PA-RISC HP-UX
Visualize-48/48XP	24-bit	yes	VGA or EVC	GSC	PA-RISC HP-UX
Visualize-FXE	24-bit	yes	VGA	PCI 32/66	PA-RISC HP-UX
Visualize-FX2/FX4/FX6	24-bit	yes	EVC	PCI 64/66	PA-RISC HP-UX
Visualize-FX5/FX10	24-bit	yes	VGA, DVI-D	PCI 64/66	PA-RISC HP-UX
HP FireGL-UX	24-bit	OpenGL	VGA, DVI-D	PCI 64/66	PA-RISC HP-UX
HP FireGL X1/X3	24-bit	OpenGL	2 DVI	AGP 8X	PA-RISC HP-UX
HP FireGL T2	24-bit	OpenGL	DVI, VGA	AGP 8X	PA-RISC HP-UX
Visualize fx2/fx4/fx6	24-bit	OpenGL	VGA	AGP+PCI	Intel Windows
Visualize fx2+/fx4+/fx6+	24-bit	OpenGL	VGA	AGP+PCI	Intel Windows
Visualize fx5/fx10	24-bit	OpenGL	VGA	AGP 2X	Intel Windows

2.7.2 PA-RISC CRX and HCRX Graphics

CRX

HP CRX are graphics adapters for HP 9000 PA-RISC workstations, available in different configurations for SGC and GSC buses in different formfactors. All adapters were officially only supported in HP-UX up to 10.20, some may still work in 11.00. CRX were often used in HP 9000 705, 710, 720, 730, 750 and 735 workstations

HP CRX cards output a fixed resolution of 1280x1024. CRX cards for SGC bus in the DIO-II formfactor use BNC connectors with either one (grayscale), three (RGB) or four (RGB and sync), while cards for SGC and GSC in EISA formfactor and mainboard-integrated CRX use HD15 VGA connectors.

The *Stinger* CRX adapter, integrated into some of the older ASP-based workstations (older 715, 725), supports four different resolution/refresh-rate combinations, which can be changed via a DIP switch on the back of the machine or in the PDC.

Device	Color Resolution	Memory	Double buffer	3D	Output	Bus and formfactor Part number
CRX	8-bit 1280x1024 72Hz	3 MB	Hardware	-	BNC	SGC DIO-II: A1659A
GRX	8-bit gray		Software	-	BNC	SGC DIO-II: A1924A
Stinger (CRX)	8-bit 1280x1024 gray 1024x768	1 MB	Software	-	VGA	SGC integrated
Artist (CRX)	8-bit 1024x768	1 MB	Hardware	-	VGA	GSC integrated
Artist ext. mem	8-bit 1280x1024	2 MB	Hardware	-	VGA	GSC integrated
CRX-24	24-bit		Hardware Software	-	BNC VGA	SGC DIO-II: A1439A SGC: A2673A
CRX-24Z	24-bit		Z-Buffer	yes	BNC VGA	DIO-II addon: A1454A SGC addon: A2674A
CRX-48Z	24-bit		Hardware Software Z-Buffer	yes	BNC/VGA	SGC DIO-II: A2091A (external) SGC: A2675A (external) GSC external: A4073A + A2091A GSC external: A4073B + A4074A
CR 2D	8-bit		Hardware Software	-	VGA	GSC: A4077A
CR 2D dual	8-bit		Hardware Software	-	2 VGA	GSC: A4078A

HP CRX video adapters were only used in 32-bit PA-RISC HP 9000 workstations like HP 9000 715, HP 9000 720, 730, 750 and HP 9000 735 and 755.

3D Acceleration (Z)

CRX with Z-suffix denotes an additional 3D acceleration board with a hardware 24-bit Z-buffer. These combined adapters like CRX-24Z support the same visuals as stand-alone versions but always provide 3D acceleration. Hardware acceleration can only be used with Starbase, PHIGS, PowerShade or PEX APIs. CRX-48Z adapters are internal GSC or SGC interface cards with a separate external processing box, which provides RGB output connectors.

Part numbers

Part numbers of CRX video cards:

- ◇ A1439A: HP CRX-24 on SGC, DIO-II form factor, picture at Wikipedia (A1439-66570)
- ◇ A1454A and A2674A: HP CRX-24Z daughter board for CRX-24, Z-Buffer at Wikipedia (A1454-66571), CRX-24Z at Wikipedia
- ◇ A1659A and A1659-66001: HP CRX on SGC, DIO-II form factor, picture at Wikipedia
- ◇ A1924A and A1924-66001: HP GRX on SGC, DIO-II form factor
- ◇ A2091A: HP CRX-48Z (external) on SGC DIO-II
- ◇ A2673A: HP CRX-24 on SGC
- ◇ A2675A: HP CRX-48Z (external) on SGC
- ◇ A4073A and A2091A (A4069A): HP CRX-48Z on GSC/SGC external
- ◇ A4073B and A2091A (A4074A?): HP CRX-48Z on GSC/SGC external

HCRX

HP HCRX are successors to HP CRX graphics adapters, used in HP 9000 and Visualize PA-RISC workstations. They were shipped in systems with GSC bus, either integrated into the mainboard or as a separate expansion board. HCRX output a fixed resolution of 1280×1024 and use a HD15 VGA connector.

Device	Color max	Double buffer	3D	Output	Bus and part number
HCRX-8	8-bit	Hardware Software	-	VGA	GSC: A4070A/A4070B GSC-M: A4315A
HCRX-8Z	8-bit	Z-Buffer	yes	VGA	GSC: A4079A/A4079B
HCRX-24	24-bit	Hardware Software	-	VGA	GSC: A4071A/A4071B GSC-M: A4316A
HCRX-24Z	24-bit	Z-Buffer	yes	VGA	GSC: A4179A
3D Accelerator for HCRX-8/24	%	Z-Buffer	yes	-	Daughter board: A4072A Daughter board: A4242A

HCRX-48Z	renamed Visualize-48	HP	A4244A	
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HP HCRX video adapters were mainly used in 32-bit PA-RISC HP 9000 715 workstations and many Visualize workstations, C100, C160, C200 and J-Class.

3D Acceleration (Z)

CRX with Z-suffix denotes additional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters like HCRX-24Z support the same visuals as stand-alone versions but always provide 3D acceleration. Hardware acceleration can only be used with Starbase, PHIGS, PowerShade or PEX APIs.

HCRX graphics adapters for HP 9000 PA-RISC workstations were succeeded by HP Visualize line of graphics cards. There was briefly a card called **HCRX-48Z** (A4244A) which was soon renamed and marketed as Visualize-48.

Part numbers

Part numbers of CRX video cards:

- ◇ A4070A and A4070B: HP HCRX-8 on GSC
- ◇ A4315A: HP HCRX-8 on GSC-mezzanine
- ◇ A4079A/A4079B: HP HCRX-8Z on GSC
- ◇ A4071A/A4071B: HP HRCX-24 on GSC, picture at Wikipedia
- ◇ A4316A: HP HRCX-24 on GSC-mezzanine
- ◇ A4179AB: HP HCRX-24Z on GSC
- ◇ A4072A: HP 3D Accelerator for HCRX
- ◇ A4242A: HP 3D Accelerator for HRCX “B-” models
- ◇ A4244A: HP HCRX-48Z 3D video adapter, 3 cards

Documentation

- ◇ Graphics Administration Guide for HP-UX 10.20 (.pdf) Hewlett-Packard (n.d.)
- ◇ Graphics Administration Guide for HP-UX 11 (.pdf) Hewlett-Packard (2006: B2355-1E003, Edition E0206)
- ◇ Standard Text Interface For Graphics Devices (.pdf) Hewlett-Packard (March 2000: Revision 8.13) **parisc linux**
- ◇ Support Matrix - HP-UX Workstations Processors, OS Versions and Graphics, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ HP Graphics Technology HP Technical Computing , Hewlett-Packard Company (1996: mirror accessed January 2024)

- ◇ HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC (pp. 188-189, 191, 198) Hewlett-Packard Company (July 1998, 14th ed.) **parisc linux**
- ◇ HP Professional, July 1995, hparchive.org archive
- ◇ HP 9000 Graphics Workstations, Solutions for the next generation, Hewlett Packard, 1995 **1000bit.it**
- ◇ HP Apollo Series 700 Graphics Systems: The Graphics Architecture of the 1990s, Hewlett Packard (October 1992, 5091-5717E) **hpmuseum**

2.7.3 Artist PA-RISC Graphics

When developing the HP 9000 712 workstation, HP integrated as much functionality in VLSI circuits as possible. This included re-developing an onboard version of the CRX adapter into the **Artist** graphics chip.

Artist graphics adapters were found in LASI-based workstations such as HP 9000 712, HP 9000 715 and were technically (almost) identical to CRX devices with much more supported resolutions and refresh rates. HP Artist had 1 MB VRAM as standard which could be extended to 2 MB.

HP aggressively integrated as much as circuitry possible with Artist to reduce manufacturing, manufacturing of the HP 712 graphics subsystem was a third of the CRX system, the entry level Artist itself only a fifth of CRX. Artist integrated almost everything but the VRAM into a single single CMOS_{26B} VLSI at 80 MHz, while the internal DACs and color tables run at 135 MHz.

Device	Resolutionmax	Colormax	Doublebuffer	3D	Output	Bus and formfactorPart number
Artist	1024x768	8-bit	Hardware	-	VGA	GSC (integrated)
Artistext. mem	1280x1024	8-bit	Hardware	-	VGA	GSC (integrated)

Color Recovery

For Artist, HP developed *HP Color Recovery Technology*, a system to display “millions of colors” within the cost constraints of an 8-bit (8-plane) graphics system. At the time, users often chose 8-bit adapters due to the high cost of systems with 24 planes.

With HP Color Recovery, the HP video system takes 24-bit data from an application and dithers it down to 8-bit for the frame buffer, from where it is scanned through a DSP to the display, “where millions of colors can be viewed.” Besides Artist, Color Recovery was also part of the HCRX-8 adapter.

Color Recovery was used in HP integrated Artist video systems on various 32-bit workstations such as HP 9000 712 workstation and some HP 9000 715 workstations (LASI-based).

Documentation

- ◇ Graphics Administration Guide for HP-UX 10.20 (.pdf) Hewlett-Packard (n.d.)
- ◇ Graphics Administration Guide for HP-UX 11 (.pdf) Hewlett-Packard (2006: B2355-IE003, Edition E0206)
- ◇ Support Matrix - HP-UX Workstations Processors, OS Versions and Graphics, Hewlett-Packard Company (2001: mirror)
- ◇ Famous Graphics Chips: HP’s Artist Graphics, Jon Peddie, computer.org 2020
- ◇ An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation (PDF, HP Journal 4/95)
- ◇ HP Color Recovery Technology (PDF, HP Journal 4/95)

2.7.4 HP Visualize PA-RISC Graphics

The HP Visualize line of graphics adapters were used in a large number of PA-RISC workstations integrated onto the mainboard and in expansion cards of various types. HP Visualize were the designated successors to HP HCRX graphics adapters.

Visualize architecture

HP integrated parallel PA-RISC floating point technology from the PA-7200 processor (FPU) into Visualize graphics boards to increase scalable performance and speed up the graphics pipeline. Two FPU cells were added to the -8 and -24, and six cells into the -48. This was heralded as “quite interesting” and “good but unusual.”

All Visualize provide 2D hardware acceleration, used by HP's X11 server on HP-UX. Visualize 3D hardware acceleration is available with Starbase, PHIGS, PowerShade or PEX APIs. Visualize cards have HD15 VGA or EVC connectors.

Visualize video cards

Device	Resolution max	Color max	Double buffer	3D	Bus and part number
Visualize-EG base	1280×1024	8-bit	Software	-	onboard with 2MB memory GSC: A4450A HSC: A3519A PCI: A4977A with 4MB SGRAM PMC: A4979A
Visualize-EG dual	1280×1024	8-bit	Software	-	GSC: A4451A
Visualize-EG ext. mem	1600×1200	8-bit	Software Hardware	-	GSC: with A4452A
Visualize-8	1280×1024	8-bit	Hardware	yes	GSC: A4441A
Visualize-24	1280×1024	24-bit	Hardware Software	yes	GSC: A4442A
Visualize-48	1280×1024	24-bit	Hardware Software	yes	GSC: A4244A
Visualize-48XP	1280×1024	24-bit	Hardware Software	yes	GSC (dual): A4246A HSC: A4455A

Part numbers

Part numbers of Visualize for PA-RISC:

- ◇ A4450A: HP Visualize-EG base, GSC
- ◇ A3519A: HP Visualize-EG base, HSC
- ◇ A4977A: HP Visualize-EG base, PCI 4 MB SGRAM
- ◇ A4979A: HP Visualize-EG base, PMC

- ◇ A4451A: HP Visualize-EG dual, GSC
- ◇ A4452A: HP Visualize-EG external memory
- ◇ A4441A: HP Visualize-8 GSC
- ◇ A4442A: HP Visualize-24 GSC
- ◇ A4244A: HP Visualize-48 GSC
- ◇ A4246A: HP Visualize-48XP GSC (dual)
- ◇ A4455A: HP Visualize-48XP HSC

HP VisualEyes

Interestingly, HP very briefly called these cards *HP VisualEyes* before renaming and marketing them under *HP VISUALIZE* as successors to the HCRX line of adapters.

Prices

- ◇ Visualize-8 for \$5,500
- ◇ Visualize-24 for \$7,000
- ◇ Visualize-48 for \$16,000

Documentation

- ◇ An Overview of the VISUALIZE fx Graphics Accelerator Hardware, HP Journal 1998, Article 4
- ◇ hp visualize fx5pro/fx10pro UNIX graphics accelerators data sheet, HP 2000, 5980-1411E
- ◇ HP VISUALIZE fx4 Whitepaper, HP 1997, no URL
- ◇ HP VISUALIZE fx5 and fx10 Configuration Guide, HP 2000, A5021-90015 [vga museum](#)
- ◇ HP fx Graphics Card Installation and Configuration Guide (fxe, fx5 and fx10), HP 2000, A5021-90015 [vga museum](#)
- ◇ Overview HP FX Graphics, HP 2003, website
- ◇ NEW HP NT AND UNIX DESKTOPS HOST LATEST VISUALIZE GRAPHICS, Techmonitor archive, 1997
- ◇ HP DUMPED HIGH-END GRAPHICS BECAUSE SGI OWNS THE MARKET, Techmonitor archive, 1998

2.7.5 HP Visualize-FX PA-RISC Graphics

HP Visualize-FX are HP video adapters and 3D accelerators for PA-RISC Unix workstation and a major redesign of their Visualize predecessors. The architecture of the graphics processors is PA-RISC based, the higher-end models in fact include more than four PA-RISC FPU cells to process the graphics.

Visualize FX were the first HP cards to support OpenGL X-Window Extension (GLX) in addition to the legacy 3D APIs (Starbase, PEX, PHIGS). FX adapters for PA-RISC were only available as PCI bus cards and only supported under HP-UX.

Visualize-FX video cards

Device	Color resolution	RAM	3D	Output	Bus	Part number
Visualize-FXE	24-bit	18 MB SGRAM	yes	VGA	PCI 32-bit 66 MHz	A4982A
Visualize-FXE rev b	24-bit 1600x1200	24 MB SDRAM	yes	VGA	PCI 32-bit 66 MHz	A4982B
Visualize-FX2	24-bit 1280x1024	16 MB SGRAM	yes	EVC	PCI 64-bit 66 MHz	A4552A
Visualize-FX4	24-bit 1600x1200	18 MB SGRAM	yes	EVC	PCI 64-bit 66 MHz	A4553A
+ optional		16 MB SDRAM	yes		daughter board	A4559A
Visualize-FX5	24-bit 1920x1200	64 MB SDRAM	yes	VGA DVI-D stereo	PCI 64-bit 33/66 MHz	A1264A
Visualize-FX5pro	24-bit 1920x1200	64 MB SDRAM	yes	VGA DVI-D stereo	PCI 64-bit 33/66 MHz	A1262A A1262-66501
Visualize-FX6	24-bit 1600x1200	18 MB SGRAM	yes	EVC	PCI 64-bit 66 MHz	A4554A
+ optional		16 MB SDRAM	yes		daughter board	A4560A
Visualize-FX10	24-bit 1920x1200	128 MB DDR	yes	VGA DVI-D stereo	PCI 64-bit 66 MHz	A1299A A1299-66503?
Visualize-FX10pro	24-bit 1920x1200	128 MB DDR	yes	VGA DVI-D stereo	PCI 64-bit 66 MHz	A1299B A1299-69003?

Visualize FX5/10pro models integrate the raster and texture-processor onto a single chip, resulting in a better performance than the standard FX5/10. Onboard RAM is used as unified buffer, Z-buffer and texture storage

Part numbers

Part numbers of Visualize FX for PA-RISC:

- ◇ A1262A and A1262-66501: HP Visualize FX5pro picture at Wikipedia
- ◇ A1264A: HP Visualize FX5

- ◇ A1299A and A1299-66503: HP Visualize FX10 picture at Wikipedia
- ◇ A1299B and A1299-69003: HP Visualize FX10pro
- ◇ A4552A: HP Visualize FX2
- ◇ A4553A and A4553-66501: HP Visualize FX4, picture at Wikipedia
- ◇ A4554A: HP Visualize FX6
- ◇ A4559A: Texture accelerator for HP Visualize FX4
- ◇ A4560A: Texture accelerator for HP Visualize FX6
- ◇ A4982A: HP Visualize FXE
- ◇ A4982B: HP Visualize FXE revision B

Note: Slight uncertainty on FX5 part numbers.

Documentation

- ◇ An Overview of the VISUALIZE fx Graphics Accelerator Hardware, HP Journal 1998, Article 4
- ◇ hp visualize fx5pro/fx10pro UNIX graphics accelerators data sheet, HP 2000, 5980-1411E
- ◇ HP VISUALIZE fx4 Whitepaper, HP 1997, no URL
- ◇ HP VISUALIZE fx5 and fx10 Configuration Guide, HP 2000, A5021-90015 **vga museum**
- ◇ HP fx Graphics Card Installation and Configuration Guide (fxe, fx5 and fx10), HP 2000, A5021-90015 **vga museum**
- ◇ Overview HP FX Graphics, HP website 2003,
- ◇ Overview ATI Fire GL UX , HP website 2003,
- ◇ HP Visualize FX, PA-RISC Linux, 2024

2.7.6 HP FireGL PA-RISC Graphics

HP sold several ATI video and 3D adapters for PA-RISC workstations running HP-UX, such as the c8000. The *HP FireGL* cards were modified ATI cards with ATI GPUs, modified slightly for HP-UX with HP providing drivers for HP-UX for 64-bit workstations running HP-UX 11.00 and higher.

Device	GPU	Color resolution	RAM	3D	Output	Bus	Part number
HP FireGL-UX (ATI FireGL-3)	GT1000 RC1000	24-bit 1920×1200	128 MB DDR	yes OpenGL	VGA DVI-D stereo	PCI 3.3V 64-bit 66 MHz	A7789A A7789-69510
ATI FireGL T2	RV350 9600 Pro	24-bit 2048×1536	128 MB DDR	yes OpenGL	DVI VGA	AGP 8X	AB638A
ATI FireGL X1	R300GL FGL-9700	24-bit 1920×1200	256 MB DDR	yes OpenGL	2 DVI	AGP 8X	A9653A
ATI FireGL X3	R420 X800 XT	24-bit 2048×1536	256 MB GDDR3	yes OpenGL	2 DVI	AGP 8X 1.5V	AB668A

Certain patches for HP-UX were required for proper X11 and 3D OpenGL functionality, dated 2002 and later. This included hardware-enablement (HWE) and specific patches and HP-UX software modules.

Part numbers of HP FireGL video adapters:

- ◇ A7789A and A7789-69510: HP FireGL-UX PCI
- ◇ A9653A: ATI FireGL X1 AGP 8X
- ◇ AB638A: ATI FireGL T2 AGP 8X
- ◇ AB668A: ATI FireGL X3 AGP 8X

FireGL-UX architecture

The FireGL-UX high-end graphics adapter was based on ATI FireGL2 or -3 board adapted for PA-RISC workstations on HP-UX Unix. It provides full OpenGL hardware acceleration with the HP X server on HP-UX and is binary compatible with HP Visualize FX10pro adapters. FireGL-UX is about twice as fast as the Visualize FX10pro.

- ◇ IBM GT1000 geometry engine
- ◇ IBM RC1000 raster engine
- ◇ 128 MB DDR SDRAM for unified frame buffer, Z-buffer and texture storage
- ◇ Digital DVI and 3-pin stereo output
- ◇ 64-bit, 66 MHz PCI card
- ◇ Part number: A7789A, A7789-60510, A7789-69510

ATI and nVIDIA for Itanium

HP Itanium workstations such as zx6000 and zx2000 were able to use a few third-party 3D graphics adapters on AGP Pro with Linux and HP-UX drivers.

Table 2.27: Maximum resolution with DVI monitors is mostly only 1600x1200

Device	GPU	Color resolution*	RAM	3D	Output	Bus	System	Part number
ATI FireGL4	GT1000 RC1000	24-bit 1920x1200	128MB DDR	yes OpenGL	2 DVI TV	AGP 4X	HP-UX	A7226-60520 A7226-69520
ATI FireGL X1	R300GL FGL-9700	24-bit 1920x1200	256MB DDR	yes OpenGL	2 DVI TV	AGP 8X Pro	HP-UX	313287-001 312523-001
ATI FireGL Z1	R300GL 9500 Pro	24-bit 1920x1200	128MB DDR	yes OpenGL	2 DVI TV	AGP 8X Pro	HP-UX	313287-001 312523-001
ATI Radeon 7000	RV100	24-bit 2048x1536	32MB DDR	(yes) OpenGL	DVI VGA	AGP	HP-UX Linux	A8049-60520 A8049-69520
nVIDIA Quadro2 EX	NV11GL	24-bit 2048x1536	32MB SDR	yes OpenGL	VGA	AGP	Linux	A7806-60510 A7806-69510
nVIDIA Quadro4 900XGL	NV25	24-bit 2048x1536	128MB DDR	yes OpenGL	2 DVI	AGP 4X	Linux	A8064-60520 A8064-69520
nVIDIA Quadro4 980XGL	NV28GL	24-bit 2048x1536	128MB DDR	yes OpenGL	2 DVI	AGP 8X	Linux	308961-001 313285-001

Part numbers of HP AT and nVIDIA video adapters for Itanium:

- ◇ A7226-60520 and A7226-69520: ATI FireGL4
- ◇ 313287-001 and 312523-001: ATI FireGL X1
- ◇ 313286-001: ATI FireGL Z1
- ◇ A8049-60520 and A8049-69520: ATI Radeon 7000
- ◇ A7806-60510 and A7806-69510: nVIDIA Quadro2 EX
- ◇ A8064-60520 and A8064-69520: nVIDIA Quadro4 900XGL
- ◇ 308961-001 and 313285-001: nVIDIA Quadro4 980XGL

Documentation

- ◇ Overview HP FX Graphics, HP 2003, website
- ◇ Overview ATI Fire GL UX , HP 2003, website
- ◇ Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000

2.7.7 HP Visualize *fx* Intel

HP offered Visualize *fx* video adapters for its Intel-based Visualize P-Class and X-Class NT workstations in the late 1990s, first developed for HP Kayak workstation. Visualize *fx* adapters for Intel were AGP, AGP Pro and often dual-slot cards with PCI. They had impressive speeds for 3D design and CAM/CAD use cases but were only offered for a few years for HP Windows NT workstations and in small quantities.

Similar to their Unix Visualize FX brethren, *fx* and *fx+* integrated PA-RISC FPU cores into their graphics accelerator with a Cirrus Logic 2D graphics chip for GUI (GD5480), at least on the AGP-PCI dual slot cards. The Visualize graphics accelerator ASIC consisted of “2 integer ALUs, 2 floating-point multipliers, 2 floating point divider/square root units and dual control,” possibly based on PA-7200 PA-RISC CPU and/or FPU.

Device	Color resolution	Chips or cores	RAM	3D	Out	Bus
Visualize <i>fx2</i>	24-bit 1600x1200	0 Texture 2 Geometry 2 Raster	18 MB SGRAM	Hardware OpenGL	VGA	AGP dual with PCI AGP 64-bit 66 MHz
Visualize <i>fx4</i>	24-bit 1600x1200	0 Texture 2 Geometry 2 Raster	18 MB SGRAM	Hardware OpenGL	VGA	AGP dual with PCI AGP 64-bit 66 MHz
+ <i>fx</i> texture		1 Texture	16 MB SDRAM	Hardware		daughter board
Visualize <i>fx6</i>	24-bit 1600x1200	0 Texture 2 Geometry 2 Raster	18 MB SGRAM	Hardware OpenGL	VGA	AGP dual with PCI AGP 2X 64- bit 133 MHz
+ <i>fx</i> texture		2 Texture	32 MB SDRAM	Hardware		daughter board
Visualize <i>fx2+</i>	24-bit	0 Texture 1 Geometry 2 Raster	18 MB SGRAM opt. Texture	Hardware OpenGL	VGA	AGP dual with PCI AGP 2X 64- bit 133 MHz – maybe also AGP Pro
Visualize <i>fx4+</i>	24-bit 1600x1200	0 Texture 2 Geometry 2 Raster	18 MB SGRAM opt. Texture	Hardware OpenGL	VGA	AGP dual with PCI AGP 2X 64- bit 133 MHz – maybe also AGP Pro
Visualize <i>fx6+</i>	24-bit 1600x1200	0 Texture 3 Geometry 2 Raster	18 MB SGRAM opt. Texture	Hardware OpenGL	VGA	AGP dual with PCI AGP 2X 64- bit 133 MHz – maybe also AGP Pro
+ <i>fx+</i> texture		1 Texture	16 MB SDRAM	-	-	daughter board
Visualize <i>fx5</i>	32-bit 1900x1200	1 Texture 3 Geometry	64 MB SDRAM	Hardware OpenGL	VGA	AGP 2X 64- bit 133 MHz AGP Pro?

Visualize <i>fx10</i>	32-bit 1900x1200	1 Texture 6 Geometry	64 MB SDRAM	Hardware OpenGL	VGA DVI	AGP 2X 64-bit 133 MHz AGP Pro?
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Visualize *fx* cards for Intel-based computers were first developed for HP Kayak personal workstations and marketed as part of their product lineup, which later got renamed to Visualize personal workstations (with Intel Pentium III).

Care had to be taken in selecting correct AGP slots and cards, as not all *fx* cards were compatible with all systems, with specific cards designated for some systems. Drivers were available for Intel-based computers on Windows NT and later 2000. At least *fx5* and *fx10* supported OpenGL 1.1, GDI, DirectDraw, and Direct3D.

Some part numbers for Visualize NT adapters – incomplete and a bit confusing:

- ◇ A5013-69001: HP Visualize *fx2* AGP and PCI
- ◇ A5012-69001: HP Visualize *fx4* AGP and PCI
- ◇ A1278-60001 and A1278-69001: HP Visualize *fx4+* AGP Pro with PCI
- ◇ A1277-60001 and A1277-69001: HP Visualize *fx6+* AGP Pro with PCI, picture at Wikipedia and back
- ◇ A5022-60001 and A5022-69001: HP Visualize *fx+* Texture module, picture at Wikipedia
- ◇ A1264-66501 and A1264-69001: HP Visualize *fx5* AGP 2X
- ◇ A1264-66502 and A1264-69002: HP Visualize *fx10* AGP 2X

Documentation

- ◇ VISUALIZE Workstation Graphics for Windows NT, HP Workstation Lab 1998
- ◇ HP VISUALZIZE Graphic Subsystems, HP Website 1999
- ◇ HP Kayak Workstation Graphics Solution, HP Website 1999
- ◇ HP Kayak: A PC Workstation with Advanced Graphics Performance, HP Journal May 1998, p. 35ff [hp archive](#)
- ◇ hp IA-32 visualize *fx5* and *fx10* Windows graphics accelerator, HP 2000 [vga museum](#)
- ◇ hp IA-32 visualize *fx5* and *fx10* Windows graphics accelerators, HP 2000 [vga museum](#)

Announcements

- ◇ NEW HP NT AND UNIX DESKTOPS HOST LATEST VISUALIZE GRAPHICS, Techmonitor archive, 1997
- ◇ HP DUMPED HIGH-END GRAPHICS BECAUSE SGI OWNS THE MARKET, Techmonitor archive, 1998

Drivers

- ◇ hp workstation Windows 2000 hp visualize fx5, fx10 video drivers, HP website 2001
- ◇ hp workstation Windows 2000 visualize fx2+, fx4+, fx6+ video drivers, HP website 2001

2.8 PA-RISC Expansion Cards

There were many HP custom expansion cards sold with and for HP 9000 computers. Many were custom designs, other were, sometimes relabeled, third party designs. This list is not exhaustive and based on HP documentation from the 1990s.

2.8.1 EISA/ISA

HP designed and shipped many custom EISA expansion cards for its HP 9000 workstations and servers.

- ◇ A2544A - Apollo Token Ring/9000 adapter
- ◇ A2545A - Apollo Token Ring/9000 adapter and EISA slot (for 720)
- ◇ A2679A - Fast SCSI-2 host adapter
- ◇ A3402A - 10/100VG LAN interface
- ◇ A3658A - 100BaseT Ethernet interface
- ◇ A3659A - FDDI interface
- ◇ A4031A - Fiberchannel interface 266Mb
- ◇ A4308A/A4308B - 100BaseT Ethernet interface
- ◇ B5502AA - FDDI interface
- ◇ E2070A/B/C - HP-IB interface, normal speed (*ISA*)
- ◇ E2071A/B/C/I - HP-IB interface, high speed
- ◇ E2074A/B - GPIO interface
- ◇ J2104A - ISDN BRI (*ISA*)
- ◇ J2109A - ISDN BRI (for the US) (*ISA*)
- ◇ J2159A - X.25 interface
- ◇ J2165A - IEEE 802.5 token ring interface
- ◇ J2220B - Programmable Serial Interface
- ◇ J2226A - SNAplus link
- ◇ J2460A - ISDN ISA/EISA adapter
- ◇ J2482A - 8-port RS232C multiplexer
- ◇ J2483A - 64-port RS232C multiplexer
- ◇ J2645AA - 10/100VG LAN interface (no Ethernet!)
- ◇ J2794A - X.25 interface
- ◇ J2802A - ATM interface, OC3/155Mb (*only 700 series*)
- ◇ J2802B - ATM interface, OC3/STS-3c 155Mb (*only 700 series*)
- ◇ J2815A - dual port Programmable Serial Interface
- ◇ 25525A/25525B - fast narrow (8-bit) HVD SCSI-2 interface

- ◇ 25560A - HP-IB interface, high speed
- ◇ 25567B - EISA LAN Ethernet card
- ◇ more...

Other Vendors

- ◇ Interphase WA-C321T-UX - FDDI SAS interface
- ◇ Interphase WA-C323T-UX - CDDI SAS interface
- ◇ Interphase WA-C326T-UX - FDDI DAS interface
- ◇ Interphase WA-C328T-UX - CDDI DAS interface
- ◇ Interphase 4811 - FDDI single MIC, single/dual UTP, single/dual STP
- ◇ Interphase 4824 - 100BaseT/10BaseT Ethernet interface
- ◇ MDL Corp. FAWS - wide single-ended SCSI-2 interface
- ◇ MDL Corp. FAW - wide differential SCSI-2 interface
- ◇ Parallax XVideo 700 - Video export/import
- ◇ Qualix IW-h100 - Phobos 10BaseT interface
- ◇ SBE WSU 432S - wide single-ended SCSI-2 interface
- ◇ SBE WSU 432D - wide differential SCSI-2 interface
- ◇ FE Phobos H100 Fast EISA Ethernet
- ◇ 3Com 3c597-TX EISA Fast Ethernet, should work with the above Phobos driver

2.8.2 GSC/HSC

The default formfactor of GSC cards is sized similarly to an standard EISA card, so it is called *EISA formfactor*; there was also the *HSC* (about 3×5 inches) and *GSC-M* form-factor. Some GSC+ cards are also called HSC, but in fact are in the EISA formfactor

EISA formfactor

- ◇ A2874-66005 - Fast-Wide high-voltage differential (HVD) SCSI-2 interface
- ◇ A4107A - wide SCSI-2 interface
- ◇ A3723A - FDDI interface
- ◇ A4070A/A4070B - HCRX-8 graphics
- ◇ A4071A/A4071B - HCRX-24 graphics
- ◇ A4072A - 3D accelerator for any HCRX graphics
- ◇ A4073A/A4073B - CRX-48Z GSC interface (for CRX-48Z graphics processor)
- ◇ A4074A - CRX-48Z graphics processor

- ◇ A4077A/A4077B (A4081-66009) - CR 2D 8-bit color graphics
- ◇ A4078A - Dual CR 2D graphics
- ◇ A4079A/A4079B - HCRX-8Z graphics (*in fact is A4070B + A4072A*)
- ◇ A4179A - HCRX-24Z graphics (*in fact is A4071B + A4072A*)
- ◇ A4211A - Visualize-48 graphics
- ◇ A4242B - Z-Buffer + accelerator for HCRX graphics
- ◇ A4244A - Visualize-48 graphics
- ◇ A4245A - texture memory for the above
- ◇ A4246A - Visualize-48XP graphics, EVC
- ◇ A4247A - texture memory for the above
- ◇ A4247A - video export daughter card for HCRX graphics
- ◇ A4253-69001 - Freedom Interface graphics, 13W3 connector
- ◇ A4253A - Freedom S3150 graphics accelerator
- ◇ A4254A - Freedom S3250 graphics accelerator
- ◇ A4255A - Freedom S3400 graphics accelerator
- ◇ A4333A - Visualize-IVX graphics, daughter card to HCRX graphics
- ◇ A4441A - Visualize-8 graphics (*in fact is A4070B + A4242A*)
- ◇ A4442A - Visualize-24 graphics (*in fact is A4071B + A4242A*)
- ◇ A4443A - upgrade HCRX-{8,24}Z to Visualize-{8,24}
- ◇ A4450A - Visualize-EG graphics, EVC
- ◇ A4451A - Dual Visualize-EG graphics, EVCconnector
- ◇ A4452A - 2MB add-on memory for A4450A & A4451A
- ◇ A4925A (A4925-60001) - 1000BaseSX fibre Gigabit-Ethernet
- ◇ A4926A - 1000BaseSX Gigabit-Ethernet interface
- ◇ J2498A - ATM interface, 155Mb
- ◇ J2499A - ATM interface, OC3c 155Mb
- ◇ J3515A - 100BaseT/10BaseT/AUI Ethernet interface
- ◇ J3516A - 100BaseT/10BaseT dual port Ethernet interface
- ◇ more...

HSC formfactor

- ◇ A2969A (A2926-60001) - Fast-Wide Differential (HVD) SCSI Adapter.
- ◇ A2999A - Color graphics, Dsub15 connector
- ◇ A3519A - Visualize-EG graphics, EVC

- ◇ A3722A - FDDI interface
- ◇ A4455A - Visualize-48XP graphics, EVC
- ◇ A4924A - 1000BaseSX
- ◇ J2468A - ATM/622
- ◇ J2469A - ATM/155 adaptor
- ◇ J2803A - ATM adaptor, OC3/155 Mbps
- ◇ J2803B - ATM adaptor, OC3/UTP5/155 Mbps
- ◇ J2499A (J2499-60011) - ATM interface, OC3c 155Mb
- ◇ J3514A (J3514-60001) - Dual 10/100Mbit Ethernet interface
- ◇ more...

GSC mezzanine formfactor

- ◇ A4248A - Video Export Board (GSC daughter)
- ◇ A4267A - 8-plane graphics
- ◇ A4268A - Fast Wide SCSI
- ◇ A4315A - HCRX-8VME
- ◇ A4316A - HCRX-24VME
- ◇ A4333A - HP VISUALIZE-IVX (GSC daughter)
- ◇ J3420A - ATM adaptor, OC3/UTP5/155 Mbps
- ◇ Z5117A - PCMCIA adaptor for 743rt

Special formfactors

- ◇ A2889A - fwdSCSI interface (B132L and B160L only)
- ◇ A2991-60001 - Access Port modem (C160, C180, C200 and C240 only)
- ◇ A3262-69211 - Access Port modem (C160, C180, C200 and C240 only)
- ◇ A2654A - FDDI Single, Daughter interface for 755
- ◇ A2658A - 802.3 AUI Daughter for 735
- ◇ A2665A - FDDI Daughter for 735
- ◇ A2831A - 802.3 10Base2 ThinLAN Daughter for 735

2.8.3 SGC

There are two types of SGC expansion cards: the bigger cards, called *DIO-II formfactor* and the EISA-like (*EISA formfactor*) cards.

DIO-II formfactor

- ◇ A1439A - CRX-24 graphics
- ◇ A1454A - CRX-24Z, Z-buffer daughter board for the above card
- ◇ A1471A - Personal VRX graphics, RGB BNC
- ◇ A1472A - Turbo VRX graphics, RGB BNC
- ◇ A1659A - CRX graphics
- ◇ A1924A - GRX graphics
- ◇ A1986A - EISA slot for model 720
- ◇ A2089A - Video/Audio for 715s/t
- ◇ A2091A - CRX-48Z graphics processor, (*external break-out box*)
- ◇ A2091A-66580 - CRX-48Z SGC interface (for the above)
- ◇ A2262A - Dual CRX graphics
- ◇ A2269A - Non-CRX to Dual-CRX graphics/Dual-CRX to Quad-CRX graphics upgrade
- ◇ A2270A - CRX-24 to Dual CRX-24 graphics upgrade
- ◇ A2271A - CRX to CRX-24 graphics upgrade
- ◇ A2288-66003 - Audio-adaptor board with room for optional FDDI slider
- ◇ A2666A - CRX-24Z to CRX-48Z graphics upgrade
- ◇ A2667A - PVRX to CRX-48Z graphics upgrade
- ◇ 98705P - P-VRX P3 graphics, RGB BNC
- ◇ 98768A - CRX graphics upgrade
- ◇ more...

EISA formfactor

- ◇ A2673A - CRX-24 graphics interface
- ◇ A2674A - CRX-24Z, Z-Buffer daughter board for the above card
- ◇ A2675A - CRX-48Z graphics interface processor, (*external break-out box*) with
A2675-66581 - CRX-48Z SGC interface
- ◇ A2804A - EISA slot for model 715
- ◇ more...

2.8.4 GIO/TSIO

GIO is the special formfactor of GSC expansion cards for HP 9000 712 systems.

- ◇ A2878A - second video

- ◇ A4011A - 802.5 Token Ring interface
- ◇ A4011B - 802.5 Token Ring interface
- ◇ A4013A - second serial port
- ◇ A4014A - second LAN (AUI+TP) and serial port. Pinout for the AUI/RS232 Y-cable
- ◇ A4015A - second serial and X25 link (DB9M RS232C connectors)
- ◇ A4217A - second LAN (AUI+TP) and second VGA
- ◇ TAMS 50488 - HP-IB interface
- ◇ TSIO: A4012A and A4012AJ - TeleShare POTS interface, analog RJ11C

2.8.5 HP-PB

There are two types of HP-PB expansion cards: single and double height.

- ◇ 28696-60001 - 16-bit differential (HVD) SCSI, double-height
- ◇ 28670-60101 - DAS FDDI with MIC connector, double-height
- ◇ 28640-60001 - 10Mbit Ethernet AUI/BNC, single.height
- ◇ A3495A (A3495A-60001, A3495A-60301) 10/100Mbit Ethernet TP, single-height
- ◇ J2157A - FDDI
- ◇ J2146A - 10Mbit Ethernet, single-height

2.9 PA-RISC SCSI Storage

2.9.1 Overview

HP 9000 workstations and servers mostly used industry-standard SCSI storage devices and controllers. There was a wide range of versions of the SCSI bus specification implemented in a variety of controller chips since the 1980s.

The table lists some of the variants of SCSI found in PA-RISC computers.

Table 2.29: SCSI buses in PA-RISC computers

SCSI	Spec	Clock	Width	Data rate max	Devices max	Signals note*	Length max	Connector
Narrow SCSI	SCSI-1	5 MHz	8-bit	5 MB/s	7	SE	6m	50-pin
Fast-Narrow SCSI	SCSI-2	10 MHz	8-bit	10 MB/s	7	SE HVD	3m 2.5m	50-pin
Fast-Wide SCSI	SCSI-2	10 MHz	16-bit	20 MB/s	15	SE HVD	3m 2.5m	68-pin
Ultra-Narrow SCSI	SCSI-3	20 MHz	8-bit	20 MB/s	7	SE LVD HVD	1.5m 1.2m 2.5m	50-pin
Ultra-Wide SCSI	SCSI-3	20 MHz	16-bit	40 MB/s	15	SE LVD HVD	1.5m 1.2m 2.5m	68-pin
Ultra2-Wide SCSI	SPI-2	40 MHz	16-bit	80 MB/s	15	LVD	1.2m	68-pin
Ultra160 SCSI	SPI-5	40 MHz	16-bit	160 MB/s	15	LVD	1.2m	68-pin
Ultra320 SCSI	SPI-5	80 MHz	16-bit	320 MB/s	15	LVD	1.2m	68-pin

* SCSI used different electrical interfaces for devices and cabling. SE is Single-Ended, HVD is High-Voltage-Differential and LVD is Low-Voltage-Differential. HVD devices and controllers must not be mixed with SE or LVD.

2.9.2 Controllers

HP 9000 workstations and servers from HP used common industry-standards SCSI controllers for drives and storage. These chips were often integrated into HP mainboards or implemented on plug-in cards for GSC and PCI buses.

Table 2.30: SCSI chipsets in PA-RISC computers

Chipset	Speed	Width	Data rate	Bus
NCR 53C700		Narrow	5 MB/s	GSC, HP-PB
NCR 53C710	Fast	Narrow	10 MB/s	GSC, EISA
NCR 53C720	Fast	Wide	20 MB/s	GSC, PCI, HP-PB

Symbios 53C875	Ultra	Wide	40 MB/s	PCI
LSI 53C896	Ultra2	Wide	80 MB/s	PCI

2.9.3 HP Adapters

HP produced custom SCSI adapters boards for its PA-RISC computers, using third-party SCSI chips for different SCSI and host system buses.

Table 2.31: Selection of HP 9000 SCSI expansion cards

Part	Bus	Chip	SCSI	Signals	Boot	HP-UX
A2679A	EISA	53C710	Fast-Narrow	SE	no	9.0-11i/32-bit
25525A	EISA	53C710	Fast-Narrow	HVD		8.05-10.20
25525B	EISA	53C710	Fast-Narrow	HVD		8.05-11.0/32-bit
A2874-66005	GSC	53C720	Fast-Wide	HVD	yes	9.05/11.0
A2969A	HSC	53C720	Fast-Wide	HVD	yes	10.01-11i
A3644A	HSC	53C720	Fast-Wide	HVD		10.20-11i
A4107A	GSC	53C720	Fast-Wide	HVD		9.05-11i/32-bit
A4268A	GSC-M	53C720	Fast-Wide	HVD	yes	9.05-11.0/32-bit
27251A	HP-PB					
28655A	HP-PB	53C710	Fast-Narrow	SE	yes	10.01-11i
28696A	HP-PB	53C720	Fast-Wide	HVD	yes	10.01-11i
A4800A	PCI	53C720	Fast-Wide	HVD	yes	10.2-11i
A4974A	PCI	53C875	Ultra-Wide	SE	yes	10.20-11.0
A4976A	PCI	53C720	Fast-Wide	HVD	yes	10.20-11.0
A4999A	PCI	53C896	Ultra2-Wide	LVD	yes	10.20-11.0
A5159A	PCI	53C720	Fast-Wide	HVD	yes	10.20-11i

2.10 PA-RISC Boot Menu

2.10.1 Overview

This article on the PDC Boot ROM on HP 9000 is incomplete and only covers early 700 workstation PDC interactions. It hopefully will be extended at some point.

HP 9000 PA-RISC computers include PDC, the processor dependent code, which functions as their firmware (boot ROM/their BIOS). PDC is used for initializing the devices and booting the system. Errors during the initialization PDC phase are displayed via error codes on the system front LEDs or LCD.

After performing selftests, the PDC searches for a proper console for I/O redirection and valid boot media for loading the operating system boot loader, ISL/IPL, to which system control is transferred then.

The PDC keeps a list of variables for system hardware and boot settings, which can be changed at the PDC prompt, accessible after power-up. If power-up is interrupted in order to enter the PDC, the following options are available:

- ◇ Choose the boot device
- ◇ Start a search for bootable devices containing an IPL
- ◇ Enter the boot administration prompt

PDC is specific to the individual hardware—it is contained in ROM/flash; the ISL/IPL boot loaders reside on the first blocks of PA-RISC boot media.

2.10.2 Boot Menu

PDC on workstations

In older 32-bit HP 9000 700 workstations, the following commands are available in the PDC menu (newer, 64-bit systems added and removed commands and variables):

Table 2.32: HP 9000 700 workstations PDC boot ROM commands

Command	Parameters	Description
AUTO		Displays the current state of the AUTOBOOT & AUTOSEARCH flags
AUTOSEARCH		Toggles whether or not the PDC automatically searches for bootable devices
AUTOBOOT		Toggles whether or not the PDC automatically boots the device described in either <i>primary</i> or <i>alternate</i> PATHs
BOOT	[device [isl]]	Boots from specified device or one of <i>pri</i> or <i>alt</i>
DATE		Sets or reads the real time clock
EXIT		Leave the PDC
FASTSIZE		Sets or reads the value of the FASTSIZE memory parameter
HELP	[item]	Shows general/ <i>item</i> -specific information

INFO		Gives info about the hardware, <i>e.g.</i> , CPU/IO/SCSI clock speeds, which LAN port is used, revision of the various chips and the PDC
LAN_ADDR		shows the MAC address of the Ethernet controller
OS		Could be used to indicate the installed operating system (probably for boot loader/kernel interaction and/or set up)
PATH	[path_type [device]]	Displays or sets either path_type or all paths in the Stable Storage path_type can be: primary, alternate, console and keyboard
PIM_INFO		Displays internal memory of the CPU, <i>e. g.</i> registers, stack
RESET		Resets the system
SEARCH	[device [ipl]]	Search either all device interfaces or just specified device interface for bootable media or IPL
SECURE		Displays or sets the secure boot mode flag — “locks” the system for 10 seconds before boot device choosing
SHOW		Shows results of the previous SEARCH

Devices

The following devices might be referenced on 700s workstations in the PDC:

- ◇ eisa.*: cards in the EISA slot(s)
- ◇ lan.*: one of the network adaptors
- ◇ graphics[_1,_2]: one of the video adaptors
- ◇ hil: HIL-input devices
- ◇ parallel: the parallel printer port
- ◇ rs232_a.*: the first serial port
- ◇ rs232_b.*: the second serial port

2.10.3 Examples

Some examples on using the PDC:

1. Show the current value of the console PATH:
BOOT_ADMIN>PATH console
2. Change this variable to the first serial port:
BOOT_ADMIN>PATH console rs232_a

3. Let the PDC search for bootable media:

```
BOOT_ADMIN>SEARCH ipl
```

4. Search only the local SCSI bus:

```
BOOT_ADMIN>SEARCH scsi ipl
```

5. Search for RBOOTD or BOOTP servers (for remote booting):

```
BOOT_ADMIN>SEARCH lan
```

6. Boot from the SCSI device at ID 6:

```
BOOT_ADMIN>BOOT scsi.6 isl
```

7. Boot HP-UX 10.20 in *single-user* mode (e. g. to repair the system):

```
BOOT_ADMIN>BOOT scsi.6 isl
```

```
ISL>hpux -is
```

2.11 PA-RISC LED codes

2.11.1 Overview

Many 32-bit and early 64-bit PA-RISC computers have status LEDs on the system front to indicate system status and errors during power-up self-tests. Newer 64-bit systems have LCDs for this purpose.

Systems with 9 LEDs

HP 9000 705 and 710, 715/33,50,75, 715/64,80,100 and 725 have 9 LEDs on the front:

8	7	6	5	4	3	2	1	0
A	A	A	A	A	A	A	A	G

0 is the Power LED, it indicates that the system is powered up. 4 is the *heartbeat*: if the system is running correctly, it flashes periodically.

Systems with 10 LEDs

HP 9000 720, 730, 750 and 735, 755 workstations have 10 status LEDs on the front:

9	8	7	6	5	4	3	2	1	0
G	A	A	A	A	A	A	A	A	G

The difference is LED number 9, the Service LED, which indicates whether the machine was booted in “Service mode”. On HP 9000 755 workstations, the LEDs are arranged from top to bottom, starting with LED 0, the Power LED.

Systems with 5 LEDs

HP Visualize workstations with LEDs like B-Class or C-Class have 5 LEDs: one Power LED and four System LEDs.

2.11.2 HP 9000 712

HP 9000 712 workstations only display two possible error messages on the single LED above the power button:

- ◇ 3/4-second flash pattern: CPU board defective
- ◇ “Three quick flashes, pause, three quick flashes” -pattern: graphics hardware problem

2.11.3 HP 9000 715 (Scorpio)

These codes apply to HP 9000 715/33, 50, 75 workstations and might be applicable to other HP 9000 workstations as well. Taken from the *Model 715 Owner's Guide*

Table 2.35: # – LED is on or flashing, / – LED is either on or off.

8	7	6	5	4	3	2	1	Error Message	Solution
–	–	–	#	/	/	/	/	CPU/FPU error	Probably replace main-board/CPU
–	–	#	–	/	/	/	/	CPU/FPU error	Probably replace main-board/CPU
–	–	#	#	/	/	/	/	CPU/Motherboard error	Probably replace main-board/CPU
–	#	–	–	/	/	/	/	CPU/FPU error	Probably replace main-board/CPU
–	#	–	–	#	–	–	#	FPU test failure	Reboot or replace CPU card
–	#	–	–	#	–	#	–	FPU test failure	Reboot or replace CPU card
–	#	–	–	#	–	#	/	FPU test failure	Reboot or replace CPU card
–	#	–	#	–	–	–	#	EISA interface error	Remove EISA cards and backplane, clean, and reinstall in the system. Replace hardware.
–	#	–	#	–	–	#	–	EISA interface error	Clean EISA cards and backplane. Replace.
–	#	–	#	–	–	#	#	EISA interface error	Clean EISA cards and backplane. Replace.
–	#	–	#	–	#	–	–	EISA interface error	Clean EISA cards and backplane. Replace.
–	#	–	#	–	#	–	#	EISA interface error	Clean EISA cards and backplane. Replace.
–	#	–	#	#	#	#	#	PDC ROM checksum error	you are lost
–	#	#	–	–	#	#	#	Memory pair 0, Slot B error	Pull out module in question, clean. Replace.
–	#	#	–	–	#	#	–	Memory pair 0, Slot A error	Pull out module in question, clean. Replace.
–	#	#	–	–	#	–	#	Memory pair 1, Slot B error	Pull out module in question, clean. Replace.
–	#	#	–	–	#	–	–	Memory pair 1, Slot A error	Pull out module in question, clean. Replace.
–	#	#	–	–	–	#	#	Memory pair 2, Slot B error	Pull out module in question, clean. Replace.
–	#	#	–	–	–	#	–	Memory pair 2, Slot A error	Pull out module in question, clean. Replace.
–	#	#	–	–	–	–	#	Memory pair 3, Slot B error	Pull out module in question, clean. Replace.
–	#	#	–	–	–	–	–	Memory pair 3, Slot A error	Pull out module in question, clean. Replace.
–	#	#	#	#	#	–	#	No memory found	Install memory
#	–	–	–	–	–	–	–	Unknown I/O device	Pull out all unnecessary devices and reboot
#	–	–	–	–	–	–	#	Error while trying to boot from SCSI device	Check SCSI cabling, termination and drives
–	#	–	–	–	–	–	#	Error while trying to boot from LAN	Check network cabling

#	-	-	-	-	-	-	#	Error trying to access Console Keyboard	Check HIL cabling, keyboard
#	-	-	-	-	#	-	-	Error while trying to access Console on COM1	Check cable and terminal [settings]
#	-	-	-	-	#	-	#	Error while trying to access Console on COM2	Check cable and terminal [settings]
#	-	-	-	-	#	#	-	Error while trying to access Parallel port	Bad luck
#	-	-	-	-	#	#	#	Error on SGC Slot 1	Clean card, maybe try another one
#	-	-	-	#	-	-	#	Unable to initialize EISA	Remove EISA card, backplane, clean both, reset
#	-	#	#	-	-	-	#	Error when reading from EEPROM	Switch off, pull cord, restart
#	-	#	#	-	-	#	-	Unexpected interrupt during PDC execution	Switch off, pull cord, restart
#	-	#	#	-	-	#	#	No working console found	Attach one
#	-	#	#	-	#	-	-	HPMC handling initiated	?
#	-	#	#	-	#	-	#	HPMC due to cache error	Switch off and reboot, if problem persists cache is probably defect. Replace CPU or motherboard.
#	-	#	#	-	#	#	-	HPMC due to memory error.	Switch off and reboot. Re-seat/replace memory.
#	-	#	#	-	#	#	#	HPMC due to bus error.	Switch off and reboot, if problem persists core is probably defect. Replace CPU or motherboard.
#	-	#	#	#	-	-	-	Nested HPMC occurred.	Switch off and reboot. (very bad)
#	-	#	#	#	-	-	#	Error while writing to EEPROM.	?
#	-	#	#	#	-	#	-	Unable to determine valid Processor Speed.	?
#	-	#	#	#	-	#	#	ROM Checksum error.	?
#	-	#	#	#	#	-	#	Illegal Processor Speed/Clock Ratio sensing.	?
#	-	#	#	#	#	#	#	Bad Memory Hardware.	?

2.11.4 HP 9000 715 (Mirage)

These codes apply to HP 9000 715/64, 80 and 100 and possibly other 700 workstations, including the HP 9000 725. Taken from the Model 715 Owner's Guide,

Table 2.36: # means LED is on or flashing, / means LED is either on or off.

8	7	6	5	4	3	2	1	Error Message	Solution
	#						#	CPU Error	?
		#				#	#	Fatal Error	?
		#					#	RAM Test Error	?
	#					#		Cache Error	?
	#				#			FP Coprocessor Error	?
		#			#			Fatal Coprocessor Error	?

#			#					I/O Device Error	?
#						#	#	ROM Checksum Error	?
		#		#	#			HPMC Error	Switch Machine off, reboot. Could indicate failure of a core component
		#				#		HPMC due to Cache Error	Switch Machine off, reboot. Indicates drastic failure in cache subsystem. If possible, replace cache/CPU module
		#			#		#	HPMC due to Bus Error	Switch Machine off, reboot.
		#			#	#	#	HPMC due to Memory Error	Switch Machine off, take the RAM out. Figure out, which module is broken.
#	#		#				#	Console Initialization Error	Look if keyboard/serial console cable is attached properly.
		#		#		#		No working console found.	"
#	#		#			#		No bootable device found.	Install one, check PATHs
#	#				#	#		InitializationError	?

2.11.5 720/730/750 (Snakes)

These codes apply to HP 9000 720, 730 and 750. Taken from the Owner's Guide,

Table 2.37: #- LED is on or flashing, /- LED is either on or off

8	7	6	5	4	3	2	1	Error Message	Solution
			#	/	/	/	/	CPU Error	Replace processor board
		#		/	/	/	/	CPU Error	Replace processor board
		#	#	/	/	/	/	CPU Error	Replace processor board
	#			/	/	/	/	CPU Error	Replace processor board
	#	#						RAM Error	Replace SIMM card in slot A1
	#	#					#	RAM Error	Replace SIMM card in slot A2
	#	#				#		RAM Error	Replace SIMM card in slot B1
	#	#				#	#	RAM Error	Replace SIMM card in slot B2
	#	#			#			RAM Error	Replace SIMM card in slot C1
	#	#			#		#	RAM Error	Replace SIMM card in slot C2
	#	#			#	#		RAM Error	Replace SIMM card in slot D1
	#	#			#	#	#	RAM Error	Replace SIMM card in slot D2
#		#	#			#		I/O Error	Replace I/O Card
#		#	#		#		#	CPU Error	Replace processor board
#		#	#		#	#		Error	Replace processor board <i>or</i> on SIMM
#		#	#		#	#	#	Error	Replace processor board <i>or</i> I/O card
#		#	#	#			/	Error	Replace processor board <i>or</i> I/O card

2.11.6 HP 9000 735/755

These codes apply to HP 9000 735 and 755. From the Service manual, supplied by Greg Fruth.

The codes mean different things depending on what state the machine is in. There are codes for the Selftest, the PDC (Processor Dependent Code), the ISL (Initial System Loader) and HP-UX (that's the

order in which they run).

- LED is on or flashing - - means LED is off.

Selftest LED Codes
#####

LED #	FRU	Error
87654321		

---#---	Processor Board	CPU Diagnose Register
---#--#-		CPU Basic Functions
---#--##		CPU ALU & Branch
---#-#--		CPU Arithmetic Conditions
---#-#-#		CPU Bit Operations
---#-##-		CPU Arithmetic Side Effects
---#-###		CPU Control Registers
---##---		CPU External Interrupts
---##--#		CPU Shadow Registers
---##-##		TLB Initialization
--#----#		Cache Data Line
--#---#-		Cache Address Line
--#---##		Instruction Cache RAM
--#--#--		Data Cache RAM
--#--#-#		Cache Tag Compare
--#--##-		Cache Errors
--#--###		Cache Configuration
--#-#---		Cache Flush
--#-#--#		Cache Byte Transaction
--#-#-#-		Instruction Cache Miss

--#-#-##		Data Cache Miss
--#-##--		Cache Done
--##---#		Memory Interface EIR
--##--#-		Memory Interface HPMC
--##-##		Memory Interface
--##-#--		Memory Interface Invalid Address
--##-#-#		Memory Interface Single Bit Error
--##-##-		Memory Interface Double Bit Error
--##-###		Memory Interface Diagnose Register
-#-----#		Floating Point Registers
-#-----#-		Floating Point Instructions
-#----##		Floating point Traps
-#-#---#	EISA Interface Controller	EISA Init
-#-#--#-		EISA ADDR Test
-#-#--##		ADDR Test Failure
-#-#-#--		EISA Pattern Test
-#-#-#-#		EISA Pattern Test Failure
-#-#####		RAM CHECKSUM Failure
-##-----	Memory	RAM Slot 5B (J100) Error
-##-----#		RAM Slot 4B (J102) Error
-##----#-		RAM Slot 3B (J104) Error
-##---##		RAM Slot 2B (J106) Error
-##--#--		RAM Slot 1B (J108) Error
-##--#-#		RAM Slot 0B (J110) Error
-###-----		RAM Slot 5A (J101) Error

```

-###---#          RAM Slot 4A (J103) Error
-###--#-         RAM Slot 3A (J105) Error
-###--##        RAM Slot 2A (J107) Error
-###-#--        RAM Slot 1A (J109) Error
-###-#-#        RAM Slot 0A (J111) Error
-###-###        RAM Configuration & Test In Progress
-#####-#       No RAM Found
-#####-        Non-Destructive RAM Test
-#####         RAM Configuration & Test
#-----        Processor Board Unknown I/O Device
#-----#       Single-Ended SCSI Init
#-----#-      LAN Init
#-----##      HIL Init
#----#--       RS232 Port A Init
#----#-#       RS232 Port B Init
#----##-       Parallel Port Init
#---#---       SGC Slot 0 Graphics Init
#---#--#       EISA Card EISA Slot Init
#--##---       FDDI Slider Board FDDI Init
#--##--#       Processor Board Fast Wide SCSI Init
    
```

```

#####
PDC LED Codes
#####
LED #
87654321      Status
=====
    
```

#-#----#	Destructive Memory Init
#-#---#-	Non-Destructive Memory Init
#-#---##	Console Selection
#-#--#--	Boot Device Selection
#-#--#-#	Autoselection Failure to Find Boot Device
#-#--##-	Launching IPL
#-#--###	TOC Handler Entered
#-#-#---	Branching to OS TOC Handler
#-#-#--#	Branching to OS HPMC Handler
#-#-#-#-	EISA Subsystem Init
#-#-#-##	Setting Up Default EISA Config
#-#-#-#-	At Least One Selftest Failed (Service Mode)
#-##---#	Error when reading EEPROM
#-##--#-	Unexpected Interrupt
#-##--##	No Console Located
#-##-#--	HPMC Handling Init
#-##-#-#	HPMC Due to Cache Error
#-##-##-	HPMC Due to Memory Error
#-##-###	HPMC Due to Bus Error
#-###---	Nested HPMC Detected
#-###--#	Error Writing EEPROM
#-###-#-	Unable to Determine Valid Processor Speed
#-####--	Processor Speed Sensing
#-####-#	Problem Calculating Memory Control Values
#-#####	Bad Memory Hardware

```

#####
ISL LED Codes
#####
LED #
87654321      Status
=====

-----      ISL Executing.

-----#      ISL is Autobooting from the Autoexec file.

-----#-      ISL Cannot Find Autoexecute file.

-----##      No Console Found. ISL Autobooting.

-----#-#      Directory of utilities is too large.

-----##-      Autoexec File is Inconsistent.

---#--#-      Error when reading Autoexec File.

---#--##      Error when reading from Console.

---#-#--      Error when writing to Console.

---#-#-#      Not an ISL Command or Utility.

---#-##-      Utility File Header Inconsistent: Invalid System ID.

---#-###      Error when reading Utility File Header.

---##---      Utility File Header Inconsistent: Bad Magic Number.

---##--#      Utility Would Overlay ISL in Memory.

---##-#-      Utility Requires More Memory Than Is Configured.

---##-##      Error when reading Utility Into Memory.

---###--      Incorrect Checksum: Reading Utility Into Memory.

---###-#      System Console Needed.

---####-      Internal Inconsistency: Invalid Boot Device Class.

--#----#      Destination Memory Address of Utility is Invalid.

--#----#-      Internal Inconsistency pdc_cache entry

```

```
--#---##      Internal Inconsistency: IODC ENTRY_INIT
--#--#--      Internal Inconsistency: IODC ENTRY_INIT Console
--#--#-#      Internal Inconsistency: IODC ENTRY_INIT Boot Device
--#--##-      Utility File Header Inconsistent: Bad aux_id
--#--###      Bad Utility File Type
```

```
#####
HP-UX Kernel LED Codes
#####
LED #
87654321      Status
=====
```

```
###-----      Kernel Loaded and Initialization Begun.
####---#       Kernel Has Entered main().
####--#-       Kernel Is About to Configure I/O System.
####-#--       Kernel Is About to Mount Root File System.
####-##-       Kernel Is About to Set Up Page-Out Daemon.
#####---      Kernel is About to Start the "INIT" Process.
-----        Shutdown In Process.
-----#--      TOC Dump.
---#-----     HPMC Dump.
--#-----#     Operating System Executing with Load
                Indicator X.
```

Once the machine is into HP-UX, the top 4 amber LEDs (1-4) assume the meanings given by the hieroglyphics next to the LEDs themselves (network in/out, net receive, SCSI, heartbeat). The bottom 4 LEDs (5-8) show the system load factor.

2.11.7 HP Visualize B-Class

These codes apply to HP Visualize B132L, B160L and B180L. From the Owner's Guide.

Table 2.38: #- LED is on or flashing, _- LED is off.

LED value	RS-232 range	Description
-----------	--------------	-------------

_ _ _ #	7401	No memory found FAULT.
_ _ # #	7000-7F00	Memory Error FAULT. (sys console indicates which board)
_ # _ _	1030-4099	Processor board FAULT.
_ # _ #	5000-500F, 8000-8FFF, CD00-CDFE	I/O System FAULT
_ # # _	8500, 8501, 8C00-8CFF	Backplane FAULT (incl. PCI).
_ # # # # _ _ _	Any	INITIALIZATION and TESTING. (alternating 1000, 0111,...)
# _ _ #	Any not in this table	Unknown FAULT.
# _ # _	CBF0-CBFE, 1001	HPMC FAULT (very bad).
# # _ #	A088-A0FF	No console/IPL error FAULT.
# # # #		If remains for longer than 1s after power-on: processor board FAULT.

2.11.8 HP Visualize C-Class

These codes apply to HP Visualize C-Class workstations with LED front panels.

Table 2.39: # – LED is on or flashing, _ – LED is off.

LED value	RS-232 range	Description
_ _ _ #	7500	No memory found FAULT.
_ _ # _	7501, 7502	Not enough memory found FAULT.
_ _ # #	7000-7D0A	Processor Board/Memory Error FAULT. (sys console indicates which board)
_ # _ _	1030-4071	Processor board FAULT.
_ # _ #	5000-500F, 8000-8FFF, CD00-CDFE	I/O System FAULT
_ # # _	CD1E, CDEF, CDD0	Backplane FAULT (incl. PCI).
_ # # # # _ _ _	Any	INITIALIZATION and TESTING. (alternating 1000, 0111,...)
# _ _ #	Any not in this table	Unknown FAULT.
# _ # _	CBF0-CBFE, 1001	HPMC FAULT (very bad).
# # _ #	A000-A0C0	No console/IPL error FAULT.
# # # #		If remains for longer than 1s after power-on: processor board FAULT.

Chapter 3

PA-RISC Computer Systems

3.1 Overview

HP produced many different PA-RISC computers in the HP 9000 Unix systems between the 1980s and 2000s.

Different types of PA-RISC computers were available: HP 9000 700 and HP Visualize workstations, HP 9000 800 servers, “lettered” and Integrity servers, until PA-RISC and Itanium converged in the 2000s.

There were third-party PA-RISC computers in the 90s and many niche PA-RISC products like VME boards and analyzers, portable computers used for scientific, industrial and military uses. PA-RISC computers were sold over a long timeline and often benchmarked against SPEC.

3.1.1 HP 9000 700 Workstations

Many different PA-RISC workstations were sold in the 1990s, from small 712, 715 and B-Class desktops to heavy 735, 755 and powerful C-Class workstations.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
705	PA-7000 35 MHz	96 KB	64 MB	ASP	None	HP-UX, Linux, OpenBSD
710	PA-7000 50 MHz	96 KB	64 MB	ASP	None	HP-UX, Linux, OpenBSD
712/60	PA-7100LC 60 MHz	64 KB	128 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
712/80	PA-7100LC 80 MHz	256 KB	128 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
712/100	PA-7100LC 100 MHz	256 KB	192 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/33	PA-7100 33 MHz	128 KB	192 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/50	PA-7100 50 MHz	128 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/75	PA-7100 75 MHz	512 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/80	PA-7100LC 80 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/100XC	PA-7100LC 100 MHz	1 MB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
720	PA-7000 50 MHz	384 KB	272 MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD
725/50	PA-7100 50 MHz	128 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
725/75	PA-7100 75 MHz	512 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
725/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
730	PA-7000 66 MHz	384 KB	272 MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD

735/99	PA-7100 99 MHz	512 KB	400 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
735/125	PA-7150 125 MHz	512 KB	400 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
750	PA-7000 66 MHz	512 KB	768 MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD
755/99	PA-7100 99 MHz	512 KB	768 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
755/125	PA-7150 125 MHz	512 KB	768 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD

3.1.2 Visualize workstations

HP moved PA-RISC workstations to **Visualize** branding in the later 1990s with lettered model names **B**, **C** and **J** marketed for graphical and technical computing.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
B132L	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B132L+	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B160L	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B180L+	PA-7300LC 180 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B1000	PA-8500 300 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
B2000	PA-8500 400 MHz	1.5 MB	4 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
B2600	PA-8600 500 MHz	1.5 MB	4 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C100	PA-7200 100 MHz	512 KB	1 GB	U2	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C110	PA-7200 120 MHz	512 KB	1 GB	U2	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C132L	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	2 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C160L	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	2 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C160	PA-8000 160 MHz	1 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C180	PA-8000 180 MHz	2 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C200	PA-8200 200 MHz	1.5 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C240	PA-8200 236 MHz	4 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C360	PA-8500 367 MHz	1.5 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C3000	PA-8500 400 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD

C3600	PA-8600 552 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3650	PA-8700 625 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3700	PA-8700 750 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3750	PA-8700+ 875 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C8000	2 PA-8800/ 2 PA-8900 0.9-1.1 GHz	3 MB L1 32 MB L2/ 64 MB L2	32 GB	zx1	PCI-X, PCI, AGP	HP-UX, Linux
J200	1-2 PA-7200 100 MHz	512 KB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J210	1-2 PA-7200 120 MHz	512 KB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J210XC	1-2 PA-7200 120 MHz	2 MB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J280	PA-8000 180 MHz	2 MB	2 GB	UTurn	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J282	1-2 PA-8000 180 MHz	2 MB	2 GB	UTurn	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J2240	1-2 PA-8200 236 MHz	4 MB	4 GB	UTurn	PCI, EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
J5000	1-2 PA-8500 440 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J5600	1-2 PA-8600 552 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6000	1-2 PA-8600 552 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6700	1-2 PA-8700 750 MHz	2.25 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6750	1-2 PA-8700+ 875 MHz	2.25 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J7000	1-4 PA-8500 440 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J7600	1-4 PA-8600 552 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
P500 P600 P700C	1-2 Intel Pentium III	0.5 MB	768 MB	440BX	PCI, ISA, AGP	Windows NT, Linux, others
X500 X550	1-2 Intel Pentium III	1.0 MB	2 GB	440GX	PCI, ISA, AGP	Windows NT, Linux, others
p733 p800 x733 x800 p1.0 x1.0	1-2 Intel Pentium III	256 KB	4 GB	RCC	PCI, AGP	Windows NT, Linux, others

3.1.3 PA-RISC notebooks

Some special portable PA-RISC workstations were produced by third-party vendors for military and measurement contracts, based on HP PA-RISC workstations.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
RDI PrecisionBook 132	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 160	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 180	PA-7300LC 180 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 60 MHz	64 KB	128 MB	LASI	PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 80 MHz	256 KB	128 MB	LASI	PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
SAIC Talon	PA-7100LC 60 MHz	64 KB	128 MB	LASI	PCMCIA EISA, VME	HP-UX, Linux, NetBSD, OpenBSD
Hitachi 3050RX/100C	Hitachi PA/50L	12 KB	80 MB	Other		HI-UX/WE2

3.1.4 HP 9000 800 and Early Servers

HP 9000 800 are the original PA-RISC servers with distinct architecture and deskside cases. The 500 were the original “HP 9000” predecessor to PA-RISC.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
520 (9020)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX, HP BASIC
530 (9030)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX
540 (9040)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX
550 (9050)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX
635SV	NS-1 30 MHz	128 KB	112 MB	SIU	CIO	HP-UX, HPBSD, Mach 3/UX, Chorus
645SV	NS-2 27.5 MHz	256 KB	112 MB	SIU	CIO	HP-UX
808	PCX	32 KB	32 MB	SPI	HP-PB	HP-UX
815	PCX	32 KB	56 MB	SPI	HP-PB	HP-UX
822	NS-2 25 MHz	32 KB	128 MB	SIU	HP-PB	HP-UX
825	NS-1 25 MHz	16 KB	112 MB	SIU	CIO	HP-UX
832	NS-2 30 MHz	128 KB	128 MB	SIU	HP-PB	HP-UX
835 834	NS-1 30 MHz	128 KB	112 MB	SIU	CIO	HP-UX, HPBSD, Mach 3/UX, Chorus
840	TS-1 8 MHz	128 KB	112 MB	CTB	CIO	HP-UX
842	PCX 32 MHz	1 MB	256 MB	SPI	HP-PB	HP-UX
845	NS-2 27.5 MHz	256 KB	112 MB	SIU	CIO	HP-UX

850	NS-1 27.5 MHz	128 KB	256 MB	SIU	CIO	HP-UX
852	PCX 50 MHz	1 MB	256 MB	SPI	HP-PB	HP-UX
855	NS-2 27.5 MHz	256 KB	256 MB	SIU	CIO	HP-UX
860	NS-2 27.5 MHz	1 MB	256 MB	SIU	CIO	HP-UX
865	PCX 50 MHz	768 KB	512 MB	SPI	CIO	HP-UX
10000 Apollo	1-4 PRISM 18 MHz	192 KB	128 MB	Apollo	VME, ISA	Domain OS
E25	PA-7100LC 48 MHz	64 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E35	PA-7100LC 64 MHz	256 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E45	PA-7100LC 80 MHz	256 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E55	PA-7100LC 96 MHz	1 MB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
F10	PA-7000 32 MHz	96 KB	768 MB	Viper	HP-PB	HP-UX
F20	PA-7000 48 MHz	128 KB	768 MB	Viper	HP-PB	HP-UX
F30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
G70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX
H20	PA-7000 48 MHz	128 KB	768 MB	Viper	HP-PB	HP-UX
H30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
H70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX
I30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
I40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
I50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX

I60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
I70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX

3.1.5 Lettered Servers

The “lettered” PA-RISC servers include tower computers in D and E-Class and desktide and cabinet systems in the K-Class. Formally HP 9000 800 (server) series, these had lettered model names like the Visualize workstations.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
A180	PA-7300LC 180 MHz	128 KB	2 GB	LASI	GSC, PCI	HP-UX, Linux, NetBSD, OpenBSD
A180C	PA-7300LC 180 MHz	128 KB L1 1 MB L2	2 GB	LASI	GSC, PCI	HP-UX, Linux, NetBSD, OpenBSD
A400	PA-8x00	depends	2 GB	Astro	PCI	HP-UX, Linux
A500	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
D200	PA-7100LC 75 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D210	PA-7100LC 100 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D220	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D230	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D250	1-2 PA-7200 100 MHz	512 KB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D260	PA-7200 120 MHz	2 MB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D270	1-2 PA-8000 160 MHz	1 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D280	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D300	PA-7100LC 75 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D310	PA-7100LC 100 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D320	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D330	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D350	1-2 PA-7200 100 MHz	512 KB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D360	2 PA-7200 120 MHz	2 MB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D370	1-2 PA-8000 160 MHz	1 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D380	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D390	1-2 PA-8200 240 MHz	4 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux

K100	PA-7200 100 MHz	512 KB	512 MB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K200	1-4 PA-7200 100 MHz	512 KB	4 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K210	1-4 PA-7200 120 MHz	512 KB	4 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K220	1-4 PA-7200 120 MHz	2 MB	4 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K250	1-4 PA-8000 160 MHz	2 MB	4 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K260	1-4 PA-8000 180 MHz	2 MB	4 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K370	1-6 PA-8200 200 MHz	4 MB	4 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K380	1-6 PA-8200 240 MHz	4 MB	4 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K400	1-4 PA-7200 100 MHz	512 KB	2 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K410	1-4 PA-7200 120 MHz	512 KB	2 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K420	1-4 PA-7200 120 MHz	2 MB	8 GB	U2	HSC, HP- PB	HP-UX, Linux, NetBSD, OpenBSD
K450	1-4 PA-8000 160 MHz	2 MB	8 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K460	1-4 PA-8000 180 MHz	2 MB	8 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K570	1-6 PA-8200 200 MHz	4 MB	8 GB	UTurn	HSC, HP- PB	HP-UX, Linux
K580	1-6 PA-8200 240 MHz	4 MB	8 GB	UTurn	HSC, HP- PB	HP-UX, Linux
L1000	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
L1500	1-2 PA-8x00	depends	8 GB	Stretch	PCI	HP-UX
L2000	1-4 PA-8x00	depends	16 GB	Astro	PCI	HP-UX, Linux
L3000	1-4 PA-8x00	depends	16 GB	Stretch	PCI	HP-UX, Linux
N4000	1-8 PA-8x00	depends	32 GB	Stretch	PCI	HP-UX, Linux
N4000	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
R380	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
R390	1-2 PA-8200 240 MHz	4 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux

3.1.6 Integrity (rp) Servers

HP called its PA-RISC servers *rp* Integrity series around the 2000s. All are 64-bit PA-RISC systems for rack-mounting (19") in data centers.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
rp2400 rp2430 rp2405	PA-8x00	depends	2 GB	Astro	PCI	HP-UX, Linux

rp2450 rp2470 rp2405	I-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
rp3410	PA-8800 800 MHz	3 MB L1 32 MB L2	6 GB	ZXI	PCI-X	HP-UX, Linux
rp3440	I-2 PA-8x00 800 MHz- 1.0 GHz	3 MB L1 32 MB L2	32 GB	ZXI	PCI-X	HP-UX, Linux
rp4410	I-2 PA-8x00 800 MHz- 1.0 GHz	3 MB L1 32 MB L2	128 GB	ZXI	PCI-X	HP-UX
rp4440	I-4 PA-8x00 800 MHz- 1.0 GHz	3 MB L1 32 MB L2	128 GB	ZXI	PCI-X	HP-UX
rp5400	I-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
rp5430	I-2 PA-8x00	depends	8 GB	Stretch	PCI	HP-UX
rp5450	I-4 PA-8x00	depends	16 GB	Astro	PCI	HP-UX, Linux
rp5470	I-4 PA-8x00	depends	16 GB	Stretch	PCI	HP-UX, Linux
rp7400	I-8 PA-8x00	depends	32 GB	Stretch	PCI	HP-UX, Linux
rp7405	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp7410	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp7420	I-8 PA-8800 900 MHz- 1.0 GHz	3 MB L1 32 MB L2	64 GB	SX1000	PCI	HP-UX
rp7440	I-8 PA-8900 1.7 GHz	3 MB L1 64 MB L2	128 GB	SX2000	PCI-X	HP-UX
rp8400 rp8410	2-16 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp8420	I-16 PA-8x00 800 MHz- 1.1 GHz	3 MB L1 32 MB L2	256 GB	SX1000	PCI-X	HP-UX
rp8440	I-16 PA-8900 1.1 GHz	3 MB L1 64 MB L2	256 GB	SX2000	PCI-X	HP-UX

3.1.7 HP Itanium Computers

HP produced three Itanium workstations before dropping Unix workstations, making these the last and probably fastest HP-UX workstations (that also run Windows).

System	CPU	Cache	RAM	Design	Expansion	Operating systems
i2000	I-2 Itanium 733-800 MHz	<i>varies</i>	16 GB	82460GX	PCI, AGP	HP-UX, Linux, FreeBSD, Windows, OpenVMS
ZX2000	Itanium 2 900 MHz-1.5 GHz	<i>varies</i>	8 GB	ZXI	PCI-X, AGP	HP-UX, Linux, FreeBSD, Windows, OpenVMS
ZX6000	Itanium 2 900 MHz-1.5 GHz	<i>varies</i>	24 GB	ZXI	PCI-X, AGP	HP-UX, Linux, FreeBSD, Windows, OpenVMS

HP also released a line of Itanium-based servers in the rack-mountable **Integrity rx** line.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
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rx1600	1-2 Itanium 2 1.0 GHz	<i>varies</i>	16 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx1620	1-2 Itanium 2 1.3-1.6 GHz	<i>varies</i>	16 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2600	1-2 Itanium 2 1.0-1.5 GHz	<i>varies</i>	24 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2620	1-2 Itanium 2 1.3-1.6 GHz	<i>varies</i>	32 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2660	1-2 Itanium 2 1.4-1.6 GHz	<i>varies</i>	32 GB	ZX2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx3600	1-2 Itanium 2 1.4-1.6 GHz	<i>varies</i>	192 GB	ZX2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx4610	2-4 Itanium 733-800 MHz	<i>varies</i>	64 GB	ZX1	PCI	HP-UX, Linux, Windows
rx4640	1-4 Itanium 2 1.1-1.6 GHz	<i>varies</i>	64 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx5670	1-4 Itanium 2 1.3-1.5 GHz	<i>varies</i>	96 GB	ZX1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx6600	1-4 Itanium 2 1.4-1.6 GHz	<i>varies</i>	192 GB	ZX2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx7620	2-8 Itanium 2 1.1-1.5 GHz	<i>varies</i>	64 GB	SX1000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx7640	2-8 Itanium 2 1.4-1.6 GHz	<i>varies</i>	256 GB	SX2000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx8620	2-16 Itanium 2 1.1-1.6 GHz	<i>varies</i>	256 GB	SX1000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx8640	2-16 Itanium 2 1.4-1.6 GHz	<i>varies</i>	512 GB	SX2000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx9610	4-16 Itanium 733-800 MHz	<i>varies</i>	128 GB	AzuzA	PCI-X	HP-UX
Integrity Superdome SD16A, SD32A, SD64A	1-64 Itanium 2	<i>varies</i>	2TB	SX1000	PCI X, PCIeX	HP-UX, Linux Windows, OpenVMS
Integrity Superdome SD16B, SD32B, SD64B	1-64 Itanium 2	<i>varies</i>	2TB	SX2000	PCI X, PCIeX	HP-UX, Linux Windows, OpenVMS

3.1.8 VME and Scientific

HP has a long tradition of measurement and control system and released many integrated PA-RISC VME and VXI boards and scientific systems, based on HP 9000 700s workstations.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
742i/50	PA-7100 50 MHz	128 KB	64 MB	ASP	VME	HP-UX, Linux, NetBSD, OpenBSD
742rt	PA-7100 50 MHz	128 KB	64 MB	ASP	VME	HP-RT
743i/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	GSC-M, VME	PMC, HP-UX, Linux, NetBSD, OpenBSD

V743/64 VXI E1497A	PA-7100LC 64 MHz	256 KB	128 MB	LASI	GSC-M, PMC, VXI	HP-UX, HP-RT, probably others
743i/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
743rt	PA-7100LC 100 MHz	256 KB	256 MB	LASI	GSC-M, PMC, VME	HP-RT
V743/100 VXI E1498A	PA-7100LC 100 MHz	256 KB	128 MB	LASI	GSC-M, PMC, VXI	HP-UX, HP-RT, probably others
744/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
744rt/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	GSC-M, PMC, VME	HP-RT
744/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
744/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	GSC-M, PMC, VME	HP-RT
745i/50	PA-7100 50 MHz	128 KB	128 MB	ASP	EISA, VME	HP-UX, Linux, NetBSD, OpenBSD
745i/100	PA-7100 100 MHz	512 KB	256 MB	ASP	EISA, VME	HP-UX, Linux, NetBSD, OpenBSD
745/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
745/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
747i/50	PA-7100 50 MHz	128 KB	128 MB	ASP	EISA, SGC, VME	HP-UX, Linux, NetBSD, OpenBSD
747i/100	PA-7100 100 MHz	512 KB	256 MB	ASP	EISA, SGC, VME	HP-UX, Linux, NetBSD, OpenBSD
748i/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
748i/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
748i/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
748i/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
16600A Agilent	PA-7300LC 150 MHz	64 KB	160 MB	LASI	Channel probes, measurement, emulation	HP-UX LOGIC, probably others
16700A 16700B Agilent	PA-7300LC 150 MHz	64 KB	160 MB 256 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others
16702A 16702B Agilent	PA-7300LC 150 MHz	64 KB	160 MB 256 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others
E4406A Agilent	PA-7300LC 150 MHz	64 KB	256 MB	LASI	mobile dev	HP-RT

3.1.9 Mainframe

These are large enterprise servers for computing and large databases, with a large range of expansion, CPUs, memory and storage options. Some could be clustered.

System	CPU	Cache	RAM	Design	Expansion	Operating systems
870	1-4 PCX 50 MHz	1 MB	768 MB	SPI	CIO	HP-UX
890	1-4 PCX? 60 MHz	4 MB	2.0 GB	Viper	HP-PB	HP-UX
T500	1-12 PA-7100 90 MHz	2 MB	3.75 GB	Viper	HP-PB	HP-UX
T520	1-14 PA-7150 120 MHz	2 MB	3.75 GB	Viper	HP-PB	HP-UX
T600	1-12 PA-8000 180 MHz	2 MB L1 8 MB L2	3.75 GB	Viper	HP-PB	HP-UX
V2200	4-16 PA-8200 200 MHz	4 MB	16 GB	HyperPlane	PCI	HP-UX
V2250	4-16 PA-8200 240 MHz	4 MB	16 GB	HyperPlane	PCI	HP-UX
V2500	2-32 PA-8500 440 MHz	1.5 MB	32 GB	HyperPlane	PCI	HP-UX
V2500 Cluster	4-128 PA-8500 440 MHz	1.5 MB	128 GB	HyperPlane	PCI	HP-UX
V2600	2-32 PA-8600 552 MHz	1.5 MB	32 GB	HyperPlane	PCI	HP-UX
V2600 Cluster	4-128 PA-8600 552 MHz	1.5 MB	128 GB	HyperPlane	PCI	HP-UX
Convex SPP1000/CD	2-16 PA-7100 100 MHz	2 MB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1000/XA	2-8 PA-7100 100 MHz	2 MB	2 GB	Crossbar	SBus	SPP-UX
Convex SPP1000/XA Cluster	8-128 PA-7100 100 MHz	2 MB	32 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/CD	2-16 PA-7200 120 MHz	512 KB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/XA	2-8 PA-7200 120 MHz	512 KB	2 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/XA Cluster	8-128 PA-7200 120 MHz	512 KB	32 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/CD	2-16 PA-7200 120 MHz	2 MB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/XA	2-8 PA-7200 120 MHz	2 MB	2 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/XA Cluster	8-128 PA-7200 120 MHz	2 MB	32 GB	Crossbar	SBus	SPP-UX
HP/Convex SPP2000 S-Class	4-16 PA-8000 180 MHz	2 MB	16 GB	Crossbar	PCI	SPP-UX

HP/Convex SPP2000 X-Class Cluster	8-512 PA-8000 180 MHz	2 MB	512 GB	Crossbar	PCI	SPP-UX
HP/Convex SPP2200 X-Class Cluster	8-512 PA-8200 200 MHz	2 MB	512 GB	Crossbar	PCI	SPP-UX
Superdome SD16000, SD32000, SD64000	1-64 PA-8600 PA-8700	1.5 MB/ 2.25 MB	1TB	Cell	PCI-X	HP-UX, Linux
Superdome SD16A, SD32A, SD64A	1-64 PA-8800	3 MB L1 32 MB L2	2TB	sx1000	PCI X, PCIeX	HP-UX, Linux
Superdome SD16B, SD32B, SD64B	1-64 PA-8900	3 MB L1 64 MB L2	2TB	sx2000	PCI X, PCIeX	HP-UX, Linux
Stratus Continuum 400	L1/P2-L2/P8 PA-7100 PA-8000 PA-8500 PA-8600	1.5 MB	8 GB	Continuum	12 PCI	HP-UX, FTX
Stratus Continuum 600	L1/P4-L2/P8 PA-7100 PA-8000 PA-8500 PA-8600	0.5- 2 MB	4 GB	Continuum	6 slots	VOS, FTX
Stratus Continuum 1200	L1/P4-L4/P16 PA-7100 PA-8000 PA-8500 PA-8600	0.5- 2 MB	4 GB	Continuum	12-18 slots	VOS, FTX

3.1.10 Third Party

Several third party vendors sold PA-RISC workstations and servers mainly in Japan in the mid-1990s as part of the Precision RISC Organisation (PRO).

Vendor	Series	Class	CPU	Operating systems
Hitachi	3050RX	Workstations	Hitachi PA/50 PA-7100 PA-7100LC PA-7300LC	HI-UX/WE2
Hitachi	3050	Servers	PA-7100	HI-UX/WE2
Hitachi	9000V	HP 9000 OEM	various	HP-UX
Hitachi	SR2	Supercomputers	Hitachi HARP-1	HI-UX/MPP
Mitsubishi	MELCOM ME	HP 9000 OEM	PA-7000	HP-UX
NEC	TX7	HP 9000 OEM Custom NEC	PA-8000 PA-8200	HP-UX
NEC	NX7000	HP 9000 OEM	various	HP-UX
OKI	OKITAC	HP 9000 OEM	various	HP-UX
Samsung	SWS715	HP 9000 OEM	PA-7100	SS-UX

Pictures Hewlett Packard, scans from product brochures, from hpmuseum.net and 100obit.it

3.2 HP 9000 and PA-RISC Story

HP 9000 was a family of technical servers and workstations produced by HP between the 1980s and 2000s, which included several ranges of Unix computers: the HP 9000 700, 800 and others, based on HP PA-RISC, Itanium and other platform.

Both RISC and Unix were developed into products during the 1980s, moving from academia via industrial R&D to productization—at a time when much computing was still done on mainframes, minicomputers and time-sharing machines such as DEC PDP, VAX, IBM AS/400 and System/360.

HP 9000 and PA-RISC were HP's new line of products in that fledgling market in the early 1980s. This page focuses on the PA-RISC part of the story, divided into four periods from the 1980s to the 2000s that each featured distinct designs.

Phase	Workstations	Servers	Mainframes	Others
Prelude: Early 1980s	Other HP 9000 500 series			Other HP 9000 200, 300 series
Infancy: Late 1980s Phase I		HP 9000 800 840 to 870, 600		Other HP 9000 Apollo, 400
Growth: 32-bit 1990s Phase II	HP 9000 700 720-750, 705-725 US Navy DTC, TAC-3, TAC-4	HP 9000 800 F/G/H/I-Class	Mainframes 890	HP VME industrial 742, 745 ⁱ , 747 ⁱ Third party PRO Hitachi, NEC, Japan
Maturity: 90s hey-days Phase III	HP 9000 700 712 and 715 HP Visualize B/C/J-Class	HP 9000 800 E-Class Lettered servers A/D/K/L/N/R-Class	Mainframes Convex T/V-Class	HP VME industrial 743, 744, 745, 748 Portables SAIC, RDI, Hitachi
Decline: 64-bit 2000s Phase IV	HP Itanium zx workstations	HP Integrity rp servers HP Itanium rx servers	Mainframes Superdome	

This article attempts to unify all the different streams of HP 9000 and PA-RISC into a single story, with simplifications. Release dates of HP 9000 computers and market entry prices are listed in the PA-RISC Timeline. Much more details on HP 9000 PA-RISC systems are described in PA-RISC Computers.

Separate articles describe the history of PA-RISC operating systems, the era of PA-RISC processors as well as the age of PA-RISC information and OpenPA itself.

3.2.1 Prelude to PA-RISC

The prelude to PA-RISC computers took place during the early to mid-1980s, starting with the 1982 HP FOCUS computers.

In the early 1980s, HP worked on both Unix and RISC development and products. Before PA-RISC, the original HP 9000 series was released with the FOCUS-based 500 series (9020). In parallel, the Motorola 68000 were added as HP Unix workstations.

Other HP 9000

There were a few other computer series offered under the HP 9000 label before HP released PA-RISC computers. This includes early HP Unix platforms based on Motorola 68000 CISC processors, the

HP FOCUS line that preceded PA-RISC and HP 3000 minicomputers, which only later switched to PA-RISC.

HP 9000 200 were the earliest incarnations of HP Unix platforms, based on Motorola 68000. They started life as HP 9826 in 1981 and were soon followed by other “high-end technical desktops”, such as the HP 9836, 9816, 9920, 9817 and 9837H. HP renamed the series in the early 1980s to HP 9000 200 and the individual computers to HP 9000/220 and so on. The HP 9000 200 ran versions of HP-UX Unix.

The other series based on Motorola M68k processors were HP 9000 300, sold from the mid-1980s to the early 1990s as HP Unix platform. HP 9000 300 had a new, functional multi-box design for each computer, later used in first HP 9000 700 workstations. HP 9000 300 series used Motorola CISC processors from 68010 to 68040. Besides HP-UX, the 300 series were supported by a variety of BSD operating systems from the 1980s well into the 2010s, including the mythical 4.4BSD and the OpenBSD/hp300 and NetBSD/hp300 siblings.

HP 9000 500: HP 520 computers were the early-1980s predecessors of PA-RISC that started the HP 9000 series. HP 9000 500 were based on the proprietary HP 32-bit processor the HP FOCUS. First released in 1982, HP 9000/520, originally 9020, were quickly followed by HP 9000 530, 540 and 550 computers. Operating system support was limited to HP-UX, which on HP FOCUS allegedly was the first commercial Unix supporting a multi-processor, multi-user system.

HP 3000 were HP business minicomputers, first released in 1972, with MPE operating system, application stack and distinct customer base. For more information see 3000-MPE from hpmuseum.net and History of the HP 3000 from Bob Green.

3.2.2 Infancy (I)

The infancy of PA-RISC were the years between 1986 and the late 1980s with first PA-RISC processor and products, using an RISC architecture still in flux.

HP moved into the fledging microcomputer market in the late 80s with several differently positioned platforms. PA-RISC computers in the HP 9000 Series 800 were HP's RISC entry into that market. HP 9000 offerings with CISC processors were sold by HP in parallel for almost a decade. PA-RISC 9000 800 were initially offered as servers for business applications but quickly adapted by HP and customers for technical and engineering – as early workstations.

HP experimented with and developed several processor, fabrication and systems designs in the those late-1980s days with the HP 9000 800, setting the scene for later HP 9000 700.

Early RISC computers and 800s

HP 9000 800 servers were the original PA-RISC computers developed by HP in the 1980s and released in mid-1980s. They consisted of several computers based on 32-bit PA-RISC 1.0 and 1.1 processors and different designs. System architecture was rather divergent to later 700 workstations with different chipsets, buses and I/O devices. The HP 9000 700 series was introduced slightly later than the 800s, with a different, more workstation-centric focus.

- ◇ **Early 840 to 870:** First PA-RISC systems to market were early HP 9000 800 servers released between 1986 and 1990 with PA-RISC 1.0 processors. HP experimented with different concepts and designs for computers and processors in that phase, from TTL-based HP 9000/840 servers in 1986 to first CMOS-based HP 9000/842, 852, 865, 870 servers. First attempts were also made for lower-cost systems.

- ◇ There was a short-lived PA-RISC-based **HP 9000 600 series** in the late 1980s. The HP 90000/635SV and 645SV were supposedly server-only versions of the 800 series PA-RISC 1.0 HP 9000/835 and 845. Both were deskside server systems and ran HP-UX. The 600 series moniker was discontinued shortly after with servers taking the 800 and workstations the 700 series.

Due to their separate system design and usage, HP 9000 700 and 800 series used different HP-UX Unix versions for a long time until HP-UX 10.20. Support for 800 series in open source systems was always limited due to sparse documentation on their architecture. Series 800 PA-RISC servers carried over into the Lettered servers of the A/D/K/N classes that kept a divergent architecture to 700 and Visualize workstations, focused on multi-user business applications.

Other HP 9000

Just before releasing the HP 9000 700 line, HP bought **Apollo**, a technical computing market leader of the 80s, with their own PRISM (RISC)-based Domain 10000 workstations. Apollo Domain workstations were carried on for a few years under HP branding. HP integrated Apollo as their workstation business unit with Apollo co-branding on HP 9000 RISC workstations for a while, but Apollo products and technology were phased out soon after so HP could concentrate on PA-RISC.

HP 9000 400 were related to the HP 9000 300 series from the early 1980s but incorporated technology from acquired Apollo Computers. They were based on Motorola 68030 and 68040 processors and ran HP-UX and Domain/OS (Apollo Unix). HP 9000 400 were sold in parallel to 700 and 800 PA-RISC computers in the early 1990s and were widely supported by BSD and open source operating systems of that era. Designs, devices and peripherals were shared between Motorola 68000-based 400 series and PA-RISC 700 and 800 series, including SGC and EISA buses, SCSI controllers, HP-HIL and HP-IB peripherals and graphics.

From the late 1980s on, **HP 3000** moved to the PA-RISC platform and used systems that were closely based on the HP 9000 800 series. HP 3000 used PA-RISC actually earlier than the widely-popular HP 9000 700 workstation series. The first MPE for PA-RISC release was MPE/XL, the last MPE version was MPE/iX with limited Unix support and POSIX compliance. HP 3000 and MPE have been discontinued since.

3.2.3 Growth (II)

Much of the growth phase of HP 9000 and PA-RISC happened between 1990 and 1992. PA-RISC computers became very successful in the industry, and HP started differentiating its PA-RISC product ecosystem from large main-frame servers to small desktop workstations on Unix.

HP introduced a dedicated PA-RISC workstation line, the HP 9000 700 series, to segment PA-RISC computers from the 800 servers. Based on new PA-RISC 1.1 processors, the original HP 9000 workstation line-up consisted of HP 9000 “Snakes”, smaller systems (705/710) and technical desktops (715/725)

These first HP 9000 workstations were often used for Unix-based graphics, engineering and R&D. Some opening up of the tightly-controlled PA-RISC happened with the HP PRO organization and third-party systems so PA-RISC was not limited to HP anymore.

HP 9000 700 workstations

A large range of PA-RISC workstations was sold by HP with the HP 9000 700 series, from the 1990s on. The 700 series soon became popular 32-bit Unix RISC workstations and used HP's new processors like the PA-7000, PA-7100 and (later) PA-7100LC.

At that time, much technical computing centered on Unix and RISC workstations, superseding older CISC computers. The new workstations were often used for CAD, CAM and specialized software for HP-UX or Unix. HP acquired Apollo Computers around that time, so "Apollo" technology and name became part of some workstations like "HP Apollo 9000."

- ◇ **Snakes 720/730/750:** HP 9000 720, 730 and 750 from 1991 were the first dedicated PA-RISC workstations on the PA-RISC 1.1 PA-7000 processor. They used rather large and heavy deskside and desktop cases with interlocking modules of backplanes and I/O boards. 730 and 750 were improved on a year later by the powerful PA-7100/PA-7150 powered HP 9000/735 and 755 workstations, among the fastest PA-RISC computers of the time.
- ◇ **Pizzabox 705/710:** The design of the original "Snake workstations" was integrated into smaller, pizza-box style desktop workstations with the HP 9000 705 and 710 with similar architecture but limited I/O and performance. 705 and 710 were an early foray into pared-down "budget" workstations, with full functionality but compromises on performance and I/O, a concept revised later in mainstream PCs (and the HP 9000 712 workstations).
- ◇ **Desktop 715/725:** Soon after the original workstations, in 1991 a range of technical workstations was released with the PA-7100 and ASP based HP 9000/715 and HP 9000 725 in /33 (horrible) to /75 variants. These featured more standardized hardware and expandability and I/O options for technical users, packaged into a more "normal" desktop housing not dissimilar to contemporary PCs. They were rather popular.

PA-RISC 700 workstations gained wide popularity in engineering, industrial and academic fields during the 1990s. During that time, PA-RISC and 700 workstations traded the "performance crown" of Unix and RISC computers frequently with DEC Alpha architecture. PA-RISC workstations were developed by the HP Workstation Systems Division in Ft. Collins, Colorado, USA. HP developed almost all PA-RISC CPUs since 1986 inhouse, in its VLSI Technology Center (VTC) and Systems & VLSI Technology Operation (SVTO), also in Fort Collins.

HP 9000 800 servers

F/G/H/I-Class: These were the second generation HP 9000 800 servers from the early-1990s. The HP 9000 Nova servers share a similar, distinct 32-bit PA-RISC design. They had wildly diverse configurations for server applications from the small F10 to the large I70.

HP 9000 890: 890 servers were an early iteration of the T-Class mainframe architecture, with later T500/T600 being updated successors. Even later, the 890/T-Class system design was discontinued in favor of more flexible Superdome systems.

VME and Industrial

HP sold PA-RISC VME computers as HP 9000 740 series from the early to late 1990s. They were used for industrial, scientific and military data measurement and real time control applications, as single-board computers utilized the industrial-grade VME bus. Processors used were 32-bit PA-RISC PA-7100, PA-7100LC and PA-7300LC with HP LASI and ASP chipsets and custom HP VME design.

Operating systems for HP 9000 740 were HP-UX for Unix and HP-RT for real-time applications, with some support in open Source operating systems. They were used in a very wide variety of applications for industrial and scientific control and measurement, including by the US military.

- ◇ **First-generation VME** computers from the early 1990s were PA-7100 ASP-based designs, the HP 9000/742i single-board computer, integrated into HP 9000/745i and 747i computers. They were closely based on the HP 9000 715 technical workstation, repackaged into single-board VME computers.
- ◇ Based on newer LASI and LC processors, **second-generation VME** 743i and 744 single-board computers were used in ruggedized 745 and 748i computers. These used newer Visualize C132L workstations design in a VME board.
- ◇ In addition to VME boards, there were other industrial and measurement systems based on HP PA-RISC like Agilent logic analyzers 16600A and 16700A and HP/Agilent V743/64 (E1497A) and V743/100 (E1498A) VXI computers.

HP 74x VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” with end of support 2007.

Third party

Precision RISC Organisation (PRO) was a consortium formed by HP and Convex in 1992 to promote PA-RISC architecture. PA-RISC chips and designs were usually not sold on the market to third-parties, licensing and distribution was tightly controlled by HP to its partners in the PRO.

Some PRO members sold third party PA-RISC computers as OEM or relabeled HP 9000 systems from HP in their markets:

- ◇ Hitachi sold both indigenous workstations (3050RX) and servers (3500) with PA-RISC processors and relabeled HP systems as OEM (9000V).
- ◇ Mitsubishi limited its PA-RISC line to the original HP 9000 “Snakes” (720, 730 and 750) sold in the early-1990s as “MELCOM ME RISC series.”
- ◇ NEC sold a range of HP PA-RISC servers as OEM in Japan, mostly rebadged
- ◇ OKI offered almost the whole range of HP PA-RISC servers and workstations in the 1990s with the various “OKITAC 9000 series.”
- ◇ Samsung apparently also sold some rebadged HP 9000 700 workstations in Korea.

These computers were mostly sold in Japan and Korea, with very limited worldwide distribution. Their vendors soon lost interest in PA-RISC as part of the 2000s general RISC decline and HP’s Itanium transition plans.

HP and the US Navy

During the 1980s and 1990s, HP was part of framework contracts with the US Navy to supply industrial computers and workstations for military uses and “tactical decision support.” These were some of the largest commercial contracts won by HP at the time for PA-RISC computers.

HP was part of at least three programs and contracts with the US Navy:

Desktop Tactical Computer (DTC-1)

This relationship started with DTC-1 program during the 1980s, where HP offered HP FOCUS based HP 9000 520C computers (HP 9020C) that were widely deployed through the US Navy. The 9020C was also part of the US Navy Joint Operational Tactical System, JTOS.

HP 9020C were pervasive in the 1980s throughout the navy, “almost every tactical or fleet staff in the United States Navy had five or more HP 9000s,” used for anti-submarine warfare, anti-air warfare, radar systems and communications. It apparently “served on US nuclear submarines well into the 1990s.”

Tactical Advanced Computer (TAC-3)

After losing out to Sun with the DTC-2 contract, HP won the newer TAC-3 and TAC-4 programs in the early to mid-90s and supplied a large range of PA-RISC computers for various uses at the US Navy and its vessels.

Used in TAC-3 for mission support and tactical use cases were HP Apollo and/or HP 9000 400 workstations (CISC) and HP 9000 720, 730 workstations. The HP 9000 720, 730 and 750 were widely used by the US Navy in TAC-3 for a variety of military applications, including electronic intelligence gathering (ELINT).

The HP 9000 735 were apparently used by the US Navy as part of the TAC-3 (Tactical Advanced Computer) framework, possibly as AN/TSQ-142 mission planning system (TEAMS) for the EA-6B and the 755 used in ATWCS for cruise missiles (Tomahawk).

Tactical Advanced Computer (TAC-4)

TAC-4, for which procurement started in 1993, was one of the “company’s largest-ever federal contract” at the time. As part of US Navy TAC-4, HP supplied PA-RISC workstations, software and infrastructure during the 1990s to the US Navy for measurement and control, including:

- ◇ HP 9000 712 workstations
- ◇ HP Visualize C-Class and J-Class workstations
- ◇ HP 9000 D-Class and K-Class servers
- ◇ HP 9000 74x VME computers
- ◇ SAIC Galaxy portables.

HP 9000 712 workstations were used widely as “TAC-4 Desktop Computer” throughout US Navy and military vessels. Visualize J-Class workstations were offered as part of a technology refreshment of TAC-4 in 1996. D-Class servers were offered as technology refreshment of TAC-4 in 1996, together with K-Class servers.

The 743i and 744 VME computers were used by the US Navy for tactical display and control applications, including the AN/UYQ-70 workstation aboard surface and submarine vessels and surveillance aircraft. With third-party VME devices and systems integrations, the 743i/744 were used with FDDI networking for this.

For environments where standard workstations were not robust enough, HP contracted SAIC to produce a ruggedized MIL-SPEC portable workstation for the Navy: the SAIC Galaxy 1100 based on HP 9000 712, built into a ruggedized case for portable military applications.

3.2.4 Maturity (III)

The maturity of PA-RISC was the phase between 1994 to 2000 with many new products offered, from the last 32-bit workstations to new 64-bit PA-RISC 2.0 when HP Unix was (still) very popular.

Many PA-RISC products were released and the HP Unix/RISC line-up matured during the 1990s, from small PA-RISC desktops to large server cabinets and mainframe-type computers. HP used increasingly complex brands and product groups—HP 9000 700, HP Visualize, HP Integrity with the various “lettered” workstations and server series A-Class, B-Class, J-Class and so on.

PA-RISC moved from 32-bit to 64-bit computing with new PA-8000 processors and successors up to the PA-8800. These were fairly high-powered Unix systems for the niche HP-UX technical and business market. Commodity and mainstream alternatives to RISC and Unix slowly started to appear at the end of that era with Window NT, Linux and faster x86 computers.

HP 9000 700 workstations

HP released very popular PA-RISC workstations in the HP 9000 700 range in 1994 and 1995, before moving PA-RISC to its Visualize branding.

Pizzabox 712 and newer 715: PA-RISC computer design was updated in 1994 with the HP 9000/712 and newer 715 workstations, based on the modern, integrated PA-7100LC processor and LASI chipset.

HP 9000 712 were a revolutionary pizza-box design that offered the advantages of a commercial Unix system on a RISC platform in a very small case (something Apple did a decade later again).

HP 9000 715 were updated with this newer 712 design, enabling a significant performance boost for the venerable 32-bit 715 workhorses. Both 712 and 715 were used a lot for CAD and graphics of the mid-1990s, and were later on popular choices for Unix and open source development.

Visualize workstations

Starting in the mid-1990s, HP started called its PA-RISC workstations “HP Visualize” and gave them lettered names: B-Class, C-Class and J-Class. Formally they were still part of the 9000 700 workstation series but marketed with different branding to focus on their preferred applications and use cases.

Visualize workstations were geared towards graphics and engineering applications such as CAD or CAM and often used with HP’s powerful Visualize and Visualize-FX graphics adapters. Processors were the whole range of PA-RISC CPUs from 32-bit PA-7200 up to 64-bit PA-8900.

- ◇ **B-Class:** Entry-level and most common HP Visualize workstation during that era, B-Class used desktop-type designs and streamlined system architecture, including the B132L, B1000 up to the B2600.
- ◇ **C-Class:** More powerful HP Visualize workstations with more resources than B-Class, the C-Class were still desktops with a slightly more sophisticated system architecture in C100, C132L, C240 up to the C3600 models.
- ◇ **J-Class:** Combining much of the PA-RISC architecture from the mid-90s to early-2000s, HP Visualize J-Class workstations were a range of mini-tower computers with many options and designs, usually multi-processor capable, from J200 to J6000 and J7000.
- ◇ The first **PA-RISC laptop** by RDI Tadpole, the RDI PrecisionBook was based on the Visualize C132L and C160L workstations.

Around 1997, due to competition and a changing market place, HP started aggressively “repricing” its HP 9000 and Visualize workstations with price drops of more than a third, to compete with Sun Ultra 1 and SGI Indigo2 workstations.

Laptops and Portables

Only three portable PA-RISC workstations were produced during 1990s — all by third-party vendors utilizing HP 9000 workstation designs from that era. First, there was the military-focused SAIC Galaxy 1100 portable from 1994, based on HP 9000/712 workstations and available through the Navy TAC-4 program, a very rare computer almost completely used in the military.

Then at the end of the 90s, there were the RDI PrecisionBooks, true laptops based on C132L workstation designs from HP, which were designed into a military-focused portable system by RDI, later acquired by Tadpole. It did not enjoy widespread success.

In the mid-1990s, Hitachi of Japan designed another PA-RISC portable, the 3050RX/100C for the Japanese market, based on the Hitachi PA/50L processor.

Lettered servers

Like workstation, HP renamed its HP 9000 servers to lettered designators that now included a spectrum of different 32- and 64-bit PA-RISC computers. These servers were quite powerful at the time of the 1990s with diverse configurations and designs, from the small A-Class to the mid-size D-Class and cabinet-size K-Class.

Early in this switch, HP still sold Unix servers under HP 9000 800 branding:

- ◇ **E-Class:** The third generation HP 9000 800 servers from the mid-1990 were HP 9000 E-Class, the follow-on of F/G/H/I-Class servers based on “low-cost” PA-7100LC processor and integrated system design in small tower cases. E25 to the E55 were the last traditional HP 9000 800 Series servers.

During that time, system architecture between HP 9000 700 workstations and 800 servers began to converge, only to start diverging again in the late-1990s with the Cell and Stretch architectures, when HP moved to hardware virtualization.

- ◇ **A-Class:** The first PA-RISC servers geared towards large-scale deployments into racks (2U), A-Class were small servers with streamlined system design geared towards “Internet” applications of the dotcom boom. HP 9000 A180 was a 32-bit PA-7300LC budget design similar to HP Visualize B180L, while HP A400 and A500 with 64-bit PA-8x00 processors were early harbinger of the **rp** moniker with a similar architecture to the Visualize C3000/C3600 workstations.
- ◇ **D-Class, R-Class and K-Class:** Three groups of servers from the HP 9000 800 range that were all based on the premise of flexibility in system design. They shared configuration, upgrades and options from 32-bit PA-7100LC to multi-processor 64-bit PA-8200. The tower-sized “enterprise” HP 9000 D-Class servers had up to two CPUs, eight hard-drives and eight I/O slots, from D200 to D390. Built into a rack-mountable case, HP 9000 R-Class R380 and R390 shared the D-Class platform with slight differences in I/O and storage.
- ◇ **L-Class and N-Class:** HP experimented with designs and concepts for both PA-RISC and Itanium with L-Class and N-Class rack-mountable 64-bit PA-RISC servers. There were four different variants and system architectures released between 1999 and 2002. L1000 and L2000 were based on HP Astro architecture, also used in workstations, L1500, L3000 and N4000 used HP Stretch

chipset, a rather strange bird, while later N4000 used HP Cell crossbar chipset like Superdome mainframes. These were already name **rp** servers.

Mainframes

The label “mainframe” is used rather broadly here to include all larger HP PA-RISC computers with a large amount of computing resources that were either multi-processor or cluster-type systems. Some were HP’s own development, like the T-Class, an outgrow of the original 800 series servers, and the later Superdome. Others were either co-developed or acquired externally, like the SPP Exemplar architecture from Convex, with which HP partnered as reseller in 1994 before buying them outright in 1995.

- ◇ **T-Class:** The HP 9000/T-Class servers were large 32-bit and 64-bit PA-RISC mainframes from the mid-1990s, built with modular system cards that contain processors, memory or I/O devices. The HP 9000/890 was an early iteration of the architecture, with the later T500/T600 being updated successors. After the 64-bit T600 the basic system design of the T-Class was discontinued in favor of the more flexible Superdome systems.
- ◇ **S-Class and X-Class Convex:** The SPP Exemplar were cluster mainframes developed by Convex in the 1990s, based on a multi-processor system design with up to 128 PA-RISC 1.1 processors. Multiple types were available in the SPP1000, SPP1200 and SPP1600: compact systems, hyper-nodes and clusters. This was followed in 1997 with the 64-bit SPP2000 S-Class/X-Class, jointly marketed between HP and Convex after the acquisition. All these are based on a crossbar architecture with an internal switching component, based on GaA. The SPP Exemplar all ran Convex SPP-UX, a custom Mach-based Unix operating system.
- ◇ **V-Class:** The V-Class V2200, V2250 and V2500 and V2600 were the second generation scalable PA-RISC servers based on the Convex Exemplar architecture, with up to 32 64-bit PA-RISC processors in a single cabinet. The architecture was HP’s own HyperPlane crossbar chipset, a continuation and upgraded from the original Convex GaA architecture with faster processors and memory. Individual V-Class nodes could be clustered into groups of four, connected by CTI links. Operating system was HP-UX.

3.2.5 Decline (IV)

HP slowly transitioned to a “post-RISC” phase in the 2000s, with a long-planned move to VLIW Itanium IA64 for its technical and Unix offerings. The decline of PA-RISC was set in stone much earlier than that, with the mid-1990s joint development of Itanium together with Intel, and decided in the mid-2000s.

Beginning in the late 1980s, PA-RISC systems often wore the crown of fastest technical (RISC and Unix) workstations until the heydays of the 90s, albeit at a (boutique) price. PA-RISC was relegated in the 2000s to a niche market with the **rp** Integrity PA-RISC servers. As a result of a changing market environment, PA-RISC slowly was phased out of the technical HP line-up first for Itanium products and later for mainstream x86 (64-bit) computers.

Integrity

HP again renamed its PA-RISC servers in the early 2000s into **rp** and shifted the focus of PA-RISC towards servers with that rename. **rp** servers were based on 64-bit PA-RISC processors from the PA-

8500 to the PA-8800, all multi-processor. Only the first rp branded systems shared design features with prior workstations and older servers, while the rest were new, server-only designs.

- ◇ **rp2400:** A rebranding of the original A-Class 64-bit A400 and A500 servers as rp2400 to rp2470 2U rack-servers with one to two PA-RISC 2.0 processors in an Astro system design.
- ◇ **rp3400:** Successors to the popular rp2400 line, rp3410 and rp3440 used the HP zx1 Itanium chipset for up to two PA-8800 or PA-8900 processors, also in 2U. Upgrades to Itanium were available.
- ◇ **rp4400:** Closely related to rp3400, rp4410 and rp4440 were 4U rack servers with up to four dual-core PA-8800 and PA8900 on HP zx1 chipset, released in 2004. Their design featured up to 128 GB memory and quite high memory throughput.
- ◇ **rp5400:** Rebranded L-Class 64-bit servers with the rp5400 and rp5450 being former L1000 and L2000 based on Astro/Elroy design and rp5430 and rp5470 former L1500 and L3000 with sophisticated Stretch chipset. 7U, up to 4-way.
- ◇ **rp7400:** Rebranded and redesigned N-Class servers, rp7400 were the original N4000 with Stretch chipset and rp7405 and 7410 sharing the N4000 name but using a completely new, Superdome-like Cell design up to 8-way. Later rp7420 and rp7440 supported newer CPUs, expansion and more memory.
- ◇ **rp8400:** Some of the largest Cell-based 64-bit servers before the Superdome mainframe, the rp8400, rp8420 and rp8440 used up to sixteen processors up to the PA-8900 plus large amounts of expansion and RAM.

With rp servers HP moved its PA-RISC offering closer to new Itanium rx server architecture. Product and technical design was similar between rp and rx, and PA-RISC rp moved strongly towards Itanium with zx1 chipsets and upgrade paths to IA64 processors. HP rp servers were the last line of PA-RISC servers.

Itanium

Around the turn of the century, HP started to offer servers and workstations based on Itanium IA64 technology, a VLIW architecture jointly designed with Intel. System architecture in PA-RISC rp and IA64 rx servers converged and Itanium slowly phased out PA-RISC from HP's technical and Unix lineup around 2002.

However, this happened at least half a decade later than HP originally planned – the “transition from PA-RISC to Itanium is inevitable,” as HP put it. To convince hesitant PA-RISC holdouts to make the move, HP claimed “Itanium is really the evolutionary successor to PA-RISC” and “PA-RISC lives on in the IPF architecture” with “HP Unix servers reflect our smooth evolutionary philosophy admirably.”

- ◇ **rx Series:** Many Itanium servers were available in parallel to PA-RISC for HP-UX, Linux, Windows or OpenVMS. Most rx are multi-processor systems, based on HP's own zx1 chipset, also used in PA-RISC, with some zx2, SX1000 and SX2000.
First generation rx included the 1U rx1600 and rx1620, 2U rx2600 and rx2620, 4U rx4640 and 7U rx4610 and rx5670 servers. These were followed soon by zx2 based systems that were similar but offered more speed and newer Itanium 2 processors in the rx2660 and rx6600 servers, among others.
- ◇ **Itanium workstations:** Only three Itanium workstations were offered, the very early HP i2000 with first-generation Itanium and Intel reference architecture, and later more flexible HP zx2000 and zx6000. HP zx2000 had a sleek tower while zx6000 were dual-processor rack systems,

technically similar to PA-RISC HP C8000 workstations on the same HP zx1 platform. Itanium workstations were not a revelation performance-wise when compared to both earlier forecasts, modern Intel x86 or even the last PA-RISC designs.

This marked the end of the PA-RISC platform at HP, with diminishing market share until the mid-2000s. The process of the long decline of RISC and commercial Unix servers was already underway then, with Unix relegated to special applications and later to high-end, mission-critical servers. HP started withdrawing from Unix workstations before Itanium, but pared down its offering even further with IA64.

Shipments of Itanium *workstations* ceased two years after release, at the time when Intel moved the x86 architecture to 64-bit. Originally envisaged as an industry-changing architecture, Itanium ended up as alternative to other RISC platforms it was meant to replace, and marked the end-phase of HP Unix and RISC platforms. Support for Itanium on Linux was also ended with Linux 6.7 in 2024.

On a side tangent of history, HP inherited both DEC Alpha RISC and OpenVMS through its acquisition of Compaq in early 2002, both had been rivals for HP platforms for decades. After discontinuing DEC Alpha, OpenVMS was to find a new home with the Itanium platform at HP, to which it was ported around 2005 to run on HP rx servers, being the first computers to offer both HP-UX and OpenVMS.

Mainframe

Large computers were the last refuge of PA-RISC architecture in the late 2000s with the Superdome “mainframe” computers that utilized a similar (Cell) architecture as earlier rp and N-Class servers.

Superdome: The Superdome servers were a completely new design, for up to 64 processors per cabinet. The Superdome “Legacy”, or white systems, used a Cell crossbar chipset with 64-bit PA-RISC processors, while the newer Superdome sx1000 and sx2000, or black systems, used SX chipsets and a mixture of Itanium 2 processors. They all ran HP-UX and Linux, while the SX models also Windows and OpenVMS.

3.2.6 Timeline

HP 9000 started as a family with HP 9000 500 in 1982, joined by PA-RISC with the 840 server in 1986, giving birth to the HP 9000 800 series of departmental servers. HP soon started to diversify its Unix and PA-RISC offerings and introduced the 700 series workstations, 740 series VME boards and in the mid-90s a large range of “lettered” computers (A-Class, J-Class ...) that were also marketed as Visualize and Integrity, then switching to *rp* and *rx* naming.

Table 3.13: PA-RISC timeline, ▲ - workstation, ■ - server, ❖ - rack

Year	500	600	700	740	800	DN	A	B	C	D	E	F-I	J	K	L	N	R	rp	rx	SD	T	V		
1982	▲ ■																							
1983																								
1984	■																							
1985																								
1986					■																			
1987					■																			
1988		■			■	▲																		
1989		■			■																			

1990					■																	
1991			▲		■						■											
1992			▲	❖							■											
1993			▲								■									❖		
1994			▲	❖						■												
1995			▲						▲	■		▲	■							❖		
1996				❖				▲	▲	■		▲	■									
1997								▲	▲	■		▲	■							❖		
1998							❖						■			❖				❖		
1999								▲	▲			▲		❖	❖		❖			❖		
2000							❖	▲	▲			▲		❖		❖				❖		
2001									▲			▲				❖						
2002																❖						
2003																❖	❖	❖				
2004									▲							❖	❖					
2005																❖						
2006																				❖		
2007																❖	❖					
Year	500	600	700	740	800	DN	A	B	C	D	E	F-I	J	K	L	N	R	rp	rx	SD	T	V

3.2.7 Sources

The information on this page is based mostly on existing OpenPA content and includes new interpretation and other sources. Some pieces were sourced from the great HP Computer Museum, but also from news releases, journals or HP Labs.

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- ❖ Itanium: A cautionary tale, CNet December 2005
- ❖ The Battle in 64 bit Land, 2003 and Beyond, Real World Tech, 2003
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- ❖ HP Completes Its PA-RISC Road Map With Final Processor Upgrade, Information Week, June 2005
- ❖ SAIC Galaxy 1100: a pre-CDE VUE of the PA-RISC with a security clearance, Old VCR, January 2023

Further reading

- ❖ The mass extinction of UNIX workstations, OSnews, Thom Holwerda, 12/2022
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- ❖ PA-RISC to Itanium family of processors road map, Hewlett-Packard Company (2002: mirror accessed January 2024)

- ◇ HP UNIX Workstations and Netstations, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP Enterprise Computing Assistance Directory, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ HP Technical Documentation, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ HP Computer Systems Buyer's Guide, Hewlett-Packard Company (1997: mirror accessed January 2024)

Pictures Hewlett Packard, scans from product brochures, hpmuseum.net and 100obit.it

3.3 HP 9000 705 and 710

HP 9000/705 and HP 9000/710 were the first small PA-RISC workstations, released in 1992. They are simplified versions of the “Snakes” 720, 730 and 750 workstations in a small case.

The basic HP 9000 technical workstation design was taken over with few changes:

- ◇ Smaller instruction and data caches on the processor
- ◇ Lower CPU clock rate
- ◇ Different memory architecture
- ◇ Integration of graphics, SCSI, Ethernet subsystem onto a single mainboard
- ◇ Reduced expansion options
- ◇ First audio capable Series 700 workstation

HP 9000 705 and 710 were marketed to compete in the early 1990s low-end workstation market. The competition between \$5,000 and \$10,000 were lower cost Sun Sparcstation IPX and from IBM RS/6000 220 for Unix.

- ◇ HP 9000 705 were introduced in 1992 for \$8,990
- ◇ HP 9000 710 were introduced in 1992 for \$12,490

HP introduced another pizzabox-sized workstation a few years later in 1994 with the HP 9000 712 workstation, based on newer 32-bit PA-7100LC processors.

3.3.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 705	PA-7000 PA-RISC 32-bit	35 MHz	96 KB off-chip
HP 9000 710	PA-7000 PA-RISC 32-bit	50 MHz	96 KB off-chip

Chipset

- ◇ HP ASP chipset, a custom HP RISC design
- ◇ HP Viper memory and I/O controller, low-cost version implemented in two chips
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ Audio 8-bit mono PSB2160 CODEC
- ◇ Other I/O (serial, parallel, i8042)
- ◇ HP Stinger (?) CRX graphics, 8-bit

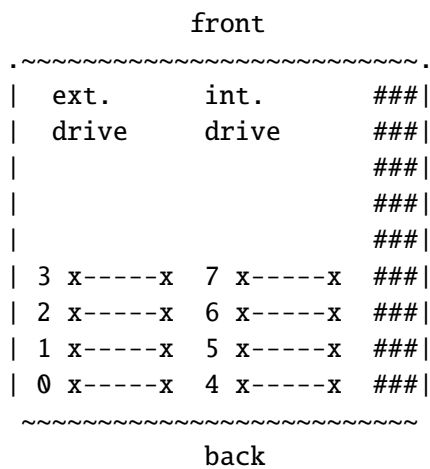
System buses

- ◇ PBus processor/memory bus, 200 MB/s at 50 MHz (710), 140 MB/s at 35 MHz (705)

- ◇ VSC main system bus, 100 MB/s at 25 MHz (710), 70 MB/s at 17.5 MHz (705)
- ◇ GSC system-level I/O bus
- ◇ SCSI-2 narrow single-ended bus

Memory

- ◇ HP-proprietary 72-pin SIMMs
- ◇ Eight sockets
- ◇ 16 MB (4×4) minimum, 64 MB maximum
- ◇ Memory has to be installed in *quartets*:
first in the “even” slots (0, 2, 4, 6), then in the “odd” slots (1, 3, 5, 7):



Expansion slots

- ◇ No expansion slots

Storage

- ◇ SCSI 3.5" 50-pin Narrow SE hard drive
- ◇ SCSI half-height 5.25" 50-pin Narrow SE drive, external accessible

3.3.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ 15-pin AUI 10 Mbit/s & 10Base2 BNC Ethernet
- ◇ VGA HD15
- ◇ HP-HIL connector for input devices

- ◇ Two phone jacks (microphone, headphones)
- ◇ Nine LEDs on the front for errors and status messages

3.3.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode, might work but unsupported
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.01, 9.03, 9.05, 9.07), pre-Y2K
 - HP-UX 8 (8.07), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ HPBSD, original 4.3BSD Unix on PA-RISC (closed)
- ◇ Mach 4/Lites, research microkernel with 4.4BSD (with issues)
- ◇ MkLinux, research Linux with Mach microkernel
- ◇ 710OSF MK-PA, OSF/1 Unix port to PA-RISC

3.3.4 Benchmarks

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 705	PA-7000 35 MHz	21.9	33.0		
HP 9000 710	PA-7000 50 MHz	31.6	47.6	0.99	1.44

Comparison to SPEC benchmark data from other contemporary Unix workstations. HP 9000 705 and 710 were slightly slower than a higher-clocked Intel 486DX2 but much faster in floating point, even beating an Intel Pentium.

Table 3.16: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 735/99	PA-7100 99 MHz	109.1	167.9	3.22	4.06
Intel Xpress	Intel Pentium 75MHz	89.1	68.5	2.31	2.02
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
HP 9000 712/60	PA-7100LC 60 MHz	67.0	85.3	2.08	2.66
SGI IRIS Indigo IP20	MIPS R4000 100MHz	57.6	60.3		
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		
IBM RS/6000 355	IBM POWER 41MHz	40.7	83.3		
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	16.1		

Motorola 8000	Motorola 88100 33MHz	27.7	18.8		
SGI IRIS Indigo IP12	MIPS R3000 33MHz	22.4	24.2		
Digital DECstation 5000	MIPS R3000 33MHz	20.9	23.4		
HP 9000 425e	Motorola 68040 25MHz	12.2	9.3		
Digital VAX4000	DEC KA46 22MHz	11.1	12.6		

3.3.5 Documentation

Manuals

- ◇ HP 9000 Series 700 Model 705 and 710 Owner's Guide, Hewlett Packard (January 1992, A1991-90608, edition E0192) [hpmuseum](#)

LED messages

- ◇ LED errors and status messages might be displayed on the HP 9000 705/710 front LEDs

Product sheets

- ◇ Introducing the Model 705 Colour workstation, The power you need, Hewlett Packard (January 1992, A1991-90608, edition E0192) [hpmuseum](#)
- ◇ HP Apollo Series 700 Model 710 Workstation, product brief, Hewlett Packard (January 1992, 5091-3183E) [hpmuseum](#)

Articles

- ◇ High-Performance Design for Low-Cost PA-RISC Desktops (.pdf) pp. 55-63 Craig Fink et al (August 1992: Hewlett-Packard Journal)
- ◇ Hewlett unveils low-cost workstations, UPI Archives, May 12 1992
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- ◇ HP Apollo Series 700 Performance Brief, Hewlett Packard (n.d., no #) [hpmuseum](#)

3.4 HP 9000 712

The HP 9000 712 workstations were a 1994 “low-cost” Unix and PA-RISC workstation design from HP and the second “pizza-box” system after the 705 and 710 workstations for HP-UX.

The design goal from HP for the 32-bit 712 workstation was to reach the performance of 1992-era workstations such as the HP 9000 735 at a fraction of their fabrication costs.

712 workstations used a highly simplified and integrated VLSI design from HP with many components on-board, its “pizza-box” case was one of the smallest Unix workstation cases of the 90s, similar to Sun SPARCstations.

Geared towards graphical user interfaces and X Window environment, 712 had hardware accelerators for 2D graphics. The beautiful NeXTSTEP PA-RISC operating system, based on Mach and Unix, was designed for and on HP 9000 712.

712 were very popular in the 1990s in technical disciplines and graphics, software and early (90s!) multi-media development. Especially the 712/60 was competitively priced at the time for an entry-level RISC Unix system, compared to HP and competing Unix RISC products. HP 712 offered “outstanding performance at new low prices” with integrated graphics, standard I/O, stereo audio, solid integer performance for Unix applications.

Together with other HP 9000 computers, 712 workstations were part of the mid-1990s US Navy TAC-4 program for tactical computers. This led to HP 9000 712s being used widely as TAC-4 Desktop Computer throughout US Navy and military vessels. HP 9000 712 and its architecture was the basis for other systems like the newer, LASI-based 715 workstations and the SAIC Galaxy 1100, the first PA-RISC portable.

- ◇ HP 9000 712/60 were introduced in 1994 for \$4,400
- ◇ HP 9000 712/80 were introduced in 1994 for \$8,820
- ◇ HP 9000 712/100 were introduced in 1995 for \$15,100

HP reduced pricing of 712 and 715 workstations quite aggressively in 1997, by up to 50 percent (to \$7,060 for 712/100) when newer B-Class computers became available. HP 9000 712 played a key role in the open source scene of the 2000s.

3.4.1 System architecture

Processors

System	CPU	Speed	L1 cache
712/60	PA-7100LC PA-RISC 32-bit	60 MHz	1 KB on-chip and 64 KB off-chip
712/80	PA-7100LC PA-RISC 32-bit	80 MHz	1 KB on-chip and 256 KB off-chip
712/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller

- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Artist graphics, 8-bit, 1 MB VRAM, 1024x768 or 1280x1024 with 2 MB VRAM
- ◇ *Integrated* Other I/O (serial, parallel, Floppy)

System buses

- ◇ GSC system level I/O bus (128 MB/s)
- ◇ SCSI-2 single-ended bus

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32 MB modules
- ◇ Either 4 memory sockets, on 712/60 and /80 models, or 6, on 712/100
- ◇ 16 MB minimum, 128 MB/192 MB maximum
- ◇ Memory has to be installed in pairs, starting from slot 0, the closest slot to the drives.

Expansion slots

- ◇ VRAM expansion slot for A2263-66520 expansion for higher resolutions/more colors, see a picture of the VRAM at hpmuseum
- ◇ One slot for a GIO card, a special formfactor GSC bus card only used in the 712, with some cards available for networking, video and I/O
- ◇ One slot for a TSIO card, a special formfactor GSC card for the *Teleshare* expansion slot, with only one card offered

Storage

- ◇ SCSI 3.5" Fast-Narrow SE 50-pin hard drive
- ◇ 3.5" Floppy drive with special connector

3.4.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Serial RS232C DB9, up to 115200 baud
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ VGA HD15

- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Three phone jacks (microphone, headphones and line-in)
- ◇ One LED on the front for errors and status messages

3.4.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9.07 (possibly also 9.05), pre-Y2K
- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ HPBSD, original 4.3BSD Unix on PA-RISC (closed)
- ◇ Mach 4/Lites, research microkernel with 4.4BSD (with issues)
- ◇ MkLinux, research Linux with Mach microkernel
- ◇ OSF MK-PA, OSF/1 Unix port to PA-RISC
- ◇ Windows NT was planned in 1994 for HP 9000 712 workstations

3.4.4 Dimensions

Height	Width	Depth	Weight
70mm	432mm	400mm	8kg

3.4.5 Benchmarks

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 712/60	PA-7100LC 60MHz	67.0	85.3	2.08	2.66
HP 9000 712/80	PA-7100LC 80MHz	97.1	123.3	3.12	3.55
HP 9000 712/100	PA-7100LC 100MHz	117.2	144.2	3.76	4.06

Comparison to SPEC benchmark data from other contemporary Unix workstations. HP 9000 712 were slightly faster than MIPS, Alpha, SPARC and Intel computers from the same time, but usually significantly faster in floating point.

Table 3.20: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 150MHz	276.3	220.0	6.08	5.42
HP 9000 C110	PA-7200 120MHz	167.0	269.0	6.00	8.14
HP 9000 735/125	PA-7150 125MHz	136.0	201.0	3.97	4.61
DEC Alphastation 250	DEC Alpha 21064A 266MHz	198.6	262.5	4.18	6.27
IBM RS/6000 43P	PowerPC 604 100MHz	128.0	120.2	3.59	3.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2	3.11	3.10
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2	4.04	2.35
Intel Xpress	Intel Pentium 75MHz	89.1	68.5	2.31	2.02
SGI Indigo2	MIPS R4400SC 75MHz	85.9	93.6		
IBM RS/6000 250	PowerPC 601 80MHz	77.6	89.4	1.82	2.03
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
SGI IRIS Indigo IP20	MIPS R4000 100MHz	57.6	60.3		
Micronics M4P	Intel 486DX4 100MHz	51.4	26.6		
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		

3.4.6 Documentation

Manuals

- ◇ Model 712 Technical Reference (PDF) Hewlett Packard 1995 [parisc linux](#)
- ◇ Model 712 Service Handbook (PDF) Hewlett Packard 1995 [parisc linux](#)

LED messages

- ◇ LED errors and status messages might be displayed on the HP 9000 712 front LEDs

Product sheets

- ◇ A Low-Cost, High-Performance PA-RISC Workstation with Built-In Graphics, Multimedia, and Networking Capabilities (PDF, HP Journal 4/95)
- ◇ An I/O System on a Chip (LASI) (PDF, HP Journal 4/95)
- ◇ Product design of the Model 712 (PDF, HP Journal 4/95)
- ◇ HP 9000 Series 700 Model 712/60 and 712/80i Workstations, Hewlett-Packard, 12/1993, 5091-9780E
- ◇ HP UNIX Workstations and Netstations, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP 9000 Models 712/60, 712/80, and 712/100 Workstations, HP Workstation Group , Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ Product Brief HP 9000 Models 712/60, 712/80, and 712/100 Workstations (PDF, 88 KB, Hewlett Packard)

- ◇ HP 9000 New product Summary guide, technical sales document, second part is on 712, Hewlett Packard: 1993 100obit.it

Articles

- ◇ Large parts of the HP Journal April 1995 Issue describe HP 9000 712
- ◇ First NeXT RISC Workstation: Our first look at NEXTSTEP on HP's low-cost pizza box, NeXTWORLD, April 1994
- ◇ Famous Graphics Chips: HP's Artist Graphics, Jon Peddie, computer.org 2020
- ◇ Booting the HP 712, Sophie Haskins, Pizza Box Computer, 2018
- ◇ NeXTstep on the HP 712 Part 1: Installation, Sophie Haskins, Pizza Box Computer, 2020
- ◇ HP to field two low-end workstations, small Unix server, Computerworld 1993-12-20: Volume 27 Issue 51

ROM update

There is a firmware update available for HP 9000 712 to the latest version 2.3.

- ◇ PF_C7120023.txt has details about contents and installation of the patch.
- ◇ PF_C7120023 contains the patch.

Other

- ◇ NetBSD 712 serial console HOWTO, instructions for serial console, i.e. headless
- ◇ Pinout for the AUI/RS232 Y-cable for the optional second Ethernet/serial card.

3.5 HP 9000 715

HP 9000 715 are 32-bit PA-RISC workstations from HP from the mid-1990s. Often used for technical design, CAD/CAM and engineering, the 715 were powerful, expandable HP-UX systems. They were popular computers when Unix workstations were used for technical computing in the 90s.

HP 9000 715 were marketed against other Unix workstations of the 90s: SGI Indy, DEC Alpha, IBM RS/6000. With their advanced video adapters, 715 were often used for graphical (2D and 3D) and video editing.

There were two different 715 designs. Early 715 versions were based on HP ASP chipset with PA-7100 CPUs: 715/33, 715/50 and 715/75 with “Apollo” branding (the 715/33 was one of the slowest and worst PA-RISC workstations ever). The second generation was more modern based on HP LASI design with PA-7100LC CPUs: 715/64, 715/80, 715/100 and 100XC, close to the pizzabox HP 9000 712 workstations, the 100XC being a rather fast machine for the 1990s.

HP marketed the LASI HP 9000/715 as supporting “bi-endian switching for current and future operating systems”, a reference to aborted Windows NT PA-RISC and other 1990s plans.

Billed by HP as having “easy installation, upgradability, expansion, and serviceability”, HP 9000 715 workstations were handy Unix computers for the 1990s and supported NeXTSTEP on PA-RISC well.

- ◇ HP 9000 715/33 were introduced in 1992 for \$4,995
- ◇ HP 9000 715/50 were introduced in 1992 for \$11,895
- ◇ HP 9000 715/75 were introduced in 1992 for \$11,005
- ◇ HP 9000 715/64 were introduced in 1994 for \$10,000
- ◇ HP 9000 715/80 were introduced in 1994 for \$13,000
- ◇ HP 9000 715/100 were introduced in 1994 for \$19,000
- ◇ HP 9000 712/100XC were introduced in 1995 for \$21,100

3.5.1 System architecture

Processors

System	CPU	Speed	Cache
715/33	PA-7100 PA-RISC 32-bit	33 MHz	128 KB off-chip
715/50	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip
715/64	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 64 KB off-chip
715/75	PA-7100 PA-RISC 32-bit	75 MHz	512 KB off-chip
715/80	PA-7100LC PA-RISC 32-bit	80 MHz	1 KB on-chip and 256 KB off-chip
715/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip
715/100XC	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 1024 KB off-chip

Chipset

715/33, 50 and 75 (first version, ASP)

First version of 715 workstations with older architecture.

- ◇ HP ASP chipset
- ◇ HP Viper memory and I/O controller
- ◇ *Integrated* NCR 53C700 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596DX 10 Mbit Ethernet controller
- ◇ Intel 82350 EISA bus adapter chipset (EISA-GSC)
- ◇ HP Stinger CRX graphics, 8-bit, 1280x1024 gray or 1024x768 color
 - *Optional* HP CRX GSC video adapters
 - *Optional* HP CRX-24 GSC video adapters
- ◇ Audio 16-bit CS4215 CODEC
- ◇ Other I/O (serial, parallel, i8042)

715/64, 80 and 100 (second version, LASI)

Second version of 715 workstations with modernized architecture.

- ◇ HP LASI chipset, highly integrated
- ◇ Memory and I/O controller integrated into the PA-7100 processor
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax, EISA bridge and HP-HIL
- ◇ HP Artist graphics, 8-bit, 1 MB VRAM (could be extended to 2), 1280x1024
 - *Optional* HP CRX GSC video adapters
 - *Optional* HP HCRX GSC video adapters
- ◇ Other I/O like serial, parallel, HP-HIL, Floppy

System buses

- ◇ GSC system level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 single-ended narrow bus
- ◇ 715/33, 50, 75PBus processor/memory bus
- ◇ 715/33, 50, 75VSC main system bus
- ◇ 715/33, 50, 75SGC expansion of the mainbus to the SGC expansion card

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Eight sockets for 8-32 MB modules
- ◇ 715/33 6 memory sockets
- ◇ 16 MB to 192 MB (6×32) or 256 MB (8×32) supported

Expansion slots

- ◇ 715/33, 50, 75 One slot for SGC (EISA formfactor) cards
- ◇ 715/64, 80, 100 One slot for GSC (EISA formfactor) cards
- ◇ With an HP adapter EISA cards can be used in the GSC or SGC slots

Storage

- ◇ Two SCSI 3.5" Fast-Narrow SE 50-pin hard drives
- ◇ SCSI half-height 5.25" Fast-Narrow SE 50-pin drive, externally accessible

3.5.2 External ports

- ◇ SCSI-2 50-pin single-ended Fast-Narrow
- ◇ Two serial RS232C DB9 (up to 115200 baud)
- ◇ Parallel DB25
- ◇ Ethernet AUI 15-pin
- ◇ VGA HD15
- ◇ 715/33, 50, 75 HP-HIL connector for input devices
- ◇ 715/64, 80, 100 SMD-10 connector, to connect HIL and PS2
- ◇ Four phone jacks (microphone, headphones and line-in and ?)
- ◇ Nine LEDs on the front for errors and status messages

3.5.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 715/64, 80, 100 HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.05, 9.07), pre-Y2K

- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ HPBSD, original 4.3BSD Unix on PA-RISC (closed)
- ◇ Mach 4/Lites, research microkernel with 4.4BSD (with issues)
- ◇ MkLinux, research Linux with Mach microkernel
- ◇ OSF MK-PA, OSF/1 Unix port to PA-RISC

3.5.4 Benchmarks

System	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 715/33	32.5	52.4	1.01	1.58
HP 9000 715/50	49.2	78.8	1.53	2.46
HP 9000 715/64	80.6	109.4	2.52	3.31
HP 9000 715/75	82.6	127.2	2.51	3.85
HP 9000 715/80	96.3	123.2	3.01	3.50
HP 9000 715/100	115.1	138.7	3.76	4.06
HP 9000 715/100XC	132.2	184.6	4.55	4.70

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.23: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 150MHz	276.3	220.0	6.08	5.42
HP 9000 C110	PA-7200 120 MHz	167.0	269.0	6.00	8.14
DEC Alphastation 250	DEC Alpha 21064A 266MHz	198.6	262.5	4.18	6.27
HP 9000 735/125	PA-7150 125 MHz	136.0	201.0	3.97	4.61
IBM RS/6000 43P	PowerPC 604 100 MHz	128.0	120.2	3.59	3.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2	3.11	3.10
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2	4.04	2.35
SGI Indy	MIPS R4400SC 75MHz	88.1	96.6		
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
SGI IRIS Indigo IP20	MIPS R4000 100MHz	57.6	60.3		
Digital DECpc XL	Intel Pentium 66MHz	51.6	47.5		
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
HP Vectra VL2	Intel 486DX4 100MHz	45.8	23.1		
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	16.1		
Motorola 8000	Motorola 88100 33MHz	27.7	18.8		
SGI IRIS Indigo IP12	MIPS R3000 33MHz	22.4	24.2		

3.5.5 Documentation

Manuals

- ◇ Model 715 Service Handbook, Hewlett Packard (August 1995, A2600â€š90039) **parisc linux**
- ◇ HP 9000 Series 700 Model 715 Owner's Guide, Hewlett Packard (April 1994, A2084-90692) **hpmuseum**
- ◇ HP Apollo 9000 Series 700 Model 715/33 and 715/50 Owner's Guide, Hewlett Packard (January 1993, A2084-90613) **hpmuseum**
- ◇ Hardware Installation Guide Model 715, Hewlett Packard (April 1993, A2084-90012) **hpmuseum**

LED messages

- ◇ LED errors and status messages might be displayed on the HP 9000 715 front LEDs

Product sheets

- ◇ HP UNIX Workstations and Netstations, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP 9000 Models 715/64, 715/80, 715/100, and 715/100XC Workstations, HP Workstation Group, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ Quick Reference Guide HP 9000 715 Workstations, Hewlett Packard 4/1994, 5962-9710LE 100bit.it
- ◇ HP 9000 Series 700 Model 715/725 Workstation Price & Configuration Guide, Hewlett Packard (August 1993, 5091-8811E) **hpmuseum**
- ◇ HP Apollo 9000 Series 700 Model 715/75 Model 725/75 Sales Guide, Hewlett Packard (August 1993, 5091-8794) **hpmuseum**
- ◇ HP Apollo Series 700 Performance Brief, Hewlett Packard (October 1992, 5091-5750E) **hpmuseum**
- ◇ HP 9000 Series 700 Model 715/33 and 715/50, product brief, Hewlett Packard (April 1994, 5091-5779E) **hpmuseum**
- ◇ HP 9000 Series 700 Model 715/33, 715/50 and 715/75, product brief, Hewlett Packard (April 1994, 5091-9991E) **hpmuseum**
- ◇ HP 9000 Series 700 Model 715/64, 715/80 and 715/100, product brief, Hewlett Packard (April 1994, 5962-9555E) **hpmuseum**

ROM update

There is a firmware update available for the 715/64, /80 and /100.

- ◇ C7X50016.text has details about the patch and installation **parisc linux**
- ◇ C7X50016.frm contains the new firmware **parisc linux**

3.6 HP 9000 720, 730 and 750

HP 9000 720, 730 and 750 were the first dedicated 32-bit PA-RISC workstations, released in 1991. Called *Snakes*, they were based on the first PA-RISC 1.1 processor, the PA-7000 (PCX-S), which was designed to power “low cost high performance” workstations.

Snakes were designed for graphics and integrated computing requirements – many I/O controllers and interfaces were integrated into the system, such as NCR SCSI, HP graphics and Intel Ethernet networking.

Cases were constructed solidly and used interlocking modules, *sliders*. Storage has its own slider, connected to the main I/O board with a short external cable. 720 and 730 share the same backplane and I/O board and could be upgraded through the exchange of the CPU system board.

HP 9000 720, 730 and 750 were widely used by the US Navy through the TAC-3 (Tactical Advanced Computer) framework for military applications, including electronic intelligence gathering (ELINT).

Later HP 9000/735 workstations share a similar case and system setup as the *Snakes*: 720 and 730 CPU and I/O boards can be swapped for 735 boards for a system upgrade, and vice versa (735 I/O boards do not work with 720 CPU boards).

- ◇ HP 9000 720 were introduced in 1991 for \$15,890
 - 720 CRX Color 2D/3D Workstation for \$22,890
 - 720 PVRX Color 3D Workstation for \$34,390
 - Upgrade to 730, CPU board \$9,000
- ◇ HP 9000 730 were introduced in 1991 for \$21,890
 - 730 CRX Color 2D/3D Workstation for \$28,890
 - 730 PVRX Color 3D Workstation for \$40,390
- ◇ HP 9000 750 were introduced in 1991 for \$43,090
 - 750 PVRX Color 3D Workstation for \$118,090
 - 750 TVRX Color 3D Workstation T4 for \$58,090
 - 112MB additional RAM for \$39,200

Especially the more affordable 720 and 730 workstations were widely used in the Unix world of the 1990s, in academia and industry for technical design and computing. Due to their popularity, many operating systems run on *Snakes* workstations and were ported to it, including research and development projects such as OSF/1 and a variety of Mach.

3.6.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 720	PA-7000 PA-RISC 32-bit	50 MHz	384 KB off-chip
HP 9000 730	PA-7000 PA-RISC 32-bit	66 MHz	384 KB off-chip
HP 9000 750	PA-7000 PA-RISC 32-bit	66 MHz	512 KB off-chip

Chipset

- ◇ HP ASP chipset
- ◇ HP Viper memory and I/O controller as VLSI chip
- ◇ Address buffer/controller, 64-pin VLSI CMOS chip
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ Intel 82C501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ Other I/O (serial, parallel, i8042)
- ◇ Graphics through separate boards:
 - *Optional* HP GRX SGC DIO-II video adapters
 - *Optional* HP CRX SGC DIO-II video adapters
 - *Optional* HP CRX-24 SGC DIO-II video adapters

System buses

- ◇ PBus processor/memory bus at full processor clock with 260 MB/s max data rate
- ◇ VSC main system (TTL) bus at half processor clock with 132 MB/s max data rate
- ◇ GSC I/O bus
- ◇ SGC, expansion of the main VSC bus to SGC expansion cards
- ◇ EISA, expansion I/O bus for standard I/O cards
- ◇ SCSI-2 narrow single-ended bus

Memory

- ◇ HP proprietary memory modules, based on DRAMs with error detection and correction (EDC), some shared with 735/755
- ◇ 720 8 slots
- ◇ 730 8 slots and 16 MB onboard, 272 MB (8×32+16) maximum
- ◇ 750 12 slots, 768 MB (12×64) maximum

Expansion slots

- ◇ 720/730
 - One SGC (DIO-II formfactor) expansion slot
 - One EISA slot

- ◇ 750
 - Two SGC (DIO-II formfactor) expansion slots
 - Four EISA slots

Storage

- ◇ 720/730 Two SCSI 3.5" Narrow SE 50-pin hard drives
- ◇ 750 Two SCSI half-height 5.25" Narrow SE 50-pin SCSI drives and two SCSI full-height 5.25" Narrow SE 50-pin SCSI drives

3.6.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ Two serial RS232C DB9 (up to 115200 baud)
- ◇ Parallel DB25
- ◇ 15-pin AUI 10 Mbit & 10Base2 BNC Ethernet
- ◇ Graphics depend on installed SGC framebuffer
- ◇ HP-HIL connector for input devices
- ◇ Jack for beep audio
- ◇ Ten LEDs on the front for errors and status messages

3.6.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode, might work but unsupported
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.01, 9.03, 9.05, 9.07), pre-Y2K
 - HP-UX 8 (8.01, 8.05, 8.07), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ 720OSF MK-PA, OSF/1 Unix port to PA-RISC
- ◇ HPBSD, original 4.3BSD Unix on PA-RISC (closed)
- ◇ Mach 4/Lites, research microkernel with 4.4BSD (with issues)
- ◇ MkLinux, research Linux with Mach microkernel
- ◇ OSF MK-PA, OSF/1 Unix port to PA-RISC

3.6.4 Benchmarks

Table 3.25: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 720	PA-7000 50MHz	36.4	58.2	1.20	2.00
HP 9000 730	PA-7000 66MHz	47.8	75.4	1.50	2.30
HP 9000 750	PA-7000 66MHz	48.1	75.0	1.50	2.30

Compared to SPEC benchmark data, HP 9000 720, 730 and 750 had similar speed to other contemporary Unix workstations and were faster than Intel 486DX2 and level with Pentium at the same clock but significantly faster in floating point.

Table 3.26: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 755/125	PA-7150 125MHz	136.0	201.0	3.97	4.61
Intel	Intel Pentium 75MHz	89.1	68.5	2.31	2.02
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
SGI IRIS Indigo IP20	MIPS R4000 100MHz	57.6	60.3		
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		
IBM RS/6000 355	IBM POWER 41MHz	40.7	83.3		
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	16.1		
Motorola 8000	Motorola 88100 33MHz	27.7	18.8		
SGI IRIS Indigo IP12	MIPS R3000 33MHz	22.4	24.2		
DEC 5000/33	MIPS R3000 33MHz	20.9	23.4		
HP 9000 425e	Motorola 68040 25MHz	12.2	9.3		
Digital VAX4000	DEC KA46 22MHz	11.1	12.6		

3.6.5 Documentation

Manuals

- ◇ HP Apollo 9000 Model 720/730 owner's guide, Hewlett Packard (January 1991, A1926-90001) **parisc linux**
- ◇ HP Apollo 9000 Model 750 owner's guide, Hewlett Packard (June 1991, A1961-90000) **parisc linux**
- ◇ Installation Guide for HP Apollo 9000 Model 720/730 Workstations and Servers, Hewlett Packard (May 1991, A1926-90000) **hpmuseum**
- ◇ Precision Architecture RISC Diagnostics Manual, Volume 1, Hewlett Packard (August 1991, 09740-90041) **hpmuseum**
- ◇ HP Apollo 9000 Series 700 Workstations/Servers CE Handbook, Hewlett Packard (June 1991, A1926-90003) **hpmuseum**

LED messages

- ◇ LED errors and status messages might be displayed on the HP 9000 720, 730 and 750 front LEDs

Product sheets

- ◇ HP Apollo Series 700 Model 720 Workstation, two pager, Hewlett Packard (1991, 5091-0974E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 720 Workstation, product brief, Hewlett Packard (1991, 5091-0977E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 730 Workstation, two pager, Hewlett Packard (February 1991, 5091-0975E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 730 Workstation, product brief, Hewlett Packard (1991, 5091-0979E) **hpmuseum**
- ◇ Feel the Power of PA-RISC Workstations, product brief, Hewlett Packard (1991, 5091-0986E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 750 Workstation, two pager, Hewlett Packard (January 1992, 5091-3188E) **hpmuseum**
- ◇ HP Apollo Series 700 U.S. Price Guide, Hewlett Packard (1991, no #) **hpmuseum**
- ◇ The Best RISC Workstations in the Industry, Hewlett Packard (February 1992, 5091-0983E) **hpmuseum**

Articles

- ◇ *System design for a low cost PA-RISC desktop workstation*, R. Horning et al, COMPCON Spring '91 Digest of Papers, 1991
- ◇ *CMOS PA-RISC processor for a new family of workstations*, M. Forsyth et al, COMPCON Spring '91 Digest of Papers, 1991
- ◇ Hewlett-Packard Journal August 1992
 - *Midrange PA-RISC Workstations with Price/Performance Leadership*, page 6 (Andrew J. DeBaets and Kathleen M. Wheeler)
 - *HP 9000 Series 700 Workstation Firmware (IODC, PDC)* page 9 (Deborah A. Savage)
 - *VLSI Circuits for Low-End and Midrange PA-RISC Computers*, page 12 (Craig A. Gleason et al.)
 - *HP 9000 Series 700 Input/Output Subsystem*, page 26 (Daniel Li and Audrey B. Gore)
 - *Design Verification of the HP 9000 Series 700 PA-RISC Workstations*, page 34 (Ali M. Ahi et al.)
 - *Mechanical Design of the HP 9000 Models 720 and 730 Workstations*, page 43 (Arlen L. Roesner and John P. Hoppal)
 - *Meeting Manufacturing Challenges for PA-RISC Workstations*, page 49 (Spencer M. Ure et al.)

- ◇ HEWLETT-PACKARD UNLEASHES ITS RS/6000 KILLERS, Tech Monitor archive, March 26, 1991
- ◇ Snake In the Box, Unix World May 1999, Volume VIII, Number 5, page 79
- ◇ High Performance PA-RISC Snakes Motherboard I/O , Hewlett-Packard 1993, **bitsavers**
- ◇ HP Apollo Series 700 Performance Brief, Hewlett Packard (October 1992, 5091-5750E) **hpmuseum**

3.7 HP 9000 725

HP 9000 725 PA-RISC workstations were desktop-sized Unix computers, released in 1992. They were a smaller option to the large and expensive HP 9000 750 computers while still offering the same amount of I/O options. System design is based on 715 workstations in a slightly smaller desktop case with dimensions very popular in the early 1990s.

725 were built in two different designs: one based on PA-7100 processors and HP ASP chipset. This original 725/50 was billed by HP as “low-cost workstation” for “applications that require fast X Window System performance and 2D/3D wireframe graphics” such as CAD, MCAD, CASE and publishing. All at “price points comparable to PCs.”

The second, newer 725 design was based on HP LASI chipset and newer PA-RISC LC processors, technically close to the pizzabox HP 9000 712 workstations. The 725/100 was a “high-performance, cost-effective expandable desktop system”. 725 workstations were never as popular however, in spite of good I/O options and a similar case and sizing to contemporary PCs (like HP Vectra).

- ◇ HP 9000 725/50 were introduced in 1992 for \$17,895
- ◇ HP 9000 725/75 were introduced in 1992 for \$20,295
- ◇ HP 9000 725/100 were introduced in 1994

3.7.1 System architecture

Processors

System	CPU	Speed	L1 Cache
HP 9000 725/50	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip
HP 9000 725/75	PA-7100 PA-RISC 32-bit	75 MHz	512 KB off-chip
HP 9000 725/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip

Chipset

725/50 and 725/75

- ◇ HP ASP chipset
- ◇ HP Viper memory and I/O controller
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ Intel 82C501AD Ethernet transceiver
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ Other I/O (serial, parallel, i8042)
- ◇ HP Stinger CRX graphics, 8-bit, 1280x1024 gray or 1024x768 color
 - *Optional* HP CRX GSC video adapters
 - *Optional* HP CRX-24 GSC video adapters

- ◇ Audio 16-bit CS4215 CODEC

725/100

- ◇ HP LASI chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ *Integrated* Other I/O (serial, parallel, i8042)
- ◇ HP Wax chip, EISA bridge, HP-HIL
- ◇ HP Artist graphics, 8-bit, 1280x1024
 - *Optional* HP CRX GSC video adapters
 - *Optional* HP HCRX GSC video adapters
- ◇ Other I/O (serial, parallel, Floppy controller, HP-HIL)

System buses

- ◇ GSC system-level I/O bus
- ◇ EISA additional I/O expansion bus
- ◇ 725/50, 75PBus processor/memory bus
- ◇ 725/50, 75VSC main system bus
- ◇ 725/50, 75SGC expansion of the mainbus to the SGC expansion card
- ◇ SCSI-2 single-ended narrow bus (Fast on 725/100)

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32 MB modules
- ◇ Eight sockets
- ◇ 32 MB (2x16) minimum, 256 MB (8x32) maximum

Expansion slots

- ◇ 725/50, 75 Three EISA expansion-slots,
One slot for either a SGC (*EISA formfactor*) or EISA card.
- ◇ 725/100 One EISA expansion slot,
Three slots for either GSC (*EISA formfactor*) or EISA cards.

Storage

- ◇ One tray for one 3.5" Narrow SE 50-pin SCSI hard drive
- ◇ One tray for one 3.5" Floppy drive
- ◇ Two trays for one half-height 5.25" Narrow SE 50-pin SCSI drive each, externally accessible
- ◇ 725/100: Fast-Narrow drives

3.7.2 External ports

- ◇ SCSI-2 50-pin Narrow SE single-ended (Narrow-fast on 712/100)
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Ethernet AUI 15-pin
- ◇ VGA HD15
- ◇ 725/50, 75 HP-HIL connector for input devices
- ◇ 725/100 SMD-10 connector, to connect HIL/PS2 with a special adapter
- ◇ Four phone jacks (microphone, headphones, line-in and ?)

3.7.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 725/100 HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.05, 9.07), pre-Y2K
- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ HPBSD, original 4.3BSD Unix on PA-RISC (closed)
- ◇ Mach 4/Lites, research microkernel with 4.4BSD (with issues)
- ◇ MkLinux, research Linux with Mach microkernel
- ◇ OSF MK-PA, OSF/1 Unix port to PA-RISC

3.7.4 Benchmarks

System	SPEC95 int	SPEC95 fp
HP 9000 725/50	1.53	2.46
HP 9000 725/75	2.51	3.85
HP 9000 725/100	3.76	4.06

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.29: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP 9000 C110	PA-7200 120MHz	6.00	8.14
DEC Alphastation 250	DEC Alpha 21064A 266MHz	4.18	6.27
Siemens PCE-5S	Intel Pentium 100MHz	4.04	2.35
SGI Indy	MIPS R5000 150MHz	3.97	4.20
DEC AlphaStation 200	DEC Alpha 21064 100MHz	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	1.13	1.38

3.7.5 Documentation

- ◇ HP 9000 Model 725 Family, HP Workstation Group , Hewlett-Packard Company (1996: mirror accessed January 2024)

Product sheets

- ◇ HP Apollo Series 700 Model 725/50 and 725/75 Low-cost, High-performance Workstations, product brief, Hewlett Packard (August 1993, 5091-8228E) [hpmuseum](#)
- ◇ HP Apollo Series 700 Model 725/50 Workstations, product brief, Hewlett Packard (August 1993, 5091-584X) [hpmuseum](#)
- ◇ HP Apollo Series 700 Model 725/75 Workstations, product brief, Hewlett Packard (August 1993, 5091-8329E) [hpmuseum](#)
- ◇ HP 9000 Series 700 Model 715/725 Workstation Price & Configuration Guide, Hewlett Packard (August 1993, 5091-8811E) [hpmuseum](#)

3.8 HP 9000 735 and 755

HP 9000 735 and 755 were powerful technical and graphical PA-RISC workstations from the early 1990s. They use 32-bit HP PA-7100 or PA-7150 RISC processors—the latter reserved for the fast and expensive 735/125 and 755/125 versions with 125 MHz.

Both 735 and 755 use heavy desk-side cases with separate modules for I/O and CPU. These boards, along with EISA cages and storage subsystem are built into “sliders” that can be removed separately from the system.

735 and 755 have similar cases and architecture as their HP 9000/730 and 750 predecessors. They support a large set of I/O buses, expansion options and drives in an updated design. 735 were widely used as FDDI node in Convex computing clusters, 735/125 workstations were rather fast Unix computers of the early 1990s and one of the fastest ever running NeXTSTEP.

HP 9000 735 were apparently used by the US Navy as part of the TAC-3 framework contract (Tactical Advanced Computer), possibly as AN/TSQ-142 mission planning system for the EA-6B aircraft and the HP 9000 755 used in ATWCS for cruise missile planning (Tomahawk).

- ◇ HP 9000 735/99 were introduced in 1992 for \$37,395
- ◇ HP 9000 735/125 were introduced in 1992 for \$35,395 (SPU)
- ◇ HP 9000 755/99 were introduced in 1992 for \$58,995
- ◇ HP 9000 755/125 were introduced in 1992

3.8.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 735/99	PA-7100 PA-RISC 32-bit	99 MHz	256/256 KB off-chip
HP 9000 755/99	PA-7100 PA-RISC 32-bit	99 MHz	256/256 KB off-chip
HP 9000 735/125	PA-7150 PA-RISC 32-bit	125 MHz	256/256 KB off-chip
HP 9000 755/125	PA-7150 PA-RISC 32-bit	125 MHz	256/256 KB off-chip

Chipset

- ◇ HP ASP2 chipset
- ◇ HP Viper memory and I/O controller
- ◇ HP *Cutoff* ASIC, interfacing with memory (*Viper*) and I/O buses, provides address decoding, bus arbitration and interrupts
- ◇ HP *Shortstop* ASIC, coordinates data communication between the I/O buses and the mainbus
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ AMD Formac Plus Am79C830 FDDI controller

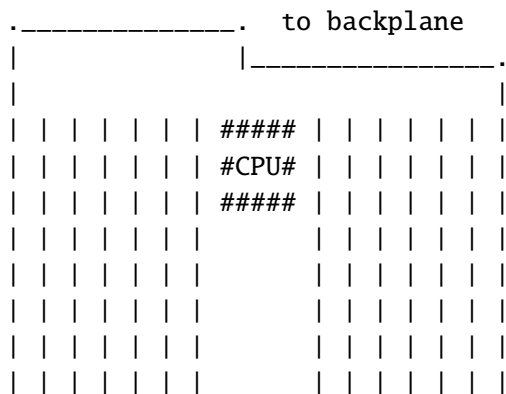
- ◇ Other I/O (serial, parallel, i8042)
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ Audio 16-bit CS4215 CODEC
- ◇ Graphics through separate boards:
 - *Optional* HP GRX SGC DIO-II video adapters
 - *Optional* HP CRX SGC DIO-II video adapters
 - *Optional* HP CRX-24 SGC DIO-II video adapters
 - *Optional* HP CRX-48Z SGC DIO-II video adapters

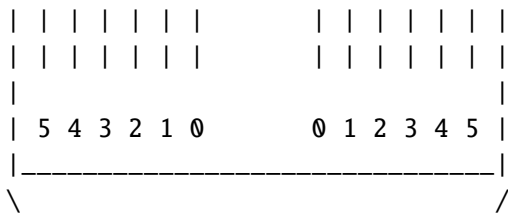
System buses

- ◇ PBus processor/memory bus, 66 MHz on 735/99 and 755/99 (264 MB/s)
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus
- ◇ EISA additional I/O expansion bus
- ◇ SGC expansion of the mainbus to the SGC expansion cards
- ◇ SCSI-2 narrow single-ended bus
- ◇ SCSI-2 Fast-Wide high-voltage differential (HVD) main storage I/O bus

Memory

- ◇ HP proprietary memory modules, same as 720, 730 and 750, and the Nova servers
- ◇ 8-32 MB modules
- ◇ 755 supports 64 MB modules
- ◇ 12 sockets
- ◇ 735 16 MB onboard, 400 MB maximum
- ◇ 755 768 MB maximum
- ◇ Memory has to be installed in pairs, from bank 0 to the outside





Expansion slots

- ◇ 735
 - One SGC in DIO-II formfactor
 - One EISA slot
 - One special daughter card slot for:
 - * A2665A - FDDI SAS daughter card with MIC connector
 - * A2658A - AUI Ethernet daughter card
 - * A2831A - ThinLAN Ethernet daughter card
- ◇ 755
 - Two SGC slots in DIO-II formfactor
 - Four EISA slots

Storage

- ◇ 735 one tray for either two 3.5" SCSI 68-pin Fast-Wide HVD or 50-pin narrow SE hard drives.
- ◇ 755 one tray for two half-height 5.25" SCSI drives and two trays for one full-height 5.25" SCSI drive each

3.8.2 External ports

- ◇ SCSI-2 50-pin single-ended external
- ◇ SCSI-3 68-pin Fast-Wide high-voltage differential HVD external
- ◇ Two standard RS232C serial
- ◇ DB25 parallel
- ◇ 735 15-pin AUI or 10Base2 BNC Ethernet or FDDI SAS MIC connector
- ◇ 755 15-pin AUI & 10Base2 BNC Ethernet connectors
- ◇ RGB BNC, depends on installed framebuffer, if at all
- ◇ HP-HIL connector for input devices
- ◇ Five phone jacks (microphone, headphones, line-in, line-out and speaker)
- ◇ Ten LEDs on the front for errors and status messages

3.8.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode, might work but unsupported
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.05, 9.07), pre-Y2K
- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ Research: HPBSD, original 4.3BSD on PA-RISC
- ◇ Research: Mach 4/Lites, microkernel with 4.4BSD
- ◇ Research: MkLinux, Linux with Mach microkernel
- ◇ Research: OSF MK-PA, OSF/1 Unix port to PA-RISC

3.8.4 Benchmarks

Table 3.31: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
HP 9000 735/99	PA-7100 99 MHz	109.1	167.9	3.22	4.06
HP 9000 755/99	PA-7100 99 MHz	109.1	167.9	3.22	4.06
HP 9000 735/125	PA-7150 125 MHz	136.0	201.0	3.97	4.61
HP 9000 755/125	PA-7150 125 MHz	136.0	201.0	3.97	4.61

Reviewers of new IBM RS/6000 offerings in Computerworld described the “raw power” of the 1994 IBM POWER2, however when compared against the 1992-vintage 735 “analysts noted that the HP 9000 735 still bested the 3BT with a SPECint92 rating of 136, vs. the IBM machine’s rating of 114.”

Table 3.32: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 150MHz	6.08	5.42
DEC Alphastation 250	DEC Alpha 21064A 266MHz	4.18	6.27
Siemens PCE-5S	Intel Pentium 100MHz	4.04	2.35
SGI Indy	MIPS R5000 150 MHz	3.82	4.78
IBM RS/6000 3CT	POWER2 67MHz	3.41	10.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	3.11	3.10
DEC AlphaStation 200	DEC Alpha 21064 100MHz	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	1.13	1.38

3.8.5 Documentation

Manuals

- ◇ HP 9000/735 Second Generation PA-RISC Snakes Workstation, Hewlett-Packard (IEEE paper, 1993) **bitsavers**
- ◇ HP Apollo 9000 Series 700 Model 735 Workstations Service Handbook, Hewlett Packard (1992, A2095-90602, edition 00893) **parisc-linux**
- ◇ HP 9000 Series 700 Model 735 Owner's Guide, Hewlett Packard (1992, A2095-90608, edition E0394) **hpmuseum**
- ◇ HP 9000 Series 700 Model 735 Hardware Installation Guide, Hewlett Packard (1992, A2095-90000, edition E0493) **hpmuseum**
- ◇ HP 9000 Series 700 Model 755 Owner's Guide, Hewlett Packard (1992, A2288-90607, edition E0894) **hpmuseum**

LED messages

- ◇ LED errors and status messages might be displayed on the HP 9000 735 and 755 front LEDs

Product sheets

- ◇ HP Apollo Series 700 Model 755 Workstation, two pager, Hewlett Packard (October 1992, 5091-9336E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 755 Workstation, product brief, Hewlett Packard (April 1993, 5091-5839E) **hpmuseum**
- ◇ HP 9000 Series 700 Model 735/125 Product Guide, Hewlett Packard (March 1994, 5962-8546E) **hpmuseum**
- ◇ HP Apollo Series 700 Model 735 and 735/125, product brief, Hewlett Packard (April 1993, 5091-5838EE) **hpmuseum**
- ◇ HP 9000 Series 700 Model 735 and 735/125, product brief, Hewlett Packard (March 1994, 5091-9898E) **hpmuseum**
- ◇ HP 9000 Series 700 Model 735CL Computational Cluster, product brief, Hewlett Packard (March 1994, 5962-8466E) **hpmuseum**

Articles

- ◇ The Art Of Computer Design, HP Professional, Hewlett-Packard (March 1997)
- ◇ IBM beefs up Unix boxes, Computerworld (1994, Volume 18, Issue 22)

3.9 HP 9000 742i, 742rt VME Workstation

HP 9000/742i are VME-based PA-RISC single-board computers based on HP 9000 715/50 workstations, released in 1992 by HP for instrumentation and measurement applications. The 742i computing logic is integrated onto a single VME board with many onboard devices but few expansion options.

SCSI is routed through the VME-P2 connector at the back of the board. Since the 742 features a VME controller, it can talk to other VME devices on the same VME bus (in VME cages) and control them.

The HP 742rt version of these VME computers was designed for the HP-RT realtime operating system but otherwise technically very close. The 745i and 747i VME computers in turn were based on very similar hardware to the 742i, but integrated into rugged VME cases with specific I/O options.

- ◇ HP 9000 742i were introduced in 1992 for \$8,000
- ◇ HP 9000 742rt were introduced in 1992

HP 74x VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” with end of support between 2003 and 2007.

3.9.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 742i	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip
HP 9000 742rt	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip

Chipset

- ◇ ASP chipset
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ Viper memory and I/O controller
- ◇ Intel 82350 EISA bus adapter chipset (EISA to GSC)
- ◇ CRX graphics, 8-bit
- ◇ CS4215 CODEC for 16-bit stereo audio
- ◇ VME bus adapter
- ◇ Other I/O (serial, parallel, i8042)

System buses

- ◇ PBus processor/memory bus
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus

- ◇ VME bus
- ◇ SCSI-2 narrow single-ended bus.

Memory

- ◇ 72-pin ECC SIMMs
- ◇ Takes 8-32 MB modules
- ◇ Two slots
- ◇ 16 MB (2×8) minimum, 64 MB (2×32) maximum

Expansion slots

- ◇ None

3.9.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ DB15 Ethernet AUI 15-pin

3.9.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode, might work but unsupported
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.01, 9.03, 9.05, 9.07), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ 742rt: HP-RT realtime 1.0 to 3.0

3.9.4 Benchmarks

System	SPEC95 int	SPEC95 fp
HP 9000 742i/50	1.53	2.46

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.35: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Siemens PCE-5S	Intel Pentium 100MHz	4.04	2.35
SGI Indy	MIPS R5000 150MHz	3.97	4.20
DEC AlphaStation 200	DEC Alpha 21064 100MHz	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	1.13	1.38

3.9.5 Dimensions

Height	Width	Depth	Weight	Power
40mm	233mm	160mm	0.9kg	35W @ 5V DC

3.9.6 Documentation

- ◇ HP 9000 Model 742i Owner's Guide (PDF, 0.5 MB, Hewlett Packard 1993) [parisc linux](#)
- ◇ VMEbus Single Board Computers and Industrial Workstations, Hewlett-Packard Company (1997: mirror accessed January 2024)

3.10 HP 9000 743i and 744 VME Workstations

HP 9000 743i and 744 workstations are VME single-board computers with 32-bit PA-RISC processors for use in VME computers, released between 1994 and 1997. They are based on HP 9000/715 and HP Visualize B132L/B160L workstations and integrated the system processing unit with memory and I/O controllers onto a VME board.

HP 9000 743i were used with HP-UX Unix in 748i VME workstations, HP 9000 744 boards in HP 9000 745 and 748 workstations but also supported HP-RT real-time in special models.

HP 9000 743i and 744 have on-board expansion options for very specialized and rare GSC-mezzanine (GSC-M) and PCI-mezzanine (PMC) cards, often used for graphics, SCSI or ATM networking. As VME computers, when installed into a VME cage (frame) with power and VME bus connections, HP 9000 743i and 744 can talk to and control other VME cards on the same VME bus, used for instrumentation and I/O.

HP 9000 74x VME were designed “hospital intensive-care systems” and “data and control functions for manufacturing, automotive, telecommunications, aerospace, medical and laboratory applications” but had many military uses.

HP 743rt and 744rt versions were sold with HP-RT realtime operating system, the sub-100µs response times critical “for a hospital system tied to a heart monitor, or a missile tracking system.”

V743rt in turn were real-time VXI embedded controllers, also sold with Agilent.

All HP 9000 74x VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” with end of support between 2003 and 2007, with HP-RT in a similar vein.

- ◇ HP 9000 743i/64 were introduced in 1994 for \$4,355
- ◇ HP 9000 743i/100 were introduced in 1994 for \$10,355
- ◇ HP 9000 743rt were introduced in 1994 for \$4,355
- ◇ HP 9000 744/132L were introduced in 1996
sold barebone for \$6,880 (HP-UX) to \$9,380 (HP-RT)
- ◇ HP 9000 744/165L were introduced in 1997
sold barebone for \$8,600 (HP-UX) to \$11,100 (HP-RT)
- ◇ HP 9000 744rt were introduced in 1996 for \$10,000 (developer kit)
- ◇ HP V743rt/64 (E1447A?) and Agilent V743/64 (E1497A) VXI were introduced in 1995
- ◇ HP V743rt/100 (E1447A?) and Agilent V743/100 (E1498A) VXI were introduced in 1995

US Navy TAC

HP 9000 743i and 744 VME computers were used by the US Navy through the TAC-4 program (Tactical Advanced Computer), in which HP was contracted to supply various PA-RISC workstation and server series to the Navy. 743i and 744 were used for tactical display and control applications like the AN/UYQ-70 workstation aboard surface and submarine vessels and surveillance aircraft. They used third-party VME devices, systems and graphics integration and FDDI networking.

V743 and Agilent VXI

HP 743 VME single-board computers were also sold for advanced measurement in the VXIbus, VME eXtension for Instrumentation bus. For this, the HP VME boards were adapted and modified for VXI bus interfaces and instrumentation, in cooperation with Agilent.

HP Agilent V743/64 and V743/100 VXI embedded computers are apparently very close to original VME 743i, integrated for VXI as single-slot, C-size, message-based computers with direct VXI access. They ran HP-UX Unix as operating system and C-SCPI and Agilent VEE.

There were apparently also V743rt/64 and V743rt/100 “High Performance Real-time VXI Embedded Controllers”, marketed without Agilent branding. They had direct VXI backplane access, were a C-Size VXI single slot module with VXI slot 0 (system) controller, graphics, 16 or 32MB RAM, various onboard I/O and SIDLrt. Mentioned in HP catalogues, it is unclear if they were ever really productized.

3.10.1 System architecture

Processors

System	CPU	Speed	Cache
HP 9000 743i/64	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 256 KB off-chip
HP 9000 743i/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip
HP 743rt	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 256 KB off-chip
HP V743rt/64	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 256 KB off-chip
HP 9000 V743rt/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip
HP 9000 744/132L	PA-7300LC PA-RISC 32-bit	132 MHz	128 KB on-chip
HP 9000 744/165L	PA-7300LC PA-RISC 32-bit	165 MHz	128 KB on-chip and 512 KB L2 off-chip
HP 9000 744rt/132L	PA-7300LC PA-RISC 32-bit	132 MHz	128 KB on-chip
HP 9000 744rt/165L	PA-7300LC PA-RISC 32-bit	165 MHz	128 KB on-chip and 512 KB L2 off-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ 744 HP Phantom PseudoBC GSC+ port
- ◇ 744 HP Visualize-EG “Graffiti” graphics with 2MB frame buffer memory
- ◇ CS4215 or AD1849 programmable CODECs
- ◇ VME controller
- ◇ PCMCIA controller
- ◇ *Integrated* Other I/O (serial, parallel, Floppy)

System buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 743i 8-256 MB RAM, with four slots for 8-64 MB special ECC mezzanine cards
- ◇ 744 64-1024 MB RAM, with four slots for 64-256 MB special ECC mezzanine cards
- ◇ V743 32-128 MB RAM
- ◇ 743i and 744 use different memory cards

Expansion slots

Some pins of the P2-VME connector are used to route GSC bus traffic to expansion options. VME cages need to be properly jumpered to support this to not interfere with these transfers. 743/744 boards must not be used in VXI cages since some of the VXI pins carry voltage which would result in damaged devices on the GSC bus.

- ◇ GSC bus expansion, through HP extender cards
- ◇ PCI and PCMCIA connector, through HP extender cards
- ◇ Expansion options for devices via expansion adapters:
 - Two GSC-mezzanine (GSC-M) cards, with the A4219A GSC Expansion kit that occupies one VME slot
 - Two PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board that occupies one VME slot
 - Two additional PCI-mezzanine (PMC) cards, requires PMC bridge adapter that occupies another VME slot
 - The PMC and GSC adapter cannot work together
- ◇ VME connection
- ◇ V743 VXI connection (TTL, ECL trigger buses)

3.10.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Two Serial micro-RS232C DB9[†]
- ◇ Micro-DB25 parallel[†]

- ◇ Micro-DB15 Ethernet AUI 15-pin[†]
- ◇ Micro-DB15 VGA graphics[†]
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout[†]
- ◇ V743 GPIB

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

3.10.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 v1 in 32-bit mode
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - 743iHP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - 743iHP-UX 9.07 (possibly also 9.05), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ 743rtHP-RT realtime 2.0 to 3.0
- ◇ V743HP-RT realtime 2.1 to 3.0
- ◇ 744rtHP-RT realtime 3.00/3.01

3.10.4 Benchmarks

System	SPEC95 int	SPEC95 fp
HP 9000 743i/64	2.52	3.31
HP 9000 743i/100	3.76	4.03
HP 9000 744/132L	6.45	6.70
HP 9000 744/165L	7.90	7.64

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.39: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20

DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
SGI Indy	MIPS R5000 150MHz	3.97	4.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	3.11	3.10
DEC AlphaStation 200	DEC Alpha 21064 100MHz	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	1.13	1.38

3.10.5 Documentation

Product features

- ◇ Agilent E1498A V743/100 VXI Embedded Computer - Datasheet (Agilent Technologies, 5965-6546E: 2001)
- ◇ VMEbus Single Board Computers and Industrial Workstations, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ Model V743rt: High Performance Real-time VXI Embedded Controllers, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ Model 744/132L and 744/165L Model 744rt/132L and 744rt/165L, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ Model 744 Configuration Options, Hewlett-Packard Company (1999: mirror accessed 2024)
- ◇ 744 and 744rt Ordering Guide (with prices), Hewlett-Packard Company (May 2000: mirror accessed 2024)
- ◇ Compatibility Matrix, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP 9000 Model V743rt catalogue entry, page 554 from:
HP Test & Measurement Catalog, Hewlett-Packard Company (1997: mirror accessed 2024)
[hparchive](#)

Manuals

- ◇ HP 9000 Model 743 Owner's Guide (PDF, 1.8 MB, Hewlett Packard 1997) [parisc linux](#)
- ◇ 743, 744 and 748 Technical Reference Manual for OEMs (PDF, 2.2 MB, Hewlett Packard 1997) [parisc linux](#)
- ◇ 744 Owner's Guide (PDF, 1.4 MB, Hewlett Packard 1997) [parisc linux](#)
- ◇ HP Model 748 Service Handbook (.pdf, 3.6 MB, Hewlett Packard 1997) [parisc linux](#)
- ◇ 743 Service Handbook (Hewlett Packard, URL gone)
- ◇ Installing the A4505A PCI Module Upgrade (Hewlett Packard, URL gone)
- ◇ Installing the A4504A PMC Bridge Adapter and A4509A Expansion Adapter (Hewlett Packard, URL gone)
- ◇ Installing Model 743 RAM Boards (Hewlett Packard, URL gone)
- ◇ Installing Model 744 RAM Cards (Hewlett Packard, URL gone)
- ◇ VME Services for HP-UX 10 and 11 (Hewlett Packard, URL gone)

Articles

- ◇ Navy pursues network-centric vision for shipboard electronics (Military & Aerospace Electronics: March 1998)
- ◇ HEWLETT ADDS ENHANCED RELEASE OF HP-RT FOR 9000 743, CBR Online Archive, August 25, 1994
- ◇ HEWLETT-PACKARD'S REAL-TIME HP-RT UP TO RELEASE 2.1, WITH TWO NEW SOFTWARE PACKAGES, CBR Online Archive, January 9, 1996
- ◇ HP UPGRADES RT REAL-TIME SYSTEM, CBR Online Archive, March 19, 1997
- ◇ HEWLETT HAS FIRST VME SINGLE-BOARD RISC COMPUTER, CBR Online Archive, June 6, 1994
- ◇ HP Real-Time Computer Automates Pharmaceutical Production, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP's real-time computing beats high-imaging speed, Hewlett-Packard Company (2000: mirror accessed 2024)

3.11 HP 9000 745 VME Workstations

HP 9000 745 PA-RISC VME industrial computers were released by HP in 1998 and integrated HP 9000 744 VME boards with 32-bit PA-7300LC PA-RISC processors into rugged VME case with integrated I/O. They were “rack-mountable, with built-in HP-IB, four EISA slots, excellent flexibility, completely compatible with all HP 9000 Series 700 controllers and workstations.”

Earlier HP 9000 745i were similar but used PA-7100LC processors.

745 had a case with room for up to four SCSI devices, a four-slot EISA or PCI cage and PCI-mezzanine expansion cards, via special so-called PMC bridges, that are quite rare these days. They were “designed for durability and reliability in harsh environments, and targets customers using compute-intensive applications in the military, and in test and measurement, telecommunications and manufacturing.”

- ◇ HP 9000 745/132L were introduced in 1998 for \$9,999
- ◇ HP 9000 745/165L were introduced in 1998

In the late 1990s, market enthusiasm for PA-RISC VME boards seemed limited. The 165 MHz version appears in technical documents but otherwise few public mentions exist. HP 9000 740 VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” .

3.11.1 System architecture

Processors

System	CPU	Speed	L1 cache	L2 cache
HP 9000 745/132L	PA-7300LC PA-RISC 32-bit	132 MHz	128 KB on-chip	
HP 9000 745/165L	PA-7300LC PA-RISC 32-bit	165 MHz	128 KB on-chip	512 KB off-chip

Chipset

- ◇ HP LASI chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Phantom PseudoBC GSC+ port
- ◇ HP Visualize-EG “Graffiti” graphics with 2MB frame buffer memory
- ◇ VME “Backplane controller ASIC”
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ *Integrated* Other I/O (serial, parallel, HP-HIL)

System buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 16-256 MB special ECC mezzanine cards (same as in 744 VME boards)
- ◇ Up to four cards can be installed
- ◇ 16 MB minimum, 1 GB maximum amount of RAM

Expansion slots

- ◇ Two sites for GSC-mezzanine (GSC-M) cards, requires A4219A GSC Expansion kit or
- ◇ Two sites for PCI-mezzanine (PMC) cards, requires A4504A PMC bridge board (two additional PMC sites can be obtained through the addition of the A4509A PMC Expander board to the above). The PMC bridge/expander boards connect to the VME backplane on a VME slot above the 744 processing board. They probably use GSC bus routed through the VME P1/P2 connectors, and not VME.
- ◇ Either four EISA or four PCI (5 V) slots in a separate I/O cage

Storage

- ◇ Four bays for external-accessible SCSI (SCSI-2 Single-ended) drives
- ◇ One bay for a 3.5" SCSI drive

3.11.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Two Serial micro-RS232C DB9*
- ◇ Micro-Parallel DB25*
- ◇ Micro-DB15 Ethernet AUI 15-pin*
- ◇ Micro-DB15 VGA graphics*
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout*

* - Note: These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

Other

- ◇ Refer also to the HP 9000 743i and 744 VME boards

3.11.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC

3.11.4 Benchmarks

System	SPEC95 int	SPEC95 fp
HP 9000 745/132L	6.45	6.70
HP 9000 745/165L	7.90	7.64

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.42: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20

3.11.5 Dimensions

Height	Width	Depth	Weight	Power
177mm	425mm	412mm	29kg	400W

3.11.6 Documentation

- ◇ HP Model 745 Technical Reference Manual (.pdf, 1.7 MB) Hewlett Packard (April 1999) **parisc linux**
- ◇ Model 745 Industrial Controller Owner's Guide (.pdf, 4.8 MB) Hewlett Packard (November 1999) **parisc linux**
- ◇ Model 745 Service Handbook (.pdf) Hewlett Packard (November 1999) **parisc linux**
- ◇ HP Test & Measurement Catalog 1999, Hewlett Packard 1999

- ◇ HP 9000 MODEL 745/132L UNIX WORKSTATION DEBUTS, The Free Library. 1998 World-wide Videotex
- ◇ VMEbus Single Board Computers and Industrial Workstations, Hewlett-Packard Company (1997: mirror accessed January 2024)

3.12 HP 9000 745i, 747i VME Workstations

HP 9000/745i and 747i were VME PA-RISC workstations from HP, released in 1992 for industrial control and medical use. They are technically close to HP 9000 715 and 725 workstations but integrated into (19") rack-mountable cases.

CPU and I/O controllers in these computers are based on integrated VME single board computers such as the 742i, used in both 745i and 747i. 747i are built into a bigger case with several VME expansion slots for devices, the 745i has a much smaller case and no expansion.

Both 745i and 747i have a HP-IB interface used for controlling, measurements and instrumentation devices. These machines have two pairs of LED banks, one at the front and the other directly on the CPU board on the back.

The similarly named HP 9000 745 (without i) were based on a newer hardware platform and PA-7300LC processors in the same case. HP 74x VME products were discontinued in 2002 as "customers have migrated to new solutions and platforms more rapidly than anticipated" with end of support between 2003 and 2007.

- ◇ HP 9000 745i/50 were introduced in 1992 for \$13,390
- ◇ HP 9000 745i/100 were introduced in 1992
- ◇ HP 9000 747i/50 were introduced in 1992 for \$15,990
- ◇ HP 9000 747i/100 were introduced in 1992

3.12.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 745i/50	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip
HP 9000 747i/50	PA-7100 PA-RISC 32-bit	50 MHz	128 KB off-chip
HP 9000 745i/100	PA-7100 PA-RISC 32-bit	100 MHz	512 KB off-chip
HP 9000 747i/100	PA-7100 PA-RISC 32-bit	100 MHz	512 KB off-chip

Chipset

- ◇ HP ASP chipset
- ◇ HP Viper memory and I/O controller
- ◇ NCR 53C700 8-bit single-ended SCSI-2
- ◇ Intel 82596DX 10 Mbit Ethernet controller
- ◇ Intel 82350 EISA bus adapter chipset
- ◇ HP CRX graphics, 8-bit
- ◇ HP-IB controller
- ◇ 747i VME controller
- ◇ PSB2160 CODEC for 8-bit mono audio

- ◇ Other I/O (serial, parallel, i8042)

System buses

- ◇ PBus processor/memory bus
- ◇ VSC main system bus
- ◇ GSC system-level I/O bus
- ◇ EISA I/O expansion bus
- ◇ HP-IB bus (IEEE-488); peripheral bus
- ◇ SCSI-2 narrow single-ended bus
- ◇ 747iSGC expansion of the mainbus to the SGC expansion slot
- ◇ 747i VME bus

Memory

- ◇ 72-pin ECC SIMM
- ◇ 8-32 MB modules (/100 models take 64 MB modules)
- ◇ Four sockets
- ◇ /50 models 16 MB (2×8) minimum, 128 MB (4×32) maximum
- ◇ /100 models 16 MB (2×8) minimum, 256 MB (4×64) maximum

Expansion slots

- ◇ 745i
 - Four EISA expansion slots
- ◇ 747i
 - Two EISA expansion slots
 - One SGC (*DIO-II formfactor*) expansion slot
 - Six VME slots

Storage

- ◇ One bay for an external-accessible 5.25" half-height SCSI drive
- ◇ One bay for an external-accessible 3.5" SCSI drive or floppy
- ◇ One bay for a 3.5" SCSI drive

3.12.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Ethernet AUI 15-pin
- ◇ HD 15 VGA
- ◇ HP-HIL connector for input devices
- ◇ HP-IB for peripherals
- ◇ Three phone jacks (microphone-in, headphone-out and speaker-out)

3.12.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode, might work but unsupported
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.01, 9.03, 9.05, 9.07), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NeXTSTEP, possibly

745i

3.12.4 Dimensions

System	Height	Width	Depth	Weight	Power
745i	175mm	425mm	412mm	18.6kg	350W
747i	310mm	425mm	412mm	29kg	700W

3.12.5 Benchmarks

System	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
745i/50	36	72	1.53	2.46
745i/100	81	138	3.22	4.06

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.47: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
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Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2	4.04	2.35
SGI Indy	MIPS R4400SC 75MHz	88.1	96.6		
SGI Indigo2	MIPS R4400SC 75MHz	85.9	93.6		
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
Digital DECpc XL	Intel Pentium 66MHz	51.6	47.5		
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
HP Vectra VL2	Intel 486DX 100MHz	45.8	23.1		
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		

3.12.6 Documentation

- ◇ 745i/50, 745i/100, 747i/50, and 747i/100 Owner's Guide (.pdf, 1.7 MB) Hewlett Packard (August 1993: First edition) **parisc linux**
- ◇ VMEbus Single Board Computers and Industrial Workstations, Hewlett-Packard Company (1997: mirror accessed January 2024)

3.13 HP 9000 748i, 748 VME Workstations

HP 9000 748i and 748 ruggedized PA-RISC workstations are HP 9000 743i and 744 VME boards built into a heavy VME case like the 747 with integrated I/O. The rugged VME cases were designed for “durability and reliability in harsh environments” and had built-in expansion options for six 6U VME slots for additional I/O boards, up to four SCSI devices and a four-slot EISA or PCI cage.

Model 748 was “exceptionally flexible and responsive”, based on 32-bit PA-RISC and compatible with other HP 9000 technology and applications.

Designed for instrumentation purposes, HP 9000 748, like the other HP PA-RISC VME computers, were often used in manufacturing, scientific but also military uses like ISR and targeting.

- ◇ HP 9000 748i/64 were introduced in 1994 for \$13,910
- ◇ HP 9000 748i/100 were introduced in 1994 for \$19,910
- ◇ HP 9000 748/132L were introduced in 1996 for \$12,000
- ◇ HP 9000 748/165L were introduced in 1997

HP 74x VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” with end of support between 2003 and 2007.

3.13.1 System architecture

Processors

System	CPU	Speed	L1 cache	L2 cache
HP 9000 748i/64	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 256 KB off-chip	
HP 9000 748i/100	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip	
HP 9000 748/132L	PA-7300LC PA-RISC 32-bit	132 MHz	128 KB on-chip	
HP 9000 748/165L	PA-7300LC PA-RISC 32-bit	165 MHz	128 KB on-chip	512 KB off-chip

Chipset

- ◇ HP LASI ASIC, which features:
 - ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
 - ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
 - ◇ HP Wax EISA bridge
 - ◇ HP Dino GSC-to-PCI bridge
 - ◇ 748 HP Phantom PseudoBC GSC+ port
 - ◇ 748 HP Visualize-EG “Graffiti” graphics with 2MB frame buffer memory
 - ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
 - ◇ VME controller
 - ◇ Other I/O (serial, parallel)

System buses

- ◇ GSC bus
- ◇ Optional EISA bus
- ◇ Optional PCI-32/33 bus
- ◇ VME bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 748i and 748 use different cards
- ◇ Up to four cards
- ◇ 748i 8-64 MB special ECC mezzanine cards, maximum 256 MB RAM
- ◇ 748 16-256 MB special ECC mezzanine cards, maximum 1 GB RAM

Expansion slots

- ◇ Two sites for GSC-mezzanine (GSC-M) cards, requires A4219A GSC Expansion kit or
- ◇ Two sites for PCI-mezzanine (PMC) cards, requires A4504A PMC bridge board (two additional PMC-sites can be obtained through the addition of the A4509A PMC Expander board to the above)
- ◇ Six 6U VME slots
- ◇ Either four EISA or four PCI slots in a separate I/O cage

3.13.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Two Serial micro-RS232C DB9[†]
- ◇ Micro-Parallel DB25[†]
- ◇ Micro-DB15 Ethernet AUI 15-pin[†]
- ◇ Micro-DB15 VGA graphics[†]
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Micro-DB9 for audio breakout[†]
- ◇ On configurations with an EISA cage: HIL connector

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

3.13.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 in 32-bit mode
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - 748iHP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - 748iHP-UX 9.07 (possibly also 9.05), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC

3.13.4 Benchmarks

System	SPEC95 int	SPEC95 fp
HP 9000 748i/64	2.52	3.31
HP 9000 HP 9000 748i/100	3.76	4.03
HP 9000 748/132	6.45	6.70
HP 9000 748/165L	7.90	7.64

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.50: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
SGI Indy	MIPS R5000 150MHz	3.97	4.20
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	3.11	3.10
DEC AlphaStation 200	DEC Alpha 21064 100MHz	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	1.13	1.38

3.13.5 Dimensions

Height	Width	Depth	Weight	Power
324mm	425mm	419mm	29kg	2×350W

3.13.6 Documentation

- ◇ Model 748 Workstation Owner's Guide (PDF, 3.2 MB, Hewlett Packard 1997) **parisc linux**
- ◇ 743, 744 and 748 Technical Reference Manual (PDF, 2.2 MB, Hewlett Packard 1997) **parisc linux**

- ◇ HP Model 748 Service Handbook (.pdf, 3.6 MB, Hewlett Packard 1997) **parisc linux**
- ◇ VMEbus Single Board Computers and Industrial Workstations, Hewlett-Packard Company (1997: mirror accessed January 2024)

Other

- ◇ Refer also to the 743i and 744 workstations

3.14 HP 9000 74x Expansion

3.14.1 743i and 748i (/64 and /100) RAM

Used in:

- ◇ 743i/{64,100}
- ◇ 748i/{64,100}

HP parts:

- ◇ A4263A - 8 MB RAM card
- ◇ A4264A - 16 MB RAM card
- ◇ A4265A - 32 MB RAM card
- ◇ A4266A - 64 MB RAM card

3.14.2 744, 745 and 748 (/132L and /165L) RAM

Used in:

- ◇ 744/{132L,165L}
- ◇ 745/{132L,165L}
- ◇ 748/{132L,165L}

Faster versions of the above 743i/748i ECC mezzanine cards.

Original HP part numbers:

- ◇ A4501A - 16 MB RAM card (only supported in HP-RT)
- ◇ A4502A - 32 MB RAM card
- ◇ A4503A - 64 MB RAM card
- ◇ A4449A - 128 MB RAM card
- ◇ A6005A - 256 MB RAM card

3.14.3 Cables

Breakout cables for the micro-connectors found on the 743i and 744 VME boards. These cables convert the micro-output to the regular connectors.

- ◇ HP A4300A HP Parallel: High Density 25-pin to standard 25-pin (female)
- ◇ HP A4301A RS-232C: High Density 9-pin to standard 9-pin (male)
- ◇ HP A4302A Audio: High Density 9-pin to three mini jacks

- ◇ HP A4303A LAN: High Density 15-pin to 15-pin AUI
- ◇ HP A4305A Video for EVC monitors: High Density 15-pin to EVC 35-pin connector (female)
- ◇ HP A4223A Video: High Density 15-pin to standard 15-pin (female)
- ◇ HP C2955A SCSI: High Density 50-pin to High Density 50-pin, .5m (male)

3.14.4 GSC-M cards

GSC-M cards are special mezzanine versions of expansion cards for the GSC bus.

- ◇ A4267A - 8-plane graphics
- ◇ A4268A - Fast-Wide high-voltage differential (HVD) SCSI
- ◇ A4315A - HCRX-8 graphics
- ◇ A4316A - HCRX-24 graphics
- ◇ J3420A - ATM card

3.15 HP 16600/16700 Agilent Logic Analyzers

HP 16600A and 16700A are logic analyzers with PA-RISC processors sold by HP and Agilent, based on PA-RISC HP 9000 workstation architecture from the mid-1990s. They were successors to Agilent 16500 series analyzers and used in engineering and science for measurements, logic analysis, prototyping and verification.

In electronics and microprocessor design, these systems were able to analyze buses (AGP, ISA, CAN, PCI, HP-PB, SCSI, USB, DIMM memory and many others) and emulate microprocessor families (ARM, IBM PowerPC, Pentium, Motorola PowerPC and MPC, CPU32, M-core, Toshiba, MIPS, Intel 960, Motorola 68000 and 88000).

All variants are based on the same 16700A or 16700B main logic board built into different chassis with system architecture related to B132L/B160L workstations with some custom I/O hardware.

- ◇ **16600A:** Small base system with integrated channel probes, one measurement slot and one emulation slot.
- ◇ **16700A:** Base system in a modular frame, with five measurement slots and two emulation slots.
- ◇ **16700B:** Updated 16700 base system with modular frame and faster mainboard.
- ◇ **16701A/16701B:** An “expansion frame” to extend the 16700 series systems with space for five more measurement and two more emulation slots.
- ◇ **16702A:** Same system board as the 16700 in a compact case as integrated Logic Analysis System with 10.3” 800x600 LCD screen display. With five measurement slots and two emulation slots.
- ◇ **16702B:** Updated version of the integrated 16702A with faster mainboard and components and a different case with integrated 12.1” touch screen. It lost the integrated keyboard on the front and one emulation slot at the back for an integrated CD drive.

Apparently, **Agilent E4406A Vector Spectrum Analyzer (VSA)** were also based on the same PA-RISC logic board:

- ◇ **E4406A:** Vector Spectrum Analyzer (VSA) apparently used for mobile protocol and device development and debugging (GSM, CDMA, EDGE) running HP-RT booting off a flash memory board. Apparently used the same processor boards as 16600/16700

Another Agilent PA-RISC product, **HP 16505A Prototype Analyzer**, was a standard HP 9000 712 workstation that connected to an Agilent 16500A series logic analyzer via special hardware and software.

- ◇ HP Agilent 16600A were introduced in 1998 for \$10,040-25,740
- ◇ HP Agilent 16700A were introduced in 1998 for \$9,990
- ◇ HP Agilent 16700B were introduced in 2000
- ◇ HP Agilent 16702A were introduced in 1999 for \$11,500
- ◇ HP Agilent 16702B were introduced in 2000 for \$11,990

Around 2004, Agilent moved away from PA-RISC and HP-UX to Windows and Intel.

3.15.1 System architecture

HP 16600 and 16700 series were an Agilent system design with individual boards:

- ◇ **CPU board:** The main logic board with PA-RISC processor, main ASICs, memory, backplanes and system slots
- ◇ **PCI board:** Bridges the PCI backplane from the CPU board to the instrument backplane for measurement modules. Extends the I/O circuitry from the CPU board and connects the Interface board
- ◇ **Interface board:** Distributes the signals from CPU and PCI boards throughout the system and connects to the measurement backplane, to which the measurement and emulation modules connect
- ◇ **Module interface board:** Connects the measurement and emulation slots and buses to the Interface board
- ◇ **Expansion frame:** Extends the measurement backplane to a separate frame with more slots

Processors

System	CPU	Speed	L1 cache
HP Agilent 16600A	PA-7300LC PA-RISC 32-bit	150 MHz	64 KB on-chip
HP Agilent 16700A	PA-7300LC PA-RISC 32-bit	150 MHz	64 KB on-chip
HP Agilent 16700B	PA-7300LC PA-RISC 32-bit	150 MHz	64 KB on-chip
HP Agilent 167020A	PA-7300LC PA-RISC 32-bit	150 MHz	64 KB on-chip
HP Agilent 16702B	PA-7300LC PA-RISC 32-bit	150 MHz	64 KB on-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Phantom PseudoBC GSC+ port
- ◇ (probably) HP Visualize-EG onboard graphics with 2 MB frame buffer memory (4 MB with the performance option 003)
- ◇ 30 MHz on-board crystal oscillator VCK
- ◇ PLL clock distribution IC
- ◇ Various ICs for the bridges and measurement and emulation ports
- ◇ FPGA1 (16700 BP protocol) on the PCI board
- ◇ FPGA1 (instrument BP protocol) on the PCI board
- ◇ Serial EPROM on the PCI board
- ◇ Intercard-controller on the Interface Board
- ◇ PLL, expansion frame circuitry, clock distribution on the Interface board

Display

- ◇ 16702A Integrated 10.3" 800×600 LCD display
- ◇ 16702B Integrated 12.1" 800×600 LCD touch panel
- ◇ All could optionally be ordered with a VGA monitor
- ◇ Supported 1280×1024 VGA monitor, 1600×1200 with option 003

Input

- ◇ 16702 series had build in input keys and devices
- ◇ 16702A Integrated front-panel keyboard
- ◇ 16702B Touch screen, knobs and dedicated hot keys

System buses

- ◇ GSC bus
- ◇ Optional PCI-32/33 bus for I/O devices and measurement and emulation modules
- ◇ IMB Inter-Module bus
- ◇ Protocol bus
- ◇ Measurement Module Backplane, Agilent 16500-compatible, connects via IMB, protocol bus to interface board
- ◇ Emulation Module Interface, connects via IMB, protocol bus to interface board
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ All logic analyzers had factory installed RAM that could be upgraded with factory options
- ◇ 120-pin memory expansion boards
- ◇ Apparently some memory is onboard
- ◇ 16700A and 16702A 64 MB to 160 MB internal RAM (with performance option 003)
- ◇ 16700B and 16702B 128 MB to 256 MB internal RAM (with performance option 003)

Expansion slots

- ◇ 16700A/16700B and 16702A/16702B expansion slots:
 - Five measurement module slots
 - Two emulation module slots
 - 16702B Only one emulation module slot

- ◇ 16600A expansion options:
 - One measurement module slot
 - One emulation module slot
 - Channel probes on the front
 - 16600A: 204 channels
 - 16601A: 136 channels
 - 16602A: 102 channels
 - 16603A: 68 channels
- ◇ 16701A and 16701B expansion slots, requires 16700 or 16702:
 - Five measurement module slots
 - Two emulation module slots

Storage

- ◇ SCSI 3.5" Fast-Narrow SE 50-pin factory-installed internal SCSI disk
- ◇ 3.5" Floppy drive
- ◇ 16700A/16702A 4 GB SCSI drive
- ◇ 16700B/16702B CD-ROM drive
- ◇ 16700B/16702B 9 GB SCSI drive
- ◇ E4406A flash memory board

3.15.2 External ports

- ◇ Ethernet LAN RJ45 and BNC
- ◇ 16702B 100BaseTX (Fast-Ethernet)
- ◇ SCSI-2 50-pin single-ended
- ◇ Serial RS232C DB9
- ◇ Parallel DB25
- ◇ VGA monitor
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ Target Control Port
- ◇ Port IN and Port OUT
- ◇ 16700/16702 Connector for 16701A expansion frame

3.15.3 Operating systems

- ◇ HP-UX with HP LOGIC and Agilent software
- ◇ They might run PA-RISC Linux and OpenBSD but not sure (the hardware is similar to already supported systems)
- ◇ *E4406AHP-RT*

More detailed pictures:

- ◇ 16700 Chassis Pictures at bitsavers.org, 2024 [bitsavers](#)
- ◇ 16700 PCB Pictures at bitsavers.org, 2024 [bitsavers](#)

3.15.4 Options

HP Agilent 16600 and 16700 series could be ordered with factory options.

Table 3.53: HP Agilent 16600 and 16700 factory options

Option	16600A	16700A/16702A	16700B/16702b
001	17" 1280x1024 monitor	17" 1280x1024 monitor	17" 1280x1024 monitor
003	160 MB system RAM, 4 MB video RAM	160 MB system RAM, 4 MB video RAM	256 MB system RAM, 4 MB video RAM
004	External CD-ROM drive	External CD-ROM drive	
008		18 GB external SCSI drive	18 GB external SCSI drive
009			External removable hard drive
010	Two 17-channel probe leads		
012			Multiframe module

3.15.5 Documentation

- ◇ HP 16700 Series Logic Analyser Page, Dave Partridge, n.d., with information on HP-UX 10.20 on Agilents
- ◇ Great series of articles on HP 16700A logic analyzer from "Keith" (2013: [techtravels.org](#))
- ◇ Agilent Technologies 16700A/16702A Service Guide (PDF) (2000: Agilent Technologies Company, mirror 2023) [bitsavers](#)
- ◇ HP 16600A and 16700A Series Logic Analysis System Mainframes Product Overview (1998: HP, 5966-3107E) [bitsavers](#)
- ◇ 16700 Series Logic Analysis System Product Overview (2003: Agilent) [bitsavers](#)
- ◇ Installation Guide HP 16600A Series HP 16700A HP 16702A Measurement Modules (PDF) (1999: Hewlett-Packard Company) [bitsavers](#)
- ◇ Training Kit for the Agilent Technologies 16700-Series Logic Analysis System (PDF) (2001: HP) [bitsavers](#)
- ◇ Agilent Technologies E4406A VSA Series Transmitter Tester Service Guide (PDF) (2006: Agilent Technologies) [bitsavers](#)

- ◇ Processor and Bus Support for Agilent Technologies Logic Analyzers (PDF) (2001: Agilent Technologies) **bitsavers**
- ◇ Don't be illogical when choosing logic-analysis tools Dan Strassberg (1999: EDN Network)
- ◇ HOT PRODUCTS OF 1998: Part 3 (1998: EDN Network)

3.16 HP 9000 A180

The HP 9000 A-Class A180 and A180C were some of the last 32-bit PA-RISC HP 9000 800 servers released by HP at the end of the 1990s in a small and rack-mountable case, often used for “Internet servers.”

Marketed by HP as “Enterprise Internet Servers” they were geared towards deployment in rack-space in datacenters, and thus have no video output, only serial console and a web console.

A-Class PA-RISC system design was pretty pared down and streamlined with a simple 32-bit PA-RISC design similar to the HP Visualize B180L workstations minus graphics and some I/O devices.

- ◇ HP 9000 A180 (A5182A) were introduced in 1998
- ◇ HP 9000 A180C (A5183A) were introduced in 1998 for \$16,000

The A180 servers were followed in 2000 by the newer 64-bit A400 and A500 servers, sharing their cases and external appearance but with more modern system design.

3.16.1 System architecture

Processors

System	CPU	Speed	L1 Cache	L2 Cache
HP 9000 A180	PA-7300LC 32-bit PA-RISC	180 MHz	64/64 KB on-chip	
HP 9000 A180C	PA-7300LC PA-RISC 32-bit	180 MHz	64/64 KB on-chip	1 MB off-chip

The additional 1 MB L2 cache is the only difference between both systems. It was upgradeable through two DIMM slots near the CPU.

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Phantom PseudoBC GSC+ port
- ◇ DEC 21142/43 10/100BaseT PCI Ethernet
- ◇ Other I/O (serial)

System buses

- ◇ GSC+ general system-level I/O bus (probably clocked at 36 MHz — 144 MB/s peak data rate)
- ◇ PCI high performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended; main storage I/O bus

Memory

- ◇ 72-pin ECC EDO SIMMs, 60ns or faster.
- ◇ Takes 64-256 MB modules
- ◇ Eight slots
- ◇ 128 MB (2×64) minimum, 2048 MB (8×256) maximum

Expansion slots

- ◇ Two slots for either GSC (*EISA formfactor*) or PCI cards

Storage

- ◇ One tray for two 3.5" Fast-Narrow 50-pin SCSI hard drives

3.16.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ Serial RS232C DB9
- ◇ Fast Ethernet RJ45
- ◇ Ethernet RJ45 "Web Console"

3.16.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, in EOE, FOE, MCOE version
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit, server version
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

HP 9000 A180C were used extensively in the development of PA-RISC Linux, for which HP provided support.

3.16.4 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp
HP 9000 A180	PA-7300LC 180 MHz	?	?
HP 9000 A180C	PA-7300LC 180 MHz	9.22	8.60

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.56: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.78
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
DEC Alphastation 500	DEC Alpha 21164 266MHz	7.93	11.1
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33

3.16.5 Documentation

Manuals

- ◇ User Manual HP 9000 Model A180, Hewlett Packard (February 2000, “aclassdocoo”) **parisc linux**
- ◇ HP’s HP9000 A-Class A180C Enterprise Server - Designed as a low-cost, high-density Web server, is the A-Class as mean as it is lean? Ralph Barker at *Dr. Dobb’s* (June 1999, accessed December 2017)

3.17 HP 9000 A400, A500 (rp2400)

HP 9000 A400 and A500 servers are 64-bit successors of the popular HP 9000 A180 rack servers. A400 were single-processor PA-RISC released in 2000, A500 up to two way multiprocessor-capable with better expandability.

A400 and A500 were part of the HP 9000 800 and Integrity server series that was later renamed **rp** and marketed as rp2400/rp2430/rp2405 (A400) and rp2450/rp2470/rp2405 (A500).

System design is based on 64-bit PA-RISC CPUs with large on-chip L1 caches, Astro memory/CPU controller and Elroy PCI bridges for expansion and I/O, a design similar to the HP Visualize C3000 line of workstations.

HP experimented with marketing of Unix servers in the 2000s – A400 were marketed as having “Screaming Performance” at a “Killer Price” with “Tight Internet Design”. Being “Street Smart”, A400 packed dotcom-era features for “Internet-edge Solutions” from WAP (phone browsers over GSM!) to e-commerce. “Your business is more aggressive than ever, so your server should be, too.”

- ◇ HP 9000 A400 rp2400 (A6109A, A6109B) were introduced in 2000 for \$4,600
- ◇ HP 9000 A400 rp2430 (A6889A) were introduced in 2000
- ◇ HP 9000 A400 rp2405 (A7121A) were introduced in 2002 for \$4,795
- ◇ HP 9000 A500 rp2450 (A5570A, A5570B) were introduced in 2000 for \$9,200
- ◇ HP 9000 A500 rp2470 (A6890A) were introduced in 2000
- ◇ HP 9000 A500 rp2405 (A7122A) were introduced in 2002

rp2405 were low-cost pre-configured servers released in 2002.

3.17.1 System architecture

Processors

Processors were designated by the [-44, -5X ... -9X] suffix.

System		CPU	Speed	L1 Cache
HP 9000 A400/rp2400	-44 -5X	PA-8500 PA-RISC 64-bit PA-8600 PA-RISC 64-bit	440 MHz 550 MHz	512/1024 KB on-chip 512/1024 KB on-chip
HP 9000 A400/rp2430	-6X	PA-8700 PA-RISC 64-bit	650 MHz	768/1536 KB on-chip
HP Integrity rp2405	-6X	PA-8700 PA-RISC 64-bit	650 MHz	768/1536 KB on-chip
HP 9000 A500/rp2450	-44 -5X	PA-8500 PA-RISC 64-bit PA-8600 PA-RISC 64-bit	440 MHz 550 MHz	512/1024 KB on-chip 512/1024 KB on-chip
HP 9000 A500/rp2470	-6X -7X	PA-8700 PA-RISC 64-bit PA-8700 PA-RISC 64-bit	650 MHz 750 MHz	768/1536 KB on-chip 768/1536 KB on-chip
HP Integrity rp2405	-6X	I-2 PA-8700 PA- RISC 64-bit	650 MHz	768/1536 KB on-chip

Possibly upgradeable to, unsure if shipped:					
	-8X -9X	PA-8700 64-bit PA-8800 64-bit <i>dual-core</i>	PA-RISC PA-RISC	875 MHz 1.0 GHz	768/1536 KB on-chip 1.5/1.5 MB on-chip 32 MB off-chip L2

Chipset

- ◇ HP Astro chipset memory controller, connects to system/processor bus (1-2 CPUs), memory bus and to I/O systems via five (A400) or seven (A500) I/O links
- ◇ A400 Three HP Elroy PCI bridges convert five I/O links into three PCI buses
- ◇ A500 Four HP Elroy PCI bridges convert seven I/O links into four PCI buses
- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C876 SCSI controller (two Symbios Logic 53C875 cores with each one Ultra-Wide SCSI-2 bus)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

System buses

- ◇ Runway CPU/memory bus, 120 MHz
- ◇ 1.9 GB/s system bus bandwidth
- ◇ 1.9 GB/s memory bandwidth
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD buses
- ◇ A400 Three independent PCI-64/66 I/O buses on five 250 MB/s I/O links
- ◇ A500 Four independent PCI-64/66 I/O buses on seven 250 MB/s I/O links

Memory

- ◇ ECC SDRAM DIMMs, 256 MB/512 MB/1 GB modules
- ◇ Eight slots, A400 uses only four
- ◇ A400 2 GB maximum
- ◇ A500 8 GB maximum

Expansion slots

- ◇ A400 Two PCI 64-bit/66 MHz, 5 V slots
- ◇ A500 Four PCI 64-bit/66 MHz, 5 V slots

Storage

- ◇ Two trays for each one 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector which require a special spud to be plugged into the system.

3.17.2 External ports

- ◇ SCSI-2 50-pin Ultra-Narrow single-ended
- ◇ SCSI-3 68-pin Ultra2-Wide LVD
- ◇ DB25 RS232C serial for console/UPS (break-out converts to three DB9 plugs)
- ◇ Fast Ethernet RJ45
- ◇ Ethernet RJ45 for Secure Web Console/GSP

3.17.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v2 in 64-bit mode
 - HP-UX 11i v1 in 64-bit mode, in EOE, FOE, MCOE version
 - HP-UX 11.00 in 64-bit mode
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s

3.17.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000rate int	SPEC2000rate fp
A500-5X(rp2450)	422	414	2-CPU: 9.3	2-CPU: 7.6
A500-7X(rp2470)	581		6.74 2-CPU: 12.9	

3.17.5 Dimensions

System	Height	Width	Depth	Weight
	95mm	482mm	635mm	23kg
Rack-mounted	2U	482mm	774mm	23kg

3.17.6 Documentation

Manuals

- ◇ Blazing Performance and Tight Internet Design, Product Brief, Hewlett-Packard Company (2000: 5968-9869EUC)
- ◇ Models of efficiency - hp servers running hp-ux , Brochure, Hewlett-Packard Company (2003: 5980-9959EN)
- ◇ hp servers rp2430 and rp2470 data sheet, Hewlett-Packard Company (2002: 5981-0170EN)
- ◇ hp server rp2400 series whitepaper, Hewlett-Packard Company (2002: 5981-0175EN)
- ◇ System Architecture and Design Guide A-Class Servers, Hewlett-Packard Company (1999/2000) [hpe](#)
- ◇ hp server rp2400 series whitepaper (URL gone)
- ◇ hp server rp2405 series whitepaper (URL gone)
- ◇ rp24xx Hardware Manual (URL gone)

Websites

- ◇ A-Class Product Overview Hewlett-Packard Company (2000: mirror accessed January 2024)
- ◇ A-Class Product Family Brochure Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ A-Class Street Talk Hewlett-Packard Company (2000: mirror accessed January 2024)
- ◇ Doug's HP 9000 - GSP Notes Page with a detailed description of the available GSP commands.
- ◇ Blazing Performance and Tight Internet Design Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP's Answer for Building World-Class Internet Infrastructure Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ A-Class Solution Ideal for E-commerce Deployment Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP's Answer for Carrier-Grade Next-Generation Network Deployments Hewlett-Packard Company (2000: mirror accessed 2024)

3.18 HP Visualize B132L, B160L, B180L

HP Visualize B-Class B132L, B160L and B180L were midrange and high-performance graphics workstations introduced in 1996 and 1997. Based on 32-bit PA-RISC processors, they were the successors to the popular 715 workstations with improved performance and I/O options for HP-UX Unix applications. B180L were introduced a year after the initial B132L and B160L as more powerful alternative.

B-Class were developed together with the HP Visualize C-Class workstations C132L/C160L, having similar design but more integrated functionality on the mainboard and fewer expansion options to minimize cost. The +-models B132L+ and B180L+ had faster Ultra-Wide SE SCSI and 100 Mbit Ethernet instead of Fast-Wide HVD SCSI and 10 Mbit Ethernet.

HP marketed these B-Class in 1996 as having “leadership integer performance and 2-D and 3-D graphics capabilities” for “complex design and analysis in mechanical design automation” such as MDA, EDA, remote sensing and GIS.

On the higher-end, B-Class were flanked by 64-bit C160/C180 and J-Class workstations. Many Visualize workstations including B-Class became widely available in the 2000s when Unix-based CAD/CAE was phased out in the industry and these workstations had solid support in open source operating systems.

- ◇ HP Visualize B132L, HP 9000/778, were introduced in 1996 for \$10,480
- ◇ HP Visualize B160L, HP 9000/778, were introduced in 1996 for \$16,480
- ◇ HP Visualize B180L, HP 9000/778, were introduced in 1997 for \$16,500

3.18.1 System architecture

Processors

Table 3.60: External L2 cache is optional, installed in two DIMM slots next to the CPU with modules of equal size. Usually, systems come with two 512KB modules âL2 1 MB L2. The L2 option cost around \$2,000 when ordering new.

System	CPU	Speed	L1 cache	L2 cache
HP Visualize B132L	PA-7300LC PA-RISC 32-bit	132 MHz	64/64 KB on-chip	1 MB off-chip optional
HP Visualize HP Visualize B132L+	PA-7300LC PA-RISC 32-bit	132 MHz	64/64 KB on-chip	1 MB off-chip optional
HP Visualize B160L	PA-7300LC PA-RISC 32-bit	160 MHz	64/64 KB on-chip	1 MB off-chip optional
HP Visualize B180L+	PA-7300LC PA-RISC 32-bit	180 MHz	64/64 KB on-chip	1 MB off-chip optional

Chipset

- ◇ HP LASI integrated chipset
- ◇ HP Phantom PseudoBC GSC+ port
- ◇ *Integrated*NCR 53C710 8-bit single-ended SCSI-2
- ◇ B132L, B160LNCR 53C720 16-bit Fast-Wide high-voltage differential SCSI-2

- ◇ B132L+, B180L+Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- ◇ B132L+, B180L+ DEC 21142/43 (*Tulip*) Fast-Ethernet controller
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Visualize-EG (“Graffiti”) graphics with 2MB frame buffer memory
- ◇ Other I/O (serial, parallel, Floppy)

System buses

- ◇ GSC general system-level I/O bus
 - B132L and B132L+: 33 MHz 132 MB/s
 - B160L: 40 MHz 160 MB/s
 - B180L+: 36 MHz 144 MB/s
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ B132L, B160L SCSI-2 Fast-Wide high-voltage differential main storage I/O bus
- ◇ B132L+, B180L+ SCSI-2 Ultra-Wide single-ended main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Six slots for 16-256 MB modules
- ◇ 32 MB to 1.5 GB supported

Expansion slots

- ◇ B132L, B160L:
 - One slot for GSC (EISA formfactor) or PCI 32-bit/33 MHz, 3.3 V cards
 - One slot for GSC (EISA formfactor), PCI 32-bit/33 MHz, 3.3 V or EISA cards
- ◇ B132L+, B180L+:
 - One slot for GSC (EISA formfactor) or PCI 32-bit/33 MHz, 5 V cards
 - One slot for GSC (EISA formfactor), PCI 32-bit/33 MHz, 5 V or EISA cards

Storage

- ◇ SCSI half-height 3.5" 68-pin hard drive, either Fast-Wide high-voltage differential (on B132L, B160L) or Ultra-Wide SE (on +-models)
- ◇ 3.5" Floppy drive
- ◇ SCSI half-height 5.25" 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible

3.18.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ B132L, B160L 68-pin HD SCSI-2 Fast-Wide high-voltage differential
- ◇ B132L+, B180L+ SCSI-3 68-pin Ultra-Wide single-ended
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ B132L, B160L Ethernet RJ45
- ◇ B132L+, B180L+ Fast Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ EVC graphics port, that needs a special HP adapter cable to convert to VGA
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)
- ◇ Four LEDs on the front for errors and status messages

3.18.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ QEMU, open-source computer emulator, supports a B160L

3.18.4 Dimensions

Height	Width	Depth	Weight
116mm	445mm	452mm	18kg

3.18.5 Benchmarks

System	SPEC95 int	SPEC95 fp	SPEC95rate int	SPEC95rate fp	SPEC2000 int	SPEC2000 fp
HP Visualize B132	6.45	6.70	58.1	60.3		
HP Visualize B132+	6.84	7.17	61.5	64.6		
HP Visualize B160L	7.75	7.56	69.7	68.1		
HP Visualize B180L+	9.22	9.43	83.0	84.8	87	60

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.63: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP Visualize C240	PA-8200 236 MHz	17.10	25.40
HP Visualize C160	PA-8000 160 MHz	10.40	16.30
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel SE440BX	Intel Pentium II 233MHz	9.38	7.40
IBM RS/6000 F50	PowerPC 604e 166 MHz	7.52	8.52
DEC Alphastation 600	DEC Alpha 21164 300MHz	7.33	12.2
Intel Alder	Intel Pentium Pro 166MHz	7.11	6.21
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
HP 9000 C110	PA-7200 120 MHz	6.00	8.14
DEC Alphastation 250	DEC Alpha 21064A 266MHz	4.18	6.27
SGI Indy	MIPS R5000 150MHz	3.97	4.20
HP 9000 712/100	PA-7100LC 100 MHz	3.76	4.06

3.18.6 Documentation

- ◇ Model B132L/B132L+/B160L/B180L Owners Guide (.pdf) Hewlett Packard, A4190-90023, September 1997 [parisc linux](#)
- ◇ Service Handbook B Class Model B132L/B132L+/B160L/B180L (.pdf) Hewlett Packard, A4190-90041, October 1997 [parisc linux](#)
- ◇ A Low-Cost Workstation with Enhanced Performance and I/O Capabilities (.pdf) Scott P. Allan et al (June 1997: Hewlett-Packard Journal)
- ◇ HP VISUALIZE Workstations Desktop Models B132L and B160L, HP Technical Computing , Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP B-Class Workstations, HP 1998, 5968-2860E

LED messages

- ◇ LED errors and status messages might be displayed on the HP B-Class front LEDs

ROM update

There is an firmware update available for the B-Class with the latest version 6.1:

- ◇ PF_CB1X0061.txt has details about contents and installation of the patch.

- ◇ CB1X0061.frm contains the patch.
- ◇ Both hosted at the PA-RISC Linux FTP server

3.19 HP Visualize B1000, C3000, C3600, C3700

HP Visualize B1000, C3000, C3600 and C3700 were late-1990s 64-bit PA-RISC workstations for the graphics and CAD on Unix markets. They used 64-bit HP PA-8500, PA-8600 and PA-8700 PA-RISC processors and were often used in technical design disciplines, before the market moved to Intel/Windows NT.

The architecture with HP Astro and Elroy PA-RISC chipsets was a major change from earlier Visualize workstations with new I/O devices added and no more LASI chipset and GSC bus— staples of 1990s PA-RISC. PCI and USB appeared.

Part of the HP 9000 Unix PA-RISC workstations, Visualize B-Class and C-Class were sold until the early 2000s as some of the last PA-RISC desktop computers, the end of an era. B1000 were the entry version whereas C3000 and C3600 were more powerful for 3D design. They were followed in 2004 by the last PA-RISC workstation, the HP c8000.

- ◇ HP Visualize B1000, HP 9000/785, were introduced in 1999 for \$9,900
- ◇ HP Visualize C3000, HP 9000/785, were introduced in 1999 for \$13,800
- ◇ HP Visualize C3600, HP 9000/785, were introduced in 2001 for \$12,243
- ◇ HP Visualize C3650, HP 9000/785, were introduced in 2001 for \$12,504
- ◇ HP Visualize C3700, HP 9000/785, were introduced in 2001 for \$15,915
- ◇ HP Visualize C3750, HP 9000/785, were introduced in 2001

3.19.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP Visualize B1000	PA-8500 PA-RISC 64-bit	300 MHz	512/1024 KB on-chip
HP Visualize C3000	PA-8500 PA-RISC 64-bit	400 MHz	512/1024 KB on-chip
HP Visualize C3600	PA-8600 PA-RISC 64-bit	552 MHz	512/1024 KB on-chip
HP Visualize C3650	PA-8700 PA-RISC 64-bit	625 MHz	768/1536 KB on-chip
HP Visualize C3700	PA-8700 PA-RISC 64-bit	750 MHz	768/1536 KB on-chip
HP Visualize C3750	PA-8700+ PA-RISC 64-bit	875 MHz	768/1536 KB on-chip

Chipset

- ◇ HP Astro memory/Runway controller
- ◇ Four HP Elroy PCI bridges
- ◇ National 87560 (*SuperI/O*) for USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)

- ◇ Symbios Logic 53C896 SCSI-3 controller
- ◇ Graphics through PCI boards:
 - *Optional*HP FireGL-UX 128 MB, PCI (“High-end 3D”)
 - *Optional*HP Visualize FX10pro 128 MB, PCI (“Midrange 3D”)
 - *Optional*HP Visualize FX5pro 64 MB, PCI
 - *Optional*HP Visualize FXe 18 MB, PCI (“2D & entry 3D:”)

System buses

- ◇ Runway CPU/memory bus
- ◇ PCI-32/33 device I/O bus
- ◇ PCI-64/33 high-performance device I/O bus
- ◇ PCI-64/66 high-performance graphics I/O bus
- ◇ C37x0PCI-64/100 high-performance graphics I/O bus
- ◇ SCSI-2 Ultra-Narrow single-ended external I/O bus
- ◇ SCSI-3 Ultra2-Wide LVD storage I/O bus
- ◇ IDE removable device I/O bus

Memory

- ◇ 278-pin 120 MHz ECC SDRAM DIMMs
- ◇ Eight slots for 128/256/512/1024 MB modules
- ◇ 128 MB to 8 GB supported

Expansion slots

- ◇ One PCI 64-bit/66 MHz, 3.3 V slot (clocked at 100 MHz on C37x0 systems)
- ◇ Three PCI 64-bit/33 MHz, 5 V slots
- ◇ Two PCI 32-bit/33 MHz, 5 V slots
- ◇ I/O slot layout (from top to bottom):
 1. PCI-64/33, pci0, 5 V
 2. PCI-64/66, pci1, 3.3 V (for primary graphics; on C37x0 systems this is a PCI-64/100 slot)
 3. PCI-64/33, pci0, 5 V
 4. PCI-64/33, pci2, 5 V (for secondary graphics)
 5. PCI-32/33, pci3, 5 V
 6. PCI-32/33, pci3, 5 V

Storage

- ◇ Two SCSI 3.5" Ultra2-Wide LVD hard drives with 80-pin SCA connector
- ◇ 3.5" Floppy drive
- ◇ Half-height IDE 5.25" drive, external accessible

3.19.2 External ports

- ◇ SCSI-2 50-pin Ultra-Narrow single-ended
- ◇ SCSI-3 68-pin Ultra2-Wide LVD
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Fast Ethernet RJ45
- ◇ Two USB ports for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

3.19.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 10.20 32-bit from version ACE9912 (C3700 will not work)
 - 11.00 64-bit from version ACE9911 (C3700: July 2001 plus PHKL_24484)
 - 11i v1 64-bit only in TCOE and MTOE versions (C3700: September 2001)
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC, in 32-bit mode
- ◇ NetBSD open-source Unix-like, ported to PA-RISC, in 32-bit mode
- ◇ QEMU, open-source computer emulator, supports C3700

3.19.4 Dimensions

System	Height	Width	Depth	Weight
Desktop	445mm	229mm	495mm	25kg
Rack-mounted	6U	451mm	665mm	25kg

3.19.5 Benchmarks

Table 3.66: Results with HP-UX 11.00

System	CPU	SPEC95 int	SPEC95 fp	SPEC95 rate int/fp	SPEC2000 int	SPEC2000 fp

HP Visualize B1000	PA-8500 300MHz	24.1	42.0	217/378		
HP Visualize C3000	PA-8500 400MHz	31.8	52.4	287/471	313	321
HP Visualize C3600	PA-8600 552MHz	42.1	64.0	379/576	432	433
HP Visualize C3650	PA-8700 625MHz				508	542
HP Visualize C3700	PA-8700 750MHz				604	576
HP Visualize C3750	PA-8700+ 875MHz				678	674

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.67: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP zx6000	McKinley 1.0 GHz	807	1422
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
SGI Origin 3200	MIPS R14000 600MHz	483	499
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610
HP Visualize P750C	Pentium III 750MHz	325	219
Compaq AlphaServer ES40	Alpha 21264 500MHz	311	382
HP Visualize P500	Intel Pentium III 500MHz	231	191

3.19.6 Documentation

- ◇ HP VISUALIZE B Class and C Class Owners Guide Hewlett Packard 2001 (PDF, 4.9 MB, A5992-90001 Edition E0501) **parisc linux**
- ◇ Service Handbook HP VISUALIZE B1000/C3000 UNIX Workstations, Hewlett Packard 2001 (A4985-90048 or E00501)
- ◇ VISUALIZE Workstation Memory Subsystem (PDF, 120 KB) **parisc linux**
- ◇ HP VISUALIZE B1000 UNIX Workstations, Hewlett Packard 1999, 5968-4835E
- ◇ HP c3700 and c3750 Workstations Data Sheet, Hewlett Packard 2005, 5982-1620EN
- ◇ The mass extinction of UNIX workstations, OSnews, Thom Holwerda, 12/2022
- ◇ VISUALIZE B1000, C3000 and J5000 Workstation Software Solution, Hewlett Packard 1999

3.20 HP Visualize B2000 and B2600

HP Visualize B2000 and B2600 PA-RISC workstations were 3D graphics workstations from 2000, equipped with the 64-bit PA-8500 or PA-8600 processors with large on-chip L1 caches.

HP B2000 used PA-8500 PA-RISC processors in a small tower case, similar to previous B1000 and C-Class. B2600 used a smaller desktop with faster and more modern PA-8600 processors.

The architecture of these B-Class workstation was a major change from those of its C-Class predecessors, now based on HP Astro/Elroy chipset, new I/O devices and no LASI I/O chip and GSC bus. All device I/O is implemented by PCI buses, human I/O devices are connected to USB ports.

An upgrade path to HP Itanium (EPIC VLIW) was envisaged for Visualize workstations but not offered eventually. B2000 and B2600 were some of the last PA-RISC workstations offered by HP, before the ultimate HP c8000 a few years later with the last PA-8800.

- ◇ HP Visualize B2000, HP 9000/785, were introduced in 2000 for \$5,075
- ◇ HP Visualize B2600, HP 9000/785, were introduced in 2000

3.20.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP Visualize B2000	PA-8500 PA-RISC 64-bit	300/440 MHz	512/1024 KB on-chip
HP Visualize B2600	PA-8600 PA-RISC 64-bit	500 MHz	512/1024 KB on-chip

There were some B2000 shipped with or upgraded to PA-8600 (PCXW+) processors.

Chipset

- ◇ HP Astro chipset memory/Runway controller
- ◇ Two HP Elroy PCI bridges
- ◇ National 87560 (SuperI/O) for USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip (on B2600 the audio card is optional)
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- ◇ Graphics through PCI boards:
 - *Optional* HP Visualize FX5pro 64 MB, PCI
 - *Optional* HP Visualize FXe 18 MB, PCI

System buses

- ◇ Runway CPU/memory bus
- ◇ PCI-32/33 device I/O bus
- ◇ PCI-64/33 high-performance I/O bus
- ◇ SCSI-3 Ultra2-Wide LVD bus main storage I/O
- ◇ IDE bus; removable device-I/O

Memory

- ◇ 278-pin 120 MHz ECC SD-RAM DIMMs
- ◇ Four slots for 128 MB-1 GB modules
- ◇ 128 MB to 4 GB supported

Expansion slots

- ◇ Two PCI 64-bit/33 MHz, 5 V slots (clocked at 66 MHz on B2600)
- ◇ Two PCI 32-bit/33 MHz, 5 V slots
- ◇ B2000 I/O slot layout, from top to bottom:
 1. PCI-64/33, 5 V
 2. PCI-64/33, 5 V
 3. PCI-32/33, 5 V
 4. PCI-32/33, 5 V
- ◇ B2600 I/O slot layout, from top to bottom:
 1. PCI-32/33, 5 V, short PCI cards
 2. PCI-32/33, 5 V, short PCI cards
 3. PCI-64/33, 5 V, short and full-length cards
 4. PCI-64/33, 5 V, short and full-length cards

Storage

- ◇ Two SCSI 3.5" Ultra2-Wide LVD hard drives with 80-pin SCA connector
- ◇ 3.5" Floppy drive
- ◇ IDE half-height 5.25" drive, external accessible

3.20.2 External ports

- ◇ B2000: VGA HD15
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Fast Ethernet RJ45
- ◇ Two USB ports for keyboard & mouse
- ◇ Four audio jacks (microphone, headphones, line-in and line-out) (on B2600 the audio card is optional)

3.20.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 11.11 64-bit, in TCOE and MTOE versions
 - 11.00 64-bit from version ACE99111 (July 2001)
 - 10.20 32-bit from version ACE9912 (plus PHCO_23042)
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC, in 32-bit mode
- ◇ NetBSD open-source Unix-like, ported to PA-RISC, in 32-bit mode

3.20.4 Dimensions

System	Height	Width	Depth	Weight
B2000	445mm	229mm	495mm	21kg
B2600	127mm	425mm	457mm	20kg

3.20.5 Benchmarks

Table 3.70: Results with HP-UX 11.00

System	CPU	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int/fp
HP Visualize B2000	PA-8500 440MHz	31.8	52.4	332	357	3.8/4.1
HP Visualize B2600	PA-8600 500MHz			403	440	4.7/5.1

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.71: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
SGI Origin 3200	MIPS R14000 600MHz	483	499

DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610
HP Visualize P750C	Pentium III 750MHz	325	219
Compaq AlphaServer ES40	Alpha 21264 500MHz	311	382
HP Visualize P500	Intel Pentium III 500MHz	231	191

3.20.6 Documentation

Manuals

- ◇ B2000 Service Handbook HP, (PDF, 8.8 MB) **parisc linux**
- ◇ B2000 Owner's Guide HP, (PDF, 2.6 MB) **parisc linux**
- ◇ B2600 Technical Reference Manual HP, (PDF, 33.0 MB) **parisc linux**
- ◇ VISUALIZE Workstation Memory Subsystem HP, (PDF, 120 KB) **parisc linux**

3.21 HP 9000 C100 and C110

HP 9000 C100 and C110 are PA-RISC graphics workstations based on the PA-7200 processor and were introduced in 1995. The C-Class were marketed as technical workstations for graphical use cases – CAD, CAE and visualization, and were pretty fast Unix desktop computers for their time.

HP billed these entry C-Classes as having “no-compromise, full computing power” to be used in “technical and design applications” with 2D and 3D graphics. HP 9000 C-Class have a similar case to the older HP 9000 735 workstations – interlocking I/O modules and CPU board, but are based on faster PA-7200 and U2.

There were other C-Class workstations with different designs: 32-bit C132L and C160L, 64-bit C160 and C180 and powerful C200 et al. Board upgrades of C100 and C110 were possible to C160 and C180.

- ◇ HP Visualize C100, HP 9000/777, were introduced in 1995 for \$19,715
- ◇ HP Visualize C110, HP 9000/777, were introduced in 1995 for \$25,715

3.21.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 C100	PA-7200 PA-RISC 32-bit	100 MHz	256/256 KB off-chip, 2 KB on-chip “assist”
HP 9000 C110	PA-7200 PA-RISC 32-bit	120 MHz	256/256 KB off-chip, 2 KB on-chip “assist”

Chipset

- ◇ HP U2 chipset Runway to GSC bridge
- ◇ HP MMC/SMC memory controllers
- ◇ HP LASI I/O chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ Graphics through separate GSC boards:
 - *Optional* HP HCRX GSC video adapter
 - *Optional* HP Visualize GSC video adapter
- ◇ Other I/O (serial, parallel, HP-HIL, Floppy)

System buses

- ◇ Runway CPU/memory bus
100 MHz 800 MB/s peak data rate on C100; 120 MHz, 960 MB/s on C110
- ◇ GSC general system-level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide high-voltage differential main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ 400 MB/s (C100), 480 MB/s (C110) peak bandwidth
- ◇ Eight slots for 16-128 MB modules
- ◇ 32 MB to 1 GB supported

Expansion slots

- ◇ One slot for a GSC (EISA formfactor) card
- ◇ Three slots for GSC (EISA formfactor) or EISA cards
- ◇ I/O slot layout (from top to bottom):
 1. EISA or GSC
 2. EISA or GSC
 3. EISA or GSC (for secondary graphics)
 4. GSC (for primary graphics)

Storage

- ◇ Storage and drives installed in the *disk slider*
- ◇ Three SCSI half-height 3.5" 68-pin hard drives, Fast-Wide high-voltage differential
- ◇ One SCSI half-height 5.25" 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible (this would take space from one internal hard drive)
- ◇ 3.5" Floppy drive

3.21.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ SCSI-3 68-pin Fast-Wide *differential* (HVD)
- ◇ Two serial RS232C DB9 (up 460.8Kb/s)
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ Graphics port depend on installed video adapter
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)
- ◇ Four LEDs on the front for errors and status messages

3.21.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9.07 (possibly), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ HPBSD research Unix operating system (closed)

3.21.4 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	21kg

3.21.5 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp	SPECrate95, int	SPECrate95, fp
HP 9000 C100	PA-7200 100 MHz	4.98	6.59	44.8	59.4
HP 9000 C110	PA-7200 120 MHz	6.00	8.14	54.0	73.3

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.75: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP Visualize C240	PA-8200 236MHz	17.1	25.4
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
SGI O2	MIPS R10000 196MHz	10.1	8.77
HP Visualize C160L	PA-7300LC 160MHz	7.75	7.56
DEC Alphastation 500	DEC Alpha 21164 266MHz	7.20	11.10
Intel Alder	Intel Pentium Pro 166MHz	7.11	6.21
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 250	DEC Alpha 21064A 266MHz	4.18	6.27
SGI Indy	MIPS R5000 150MHz	3.97	4.20
HP 9000 712/100	PA-7100LC 100MHz	3.76	4.06
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20

3.21.6 Documentation

Manuals

- ◇ C100/110 Owners Guide (.pdf), Hewlett Packard 1995, A4200-90014 [parisc linux](#)
- ◇ Service Handbook C Class (.pdf), Hewlett Packard 1998, A4200-90042 [parisc linux](#)
- ◇ HP 9000 C-Class Workstation Family Models C100 and C110, HP Technical Computing , Hewlett-Packard Company (1997: mirror accessed January 2024)

LED messages

- ◇ LED errors and status messages might be displayed on the HP C-Class front LEDs

3.22 HP Visualize C132L, C160L

HP Visualize C132L and C160L PA-RISC workstations were entry-level Unix workstations with integrated, low-cost PA-7300LC processors and LASI chipset. They have a similar case to that of the old HP 9000/735 workstation, built of interlocking modules for I/O board, MPU board etc.

C132L and C160L were close to the slightly older and less powerful C100/C110, which were PA-7200 based, and technically almost identical to the smaller and less expandable B132L/B160L workstations. PA-7300LC C160L was marketed by HP for “MDA, EDA, GIS, or software development” with “outstanding graphics and compute performance in an affordable and expandable system.”

A C180L is mentioned in documentation but it is unclear if ever existed. The very rare PA-RISC laptops from RDI, PrecisionBooks from 1998, were technically based on Visualize C132L, C160L and C180L workstation designs.

- ◇ HP Visualize C132L, HP 9000/779, were introduced in 1996
- ◇ HP Visualize C160L, HP 9000/779, were introduced in 1996 for \$19,480

3.22.1 System architecture

Processors

Table 3.76: The external L2 cache SRAM is optional and installed in two DIMM slots next to the CPU socket with modules of equal size. Usually, systems come with two 512 KB modules â 1 MB L2.

System	CPU	Speed	L1 cache	L2 cache
HP Visualize C132L	PA-7300LC PA-RISC 32-bit	132 MHz	64/64 KB on-chip	1 MB off-chip
HP Visualize C160L	PA-7300LC PA-RISC 32-bit	160 MHz	64/64 KB on-chip	1 MB off-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ GP Phantom PseudoBC GSC+ port
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ NCR 53C720 16-bit Fast-Wide *differential* (HVD) SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Visualize-EG graphics with 2MB frame buffer memory
- ◇ Graphics could be extended through separate boards:
 - *Optional* HP HCRX GSC video card
 - *Optional* HP Visualize GSC video card

- *Optional* HP Visualize-FX PCI video card
- ◇ Other I/O (serial, parallel, Floppy, HP-HIL)

System buses

- ◇ GSC-2 system and I/O bus (33 MHz with 132 MB/s peak data rate on C132L, 40 MHz 160 MB/s on C160L)
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide *differential* main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ 12 slots for 16-256 MB modules
- ◇ 32 MB to 2 GB supported

Expansion slots

- ◇ Two slots for GSC (EISA formfactor) or EISA cards
- ◇ One slot for a PCI 32-bit/33 MHz, 3V or EISA card
- ◇ One slot for a PCI 32-bit/33 MHz, 3V card
- ◇ Slot layout, from top to bottom:
 1. EISA or GSC
 2. EISA or GSC
 3. PCI-32/33.3 V or EISA
 4. PCI-32/33

Storage

- ◇ Storage and drives installed in the *disk slider*
- ◇ Three SCSI half-height 3.5" 68-pin hard drives, Fast-Wide high-voltage differential
- ◇ One SCSI half-height 5.25" 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible (this would take space from one internal hard drive)
- ◇ 3.5" Floppy drive

3.22.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ SCSI-3 68-pin Fast-Wide *differential* (HVD)
- ◇ Two serial RS232C DB9 (up 460.8Kb/s)
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ EVC graphics port, that needs a special HP adapter cable to convert to VGA
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)
- ◇ Four LEDs on the front for errors and status messages

3.22.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

3.22.4 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp	SPEC95rate int	SPEC95rate fp
HP Visualize C132L	PA-7300LC 132 MHz	6.45	6.70	58.1	60.3
HP Visualize C160L	PA-7300LC 160 MHz	7.75	7.56	7.75/7.56	69.7/68.1

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.78: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP Visualize C240	PA-8200 236 MHz	17.10	25.40
HP Visualize C160	PA-8000 160 MHz	10.40	16.30
SGI O2	MIPS R10000 196MHz	10.10	8.77
Intel SE440BX	Intel Pentium II 233MHz	9.38	7.40
IBM RS/6000 F50	PowerPC 604e 166 MHz	7.52	8.52
DEC Alphastation 600	DEC Alpha 21164 300MHz	7.33	12.2

Intel Alder	Intel Pentium Pro 166MHz	7.11	6.21
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
HP 9000 C110	PA-7200 120 MHz	6.00	8.14
SGI Indy	MIPS R5000 150MHz	3.97	4.20
HP 9000 712/100	PA-7100LC 100 MHz	3.76	4.06

3.22.5 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	21kg

3.22.6 Documentation

Manuals

- ◇ C160L Owners Guide (.pdf), Hewlett Packard 1996, A4200-90021 **parisc linux**
- ◇ Service Handbook C Class (.pdf), Hewlett Packard 1998, A4200-90042 **parisc linux**
- ◇ HP VISUALIZE Workstation Desktop Model C160L, HP Technical Computing , Hewlett-Packard Company (1997: mirror accessed January 2024)

LED messages

- ◇ LED errors and status messages might be displayed on the HP C-Class front LEDs

3.23 HP Visualize C160, C180

HP Visualize C160 and C180 were graphics workstations equipped with 64-bit PA-8000 processors, introduced in 1996. They were higher-end offerings with better CPUs and configurations compared to older HP Visualize C100, C110, or lower-cost C132L, C160L.

The case is similar to that of the HP 9000/735 workstation with interlocking modules. These machines were aimed at CAD/CAM/3D modelling and were succeeded by the powerful C200 and C240.

C160 and C180 were the first smaller 64-bit PA-RISC workstations for graphics applications and positioned by HP against Sun Ultra 2 and Silicon Graphics Indigo2 workstations for Unix technical computing. HP marketed them for “MDA, EDA, Exploration and Production, GIS, and Medical Imaging” as well as “fluid dynamics and structural analysis” as they had “outstanding floating point and graphics performance.”

- ◇ HP Visualize C160, HP 9000/780, were introduced in 1996 for \$24,000

- ◇ HP Visualize C180, HP 9000/780, were introduced in 1996 for \$50,000

C180 were sometimes marketed as C180-XP with included Visualize 48XP graphics adapter. 32-bit C100 and C110 were board-upgradable to C160 and C180.

3.23.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP Visualize C160	PA-8000 PA-RISC 64-bit	160 MHz	512/512 KB off-chip
HP Visualize C180	PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip

Chipset

- ◇ HP UTurn chipset Runway to GSC bridge
- ◇ HP MMC/SMC memory controllers
- ◇ HP LASI I/O chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Visualize-EG graphics with 2MB frame buffer memory
- ◇ Graphics could be extended through separate boards:
 - *Optional* HP HCRX GSC video adapter
 - *Optional* HP Visualize GSC video adapter

- *Optional* HP Visualize-FX PCI video adapter
- ◇ Other I/O (serial, parallel, Floppy, HP-HIL)

System buses

- ◇ Runway CPU/memory bus (120 MHz with 960 MB/s peak bandwidth)
- ◇ Cache: 128-bit wide bus between cache and CPU
 - C160: 2.56 GB/s I-fetch, 2.56 GB/s D-load (16-Byte), 1.26 GB/s D-store
 - C180: 2.88 GB/s I-fetch, 2.88 GB/s D-load (16-Byte), 1.44 GB/s D-store
- ◇ GSC-2 general system-level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ PCI-32/33 high-performance device I/O bus
- ◇ SCSI-2 single-ended bus
- ◇ SCSI-2 Fast-Wide high-voltage differential main storage I/O bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving
- ◇ 960 MB/s peak bandwidth
- ◇ 12 slots for 16-256 MB modules
- ◇ 32 MB to 3 GB supported

Expansion slots

- ◇ One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 3.3 V card
- ◇ One slot for a GSC (EISA formfactor), EISA or PCI 32-bit/33 MHz, 3.3 V card
- ◇ Two slots for GSC (EISA formfactor) or EISA cards
- ◇ I/O slot layout, from top to bottom:
 1. EISA or GSC
 2. EISA or GSC
 3. PCI-32/33, 3.3 V or EISA or GSC
 4. PCI-32/33, 3.3 V or GSC
- ◇ Often used for graphics applications with HP adaptors like Visualize-48

Storage

- ◇ Storage and drives installed in the *disk slider*
- ◇ Three SCSI half-height 3.5" 68-pin hard drives, Fast-Wide high-voltage differential
- ◇ One SCSI half-height 5.25" 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible (this would take space from one internal hard drive)
- ◇ 3.5" Floppy drive

3.23.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ SCSI-3 68-pin Fast-Wide *differential* (HVD)
- ◇ Two serial RS232C DB9 (up 460.8Kb/s)
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ EVC graphics port, that needs a special HP adapter cable to convert to VGA
- ◇ Two PS/2 connectors for keyboard and mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)
- ◇ Four LEDs on the front for errors and status messages

3.23.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 64-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 64-bit mode
 - HP-UX 10.20 32-bit
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

3.23.4 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	21kg

3.23.5 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp	SPEC95rate int	SPEC95rate fp
HP Visualize C160	PA-8000 160 MHz	10.40	16.30	93.6	147
HP Visualize C180	PA-8000 180 MHz	11.80	18.70	107	169

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.83: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP Visualize C240	PA-8200 236 MHz	17.1	25.4
SGI Origin 2000	MIPS R10000 250MHz 4MB	14.7	24.5
Sun Ultra 5 333	Sun UltraSPARC Iii 333MHz	14.1	18.3
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.78
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel SE440BX	Intel Pentium II 233MHz	9.38	7.40
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
HP Visualize C160L	PA-7300LC 160 MHz	7.75	7.56
IBM RS/6000 F50	PowerPC 604e 166 MHz	7.52	8.52
DEC Alphastation 600	DEC Alpha 21164 300MHz	7.33	12.2
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33

3.23.6 Documentation

- ◇ Model C160 / C180 / C200 / C240 / C360 Owner's Guide (.pdf), Hewlett Packard 1998, A4200-90050 **parisc linux**
- ◇ Service Handbook C Class (.pdf), Hewlett Packard 1998, A4200-90042 **parisc linux**
- ◇ HP VISUALIZE Workstations Power Desktop Models C160 and C180-XP, HP Technical Computing, Hewlett-Packard Company (1997: mirror accessed January 2024)

LED messages

- ◇ LED errors and status messages might be displayed on the HP C-Class front LEDs

ROM update

There is a firmware update available for the C160 and C180, which contains the latest version (6.2).

- ◇ PF_CC2X0062.text has details about the contents and installation of the patch **parisc linux**
- ◇ PF_CC2X0062.frm contains the patch **parisc linux**

3.24 HP Visualize C200, C240, C360

HP Visualize C200, C240 and C360 PA-RISC workstations were aimed at the late-1990s Unix graphics market, with powerful 64-bit PA-8200 and PA-8500 64-bit PA-RISC CPUs. They were based on earlier 32-bit Visualize C100/C110 workstations.

C-Class have a similar case to that of early-90s HP 9000 735 workstations with interlocking modules where I/O, CPU and other boards can be easily taken out. These newer 64-bit Visualize C-Class were graphics workstations aimed at CAD/CAM/3D modeling, and were at the time the fastest configurations of C-Class.

HP Visualize C200 and C240 were sometimes also called C200+ and C240+. HP marketed C-Class both the newer, late-1990s Visualize brand as well as the prior HP 9000 (700) naming scheme, going back to the 1990s.

- ◇ HP Visualize C200, HP 9000/782, were introduced in 1997 for \$21,000
- ◇ HP Visualize C240, HP 9000/782, were introduced in 1997 for \$46,000
- ◇ HP Visualize C360, HP 9000/785, were introduced in 1998 for \$22,365*

* List prices were moving a lot in 97-98 due to pressure from Windows NT workstations and HP adjusted prices often. Not sure this is right, though.

3.24.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP Visualize C200	PA-8200 PA-RISC 64-bit	200 MHz	512/1024 KB off-chip
HP Visualize C240	PA-8200 PA-RISC 64-bit	236 MHz	2048/2048 KB off-chip
HP Visualize C360	PA-8500 PA-RISC 64-bit	367 MHz	512/1024 KB on-chip

Chipset

- ◇ HP UTurn I/O adapter Runway to GSC bridge
- ◇ HP MMC/SMC memory controllers
- ◇ HP LASI integrated I/O chipset
- ◇ Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- ◇ DEC 21142/43 (*Tulip*) Fast-Ethernet controller
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ HP Dino GSC-to-PCI bridge
- ◇ HP Cujo GSC-to-PCI bridge, 64-bit

- ◇ Graphics could be extended through separate boards:
 - *Optional* Visualize GSC video adapters
 - *Optional* Visualize-FX PCI video adapters
- ◇ Other I/O (serial, parallel, Floppy)

System buses

- ◇ Runway CPU/memory bus (120 MHz with 960 MB/s peak data rate)
- ◇ GSC-2 general system-level I/O bus (256 MB/s)
- ◇ EISA (built to order option), additional expansion I/O
- ◇ PCI-32/33 device I/O bus
- ◇ PCI-64/66 high-performance device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ SCSI-2 Ultra-Wide single-ended bus main storage I/O

Memory

- ◇ 72-pin ECC EDO SIMMs, 50ns or faster
- ◇ 12 slots for 16-256 MB modules
- ◇ 32 MB to 3 GB supported

Expansion slots

- ◇ Three slots for GSC (EISA formfactor) or PCI cards
- ◇ One slot for a GSC (EISA formfactor), PCI or EISA card
- ◇ Two PCI slots are 32-bit/33 MHz, 5 V; the other two PCI 64-bit/66 MHz, 3.3 V. Some systems do not have the optional EISA slot
- ◇ I/O slot layout, from top to bottom:
 1. PCI-32/33, 5 V or EISA or GSC
 2. PCI-64/66, 3.3 V or GSC
 3. PCI-32/33, 5 V or GSC
 4. PCI-64/66, 3.3 V or GSC

Storage

- ◇ Storage and drives installed in the *disk slider*
- ◇ Three SCSI half-height 3.5" 68-pin hard drives, Ultra-Wide single-ended (SE)

- ◇ One SCSI half-height 5.25" 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible (this would take space from one internal hard drive)
- ◇ 3.5" Floppy drive

3.24.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ SCSI-3 68-pin Ultra-Wide single-ended
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Fast Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and ?)
- ◇ Four LEDs on the front for errors and status messages

3.24.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 v1 in 64-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 64-bit mode
 - HP-UX 10.20 32-bit (ACE 9707 and ACE 9806)
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

3.24.4 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	23kg

3.24.5 Benchmarks

Table 3.86: Results with HP-UX 10.20

System	CPU	SPEC95 int	SPEC95 fp	SPECrate95, int	SPECrate95, fp
HP Visualize C200	PA-8200 200 MHz	14.20	21.40	129	193
HP Visualize C240	PA-8200 236 MHz	17.10	25.40	156	229
HP Visualize C360	PA-8500 367 MHz	26.00	28.10	234	252

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.87: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
IBM RS/6000 44P 170	POWER3-II 400MHz	25.3	47.9
Siemens Celsius 2000	Intel Pentium II 450MHz	18.9	15.0
DEC Workstation 600au	DEC Alpha 21164 600MHz	18.4	21.3
SGI Origin 200	MIPS R12000 270MHz	15.8	25.2
Sun Ultra 5 333	Sun UltraSPARC Ili 333MHz	14.1	18.3
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.4
HP Visualize C180	PA-8000 180MHz	11.8	18.7
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.7
SGI O2	MIPS R10000 196MHz	10.1	8.7
Intel Alder	Intel Pentium Pro 200MHz	8.0	6.7
HP Visualize C160L	PA-7300LC 160MHz	7.7	7.5
HP 9000 C110	PA-7200 120MHz	6.0	8.1

3.24.6 Documentation

Manuals

- ◇ Model C160 / C180 / C200 / C240 / C360 Owner's Guide (.pdf), Hewlett Packard 1998, A4200-90050 **parisc linux**
- ◇ Service Handbook C Class (.pdf), Hewlett Packard 1998, A4200-90042 **parisc linux**

LED messages

- ◇ LED errors and status messages might be displayed on the HP C-Class front LEDs

3.25 HP C8000

HP c8000 is the last PA-RISC workstation produced by HP in 2004, with up to two dual-core PA-8800 *Mako* or PA-8900 64-bit processors. C8000 were the pinnacle of PA-RISC workstation design, released at a time when RISC workstations were on their way out.

HP produced a long line of C-Class Unix workstations, starting with 32-bit HP Visualize C100 in 1995 to C3750 in 2001 and finally c8000 in 2004, when Windows workstations with powerful PC graphics already took their place in CAD/CAM and 3D.

With an array of system and I/O options, the core of c8000 workstations is the HP *zx1* Itanium chipset, designed for HP Itanium workstations and servers. c8000 are built in a sleek, silent tower casing and also available as a rack-mount option.

HP c8000 were sold at the same time as Itanium workstations in the early 2000s, when HP offered Itanium zx2000 and zx6000 workstations with HP-UX Unix but also Windows 2000 and OpenVMS IA64.

- ◇ HP c8000 were introduced in 2004 for \$9,312

3.25.1 System architecture

Processors

System		CPU	Speed	L1 Cache
C8000	1-2	PA-8800 PA-RISC 64-bit dual-core	900 MHz-1.0 GHz	1.5/1.5 MB on-chip 32 MB off-chip L2
C8000	1-2	PA-8900 PA-RISC 64-bit dual-core	900 MHz-1.1 GHz	1.5/1.5 MB on-chip 64 MB off-chip L2

Chipset

- ◇ HP *zx1* chipset, on original HP Itanium design based on two main components: central memory and I/O controller (MIO), and I/O adapters (IOAs).
- ◇ HP Pluto, *zx1* MIO, the chipset controller connects the processor bus, two memory buses and seven I/O channels. Contains memory and cache controllers.
- ◇ Six HP Mercury, *zx1* IOAs, connect PCI-X slots and I/O devices to the *zx1* MIO on seven I/O channels (3.5 GB/s)
- ◇ Gigabit Ethernet controller
- ◇ Graphics through separate boards:
 - *Optional* ATI FireGL T2 128 MB, AGP
 - *Optional* ATI FireGL X1 256 MB, AGP
 - *Optional* ATI FireGL X3 256 MB, AGP
 - *Optional* HP fxe 18 MB, PCI
 - Other cards might or might not work
- ◇ Two-channel Ultra-320 SCSI controller
- ◇ UltraATA-133 IDE controller

- ◇ 8 MB Flash EEPROM

System buses

- ◇ Itanium 2/ZXT processor bus 6.4 GB/s
- ◇ Two ZXT memory buses, 266 MHz, 4.25 GB/s for 8.5 GB/s memory bandwidth
- ◇ Seven ZXT I/O channels/buses (“ropes”), aggregate 3.5 GB/s
 1. AGP 8X graphics on possibly two or more channels— 1.0 GB/s
 2. PCI-X 64/133 on possibly two channels— 1.0 GB/s
 3. PCI-X 64/66 and Ultra320 SCSI on one channel— 0.5 GB/s
 4. PCI 64/33, PCI 32/33, IDE and Ethernet on one channel— 0.5 GB/s
- ◇ AGP 8x graphics bus, 2133 MB/s
- ◇ PCI-X 64/133 I/O bus, 1066 MB/s
- ◇ PCI-X 64/66 I/O bus, 533 MB/s
- ◇ PCI 64/33 I/O bus, 266 MB/s
- ◇ PCI 32/33 I/O bus, 133 MB/s
- ◇ SCSI-3 Ultra320 (LVD) storage I/O bus, 320 MB/s
- ◇ UltraATA-133 IDE secondary storage I/O bus, 133 MB/s

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Up to 4 GB modules
- ◇ Eight slots
- ◇ 32 GB maximum
- ◇ 8.5 GB/s memory bandwidth
- ◇ 80ns memory latency

Expansion slots

All PCI slots are 3.3 V

1. PCI-32/33, short PCI cards
2. PCI-32/33, short PCI cards
3. AGP-8X Pro, 110W
4. PCI-64/33, short and full-length cards
5. PCI-64/66, short and full-length cards

6. PCI-64/66, short and full-length cards
7. PCI-64/133, short and full-length cards

Storage

- ◇ Four internal 3.5" bays for Ultra320 LVD SCSI drives with 68-pin connector
- ◇ Two internal 3.5" bays for UltraATA-133 IDE hard drives
- ◇ Three half-height 5.25" bays for externally accessible SCSI (LVD or SE) or UltraATA-133 drives

3.25.2 External ports

- ◇ Two serial RS232C DB9
- ◇ Five USB 2.0 ports (two in front, three in rear)
- ◇ TP/RJ45 Gigabit Ethernet
- ◇ Four phone jacks (microphone, headphones, line-in and line-out) on optional 16-bit audio card

3.25.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - I11 V1 TCOE (Technical Computing Operating Environment)
 - I11 V1 MTOE (Minimal Computing Operating Environment)
 - X11 graphics drivers are included for HP Visualize and some ATI 3D adapters
- ◇ PA-RISC Linux, not all video adapters are supported for X11 and not as stable as HP-UX

3.25.4 Dimensions

System	Height	Width	Depth	Weight
Tower	490mm	287mm	572mm	22.5kg
Rack-mounted	5U	424mm	572mm	21.9kg

Power output 650W

3.25.5 Benchmarks

HP c8000 workstations with PA-8800/PA-8900 processors were very fast PA-RISC computers Benchmark results were never published, probably not to interfere with Itanium workstations.

Table 3.90: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
HP c8000	PA-8800 1.0 GHz	1001 (est.)	

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.91: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
AMD	Opteron 250 2.4GHz	1619	1652
HP zx6000	Madison 1.5 GHz	1315	2106
Intel	Pentium 4 520 2.8GHz	1290	
HP ProLiant BL40p	Intel Xeon 2.8GHz	1249	1081
AMD	Athlon XP 2.2GHz	1080	873
HP zx6000	McKinley 1.0 GHz	807	1422
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
HP Visualize C3750	PA-RISC PA-8700+ 875 MHz 2.2MB	678	674
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610

3.25.6 Documentation

- ◇ HP Workstation c8000 Technical Reference Guide, HP 2004, 5969-3188
- ◇ Alternative: HP Workstation c8000 Technical Reference Guide, HP kernel.org
- ◇ QuickSpecs HP c8000 Workstation, HP 2007, DA 12134
- ◇ HP Workstation c8000 Product Overview, HP 2004, 5982-5771EN
- ◇ HP Workstation c8000 Product Design Highlights, HP 2004
- ◇ HP PA-RISC Workstations Options, HP 2005, website
- ◇ Hardware and Software Setup HP workstation c8000, HP Januar 2004, AB629-90001, [mirror](#)

3.26 HP 9000 D-Class and R-Class

HP 9000 D-Class servers were flexible, upgradable and scalable PA-RISC enterprise servers for Unix applications of the late-1990s. They were designed to bring “mid-range performance for an entry-level price,” with processors from 32-bit PA-7100LC to 64-bit PA-8200 and some multi-processing SMP support, released in 1996-1998.

All D-Class servers were HP 9000 800 server series and used two different architectures: LASI for PA-7100LC and PA-7300LC models and U2/UTurn for PA-7200/PA-8000 models. They were built into a mid-tower case for use as a departmental server. Still rather big and loud machines for the late-1990s.

R-Class “Ultralight” servers R380 and R390 are rack-mountable versions of their D-Class counterparts D380/D390. They are technically almost identical, except some differences in the I/O and storage configuration.

D-Class were technically close to the larger K-Class servers.

In the 1990s, D-Class servers were part of the US Navy TAC-4 program, in which HP was a vendor supplying RISC Unix computers for uses throughout the Navy. The D-Class were part of a technology refreshment of TAC-4 in 1996.

Different models were available which could be upgraded within the series to another model with various options for each system. The servers used the following naming convention and were part of the HP 9000 800 series:

- ◇ The first digit after “D” : 2 or 3, indicates the general D-Class type — D2x0 were smaller servers, D3x0 bigger with more expansion and options.
- ◇ Following digits 00, 10, ... 90 indicate system features like CPU and chipset.
- ◇ R380/R390 are R-Class rack-mountable servers for 19” racks.

System	Model number	Introduced	Price
D200, D300	HP 9000/801	January 1996	
D210, D310	HP 9000/811	January 1996	\$6,900
D220, D320	HP 9000/803, HP 9000/813	January 1997	\$8,900
D230, D330	HP 9000/823, HP 9000/833	January 1997	\$16,700
D250, D350	HP 9000/821, HP 9000/831	January 1996	
D260, D360	HP 9000/841, HP 9000/851	May 1996	
D270, D370	HP 9000/861, HP 9000/871	November 1996	
D280, D380	HP 9000/810, HP 9000/820	September 1997	
D390	HP 9000/800	July 1998	\$30,000
R380, R390	HP 9000/800	September 1998	

3.26.1 System architecture

Processors

HP 9000 D-Class shipped with a variety of PA-RISC processors – three types of 32-bit CPUs and two 64-bit.

System	CPU	Speed	L1 cache
D200 D300	PA-7100LC PA-RISC 32-bit	75 MHz	1 KB on-chip and 256 KB off-chip
D210 D310	PA-7100LC PA-RISC 32-bit	100 MHz	1 KB on-chip and 256 KB off-chip

D220	D320	PA-7300LC PA-RISC 32-bit	132 MHz	64/64 KB on-chip plus 1 MB L2 off-chip optional
D230	D330	PA-7300LC PA-RISC 32-bit	160 MHz	64/64 KB on-chip plus 1 MB L2 off-chip optional
D250	D350	1-2 PA-7200 PA-RISC 32-bit	100 MHz	256/256 KB off-chip, 2 KB on-chip "assist"
D260	D360	1-2 PA-7200 PA-RISC 32-bit	120 MHz	1/1 MB off-chip, 2 KB on-chip "assist"
D270	D370	1-2 PA-8000 PA-RISC 64-bit	160 MHz	512/512 KB off-chip
D280	D380	1-2 PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
D390	R390	1-2 PA-8200 PA-RISC 64-bit	240 MHz	2/2 MB off-chip

Chipset

D-Class used different chipsets and systems architectures, depending on used processors. There were actually four different processor and system bus setups.

- ◇ PA-7200 models HP U2 chipset Runway to GSC bridge
- ◇ PA-7300LC models HP Phantom PseudoBC GSC+ port
- ◇ PA-7200/PA-8000 models HP MMC/SMC memory controllers
- ◇ PA-8000 models HP UTurn chipset Runway to GSC bridge
- ◇ HP LASI I/O chipset
- ◇ Integrated NCR 53C710 8-bit single-ended SCSI-2
- ◇ Integrated Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit audio
- ◇ HP Wax EISA bridge
- ◇ D3x0 NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ D390/R380/R390 DEC 21140 Fast Ethernet controller
- ◇ Other I/O (serial, parallel)

System buses

- ◇ PA-7200/PA-8000 Runway CPU/memory bus
- ◇ GSC+ bus for the general system level I/O
- ◇ EISA expansion bus
- ◇ D3x0 SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage
- ◇ SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Note: Fast-Wide differential bus was optional on D2x0 models.

Memory

- ◇ 72-pin ECC SIMMs
- ◇ PA-7100LC 512 MB maximum in four slots

- ◇ PA-7200/PA-8000 1.5 GB maximum in six slots
- ◇ Systems with a PA-8000/PA-8200 need 50ns RAM modules, PA-7200/PA-7300LC take up to 60ns, PA-7100LC even slower modules

Expansion slots

- ◇ *D2x0*
 - One slot for GSC/HSC cards (EISA formfactor)
 - Two slots for EISA cards
 - Three slots for GSC/HSC or EISA cards
- ◇ *D3x0*
 - One slot for GSC/HSC cards (EISA formfactor)
 - Three slot for EISA cards
 - Four slots for GSC/HSC or EISA cards
- ◇ *R380/R390*
 - One slot for GSC/HSC cards (EISA formfactor)
 - Four slot for EISA cards
 - Three slots for GSC/HSC or EISA cards

Storage

- ◇ Up to three 5.25" 50-pin Fast-Narrow SE SCSI half-height drives, external accessible
- ◇ *D2x0/R3x0* Up to two Fast-Narrow 50-pin SCSI-2 single-ended hard drives
- ◇ *D3x0* Five hot-swap trays for Fast-Wide 68-pin SCSI-2 high-voltage differential drives
- ◇ *R380/R390* One 5.25" 50-pin Fast-Narrow SE SCSI half-height drive, external accessible

3.26.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ TP/RJ45 10BaseT 10 Mbit Ethernet
- ◇ Two serial RS232C DB9, one for console, one for USV
- ◇ Parallel DB25
- ◇ Two PS/2 connectors for keyboard und mouse

3.26.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit or 64-bit mode, in EOE, FOE, MCOE version
 - HP-UX 11.00 in 32-bit or 64-bit mode
 - HP-UX 10.20 32-bit, server version
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC (D220, D230, D320, D330)
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC (D200, D210, D220, D230, D300, D310, D320, D330)

3.26.4 Benchmarks

System	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp	SPEC95rate int	SPEC95rate fp
HP 9000 Dx00	115	146	2.18	2.90	19.2	25.8
HP 9000 Dx10	152	194	3.74	4.08	33.6	36.7
HP 9000 Dx20			6.57	6.72	59.2	60.5
HP 9000 Dx30			7.87	7.58	70.8	68.3
HP 9000 Dx50	144	218	5.01	6.77	45.1	61.0
HP 9000 Dx60					114	143
HP 9000 Dx70			10.40	15.00	93.9 2P:184	135 2P:190
HP 9000 Dx80			12.30	17.40	111 2P:219	157 2P:221
HP 9000 D390			15.50	25.50		

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.95: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
DEC Alphastation 500	DEC Alpha 21164 500MHz	15.0	20.4
SGI Origin 2000	MIPS R10000 250MHz 4MB	14.7	24.5
Sun Ultra 5 333	Sun UltraSPARC IIi 333MHz	14.1	18.3
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.78
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
Siemens PCE-5S	Intel Pentium 100MHz	4.04	2.35
SGI Indy	MIPS R5000 150MHz	3.97	4.20
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	3.11	3.10

3.26.5 Documentation

Manuals

- ◇ D-Class and R-Class Installation Guide (URL gone)
- ◇ D-Class and R-Class Operator's Guide (URL gone)
- ◇ D-Class and R-Class System Upgrade Guide (URL gone)

Articles

- ◇ An Entry-Level Server with Multiple Performance Points (.pdf) Lin A. Nease et al (June 1997: Hewlett-Packard Journal)

3.27 HP 9000 E-Class

HP 9000 E-Class were 32-bit PA-RISC servers from the 800 series sold in the mid-1990s as replacements for older F and G-Class Nova servers. Designed by HP's technical server division for reduced manufacturing cost, they were closely aligned with HP 9000/712 but still used a distinct server architecture.

HP 9000 E-Class servers and 712 workstations were complementary products— E-Class as central database and compute servers with the closely integrated 712 as client workstations.

The E-Class case was taken over almost without changes from F-Class, with CPU, memory and many I/O systems being new. Only networking and few other functions were used from the integrated LASI chipset— due to time constraints a modified version of F-Class HP-PB “Personality boards” was used for SCSI, MUX and parallel.

HP 9000 E-Class were positioned by HP in the 1994 Unix server market against IBM RS/6000 POWER-based 220, 230 and 250 and the Sun SPARCclassic and SPARCstation 10.

- ◇ HP 9000 E25, HP 9000/806, were introduced in 1994 for \$6,000
- ◇ HP 9000 E35, HP 9000/816, were introduced in 1994
- ◇ HP 9000 E45, HP 9000/826, were introduced in 1994 for \$11,320
- ◇ HP 9000 E55, HP 9000/856, were introduced in 1995

3.27.1 System architecture

Processors

System	CPU	Speed	L1 Cache
HP 9000 E25	PA-7100LC PA-RISC 32-bit	48 MHz	1 KB on-chip and 64 KB off-chip
HP 9000 E35	PA-7100LC PA-RISC 32-bit	64 MHz	1 KB on-chip and 256 KB off-chip
HP 9000 E45	PA-7100LC PA-RISC 32-bit	80 MHz	1 KB on-chip and 256 KB off-chip
HP 9000 E55	PA-7100LC PA-RISC 32-bit	96 MHz	1 KB on-chip and 1024 KB off-chip

Chipset

- ◇ LASI as central I/O chipset
- ◇ Wax EISA bridge
- ◇ HP-PB bus converter, 8 MHz HP-PB frequency
- ◇ HP ASICs for HP-PB, SCSI and MUX port

System buses

- ◇ Memory attaches directly to the PA-7100LC processors
- ◇ GSC as the main system bus (128 MB/s) that connects CPU, LAN, I/O and HP-PB
- ◇ HP-PB device and I/O bus (32 MB/s)

- ◇ Integrated I/O Card attaches to HP-PB with SCSI, serial and parallel
- ◇ SCSI-2 Fast-Narrow single-ended bus; main storage I/O

Memory

- ◇ 72-pin ECC SIMMs, 8-64 MB modules
- ◇ Eight slots
- ◇ 16 MB minimum, 512 MB maximum

Expansion slots

- ◇ Two slots for HP-PB cards

Storage

- ◇ One tray for two 3.5" Fast-Narrow SE 50-pin SCSI hard drives
- ◇ One tray for three half-height 5.25" Fast-Narrow SE 50-pin drives, externally accessible

3.27.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ High-pin-count MUX connector
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ Parallel DB25

3.27.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 in 32-bit mode, might work but unsupported
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.04?, 9.06), pre-Y2K
- ◇ PA-RISC Linux: very limited hardware support (no SCSI and other)
- ◇ NetBSD: very limited hardware support (no SCSI, only serial and other)

E-Class used a proprietary 800 series system design like older F and G-Class Nova servers for which few architecture specifications were released by HP. There has never been much support in open source operating systems.

3.27.4 Benchmarks

System	CPU	SPEC92 int	SPEC92 fp	MIPS
HP 9000 E25	PA-7100LC 48 MHz	45.0	66.7	45
HP 9000 E35	PA-7100LC 64 MHz	65.6	98.5	66
HP 9000 E45	PA-7100LC 80 MHz	82.1	122.9	82
HP 9000 E55	PA-7100LC 96 MHz	108.0	163.4	108

Comparison to SPEC benchmark data from other contemporary Unix computers:

Table 3.98: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp
IBM RS/6000 43P	PowerPC 604 100 MHz	128.0	120.2
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2
HP 9000 I50	PA-7000 96 MHz	100.0	158.5
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2
SGI Indy	MIPS R4400SC 75MHz	88.1	96.6
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2
HP 9000 G40	PA-7000 64 MHz	65.2	91.3
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1
IBM RS/6000 355	IBM POWER 41MHz	40.7	83.3
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	16.1
HP 9000 F20	PA-7000 48 MHz	33.6	56.1
Motorola 8000	Motorola 88100 33MHz	27.7	18.8

3.27.5 Documentation

- ◇ Development of a Low-Cost, High-Performance, Multiuser Business Server System (PDF, HP Journal 4/95)
- ◇ HP 9000 E-Class Servers Product Brief, Hewlett-Packard Company (1993, 5091-8997E) [hpmuseum](#)
- ◇ HP 9000 New product Summary guide, technical sales document, first part is on 712, Hewlett Packard: 1993 1000bit.it
- ◇ HP 3000 and HP 9000 PA-RISC Computer Systems CE Handbook Hewlett-Packard Company (1993, A2051-90003) [bitsavers](#)

3.28 HP 9000 500 FOCUS

With Frank McConnell

HP 9000 500 computers were the first members of the HP 9000 series in the early-1980s and predecessors of PA-RISC workstations. Introduced in 1982, the HP 9000 500 were based on a modern 32-bit HP processor, the HP FOCUS. PA-RISC was developed only a few years later by HP.

The HP 9000 520, originally marketed as 9020, was the first computer of the HP 9000 workstation range. The Hewlett Packard Journal described it in 1983 as “the new HP 9000 computer, a mainframe on the desktop.” Four 500 series were released: 520, 530, 540 and 550; all used the same HP FOCUS CPU, memory and I/O; differences were casing, expandability and built-in I/O.

- ◇ HP 9000 520 *Dawn* were introduced in 1982 for \$30,000
- ◇ HP 9000 530 *Corona* were introduced in 1982 for \$23,105
- ◇ HP 9000 540 *Corona* were introduced in 1982 for \$24,115
- ◇ HP 9000 550 *Shuttle* were introduced in 1984

The HP 9000/500 series was phased out in the late 1980s, probably due to the complexity and cost of its architecture. It was replaced by HP PA-RISC (700/800 series) and M68K (300/400 series) computers with HP-UX. The first PA-RISC NMOS processor had one third the amount of FETs of the FOCUS processor in a much more streamlined design.

The HP 9000 520 was used widely by the US Navy from the mid-1980s in the DTC as desktop computer for tactical uses. Originally called Desk-Top Computer in 1982, the DTC program later became Desktop Tactical Computer (DTC-1) and looked at using commercial COTS desktop computers for tactical decision support in US Navy facilities and ships.

After an evaluation in the Navy the contract was awarded to HP, after which the 9020C version (520 workstation with 13" monitor) became widely deployed throughout the US Navy. It apparently “served on US nuclear submarines well into the 1990s.” The 9020C was also part of the US Navy Joint Operational Tactical System, JTOS: (from the HP Computer Museum, Bill Reed)

"Despite the fact that some naval leaders didn't see the point of JOTS, at one time, almost every tactical or fleet staff in the United States Navy had five or more HP 9000s, often networked together. Some had the early projection systems for common displays. There was a sharing of the load, so to speak. The computers gave those that processed anti-submarine warfare what they wanted on one terminal while those involved with anti-air warfare processed on another computer. The technology that ensued included special interface boards capturing radar systems, communications systems and aircraft systems, many connected with fiber optics."

3.28.1 Systems

Four models were introduced between 1982-1984 with the same architecture:

System	Processor	Cache	RAM	Design	I/O	Storage	Price	Introduced
520	1-3 FO-CUS 18 MHz	16 KB	10 MB	IOP	GP-IO	10 MB	\$30,000	1982

	9020A: 12" color mon- itor with 512x390 resolution							
	9020B: 12" monochrome (green) mon- itor with 560x455 resolution							
	9020C: 13" color mon- itor with 560x455 resolution							
	9020AS (bundled system): 9020A with 1 MB RAM, 10 MB hard drive, thermal printer, HP BASIC							
	9020AT (bundled system): 9020A with 1.5 MB RAM, thermal printer, HP-UX operating system							
530	I-3 FO- CUS 18 MHz	16 KB	10 MB	IOP	GP-IO	10 MB	\$23,105	1982
	9030A: base system 19" rack- mount							
540	I-3 FO- CUS 18 MHz	16 KB	10 MB	IOP	GP-IO	10 MB	\$24,115	1982

	9040A: base system, free-standing cabinet system							
	9040AT (bundled system): 9040A with 1.5 MB RAM, HP-UX operating system (single-user)							
	9040AM (bundled system): 9040A with 1.5 MB RAM, HP-UX operating system (multi-user)							
550	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP + DSP	HP-IB	10 MB		1984
	9050A: base system, industrial system that replaced 530 and 540							
	9050AT (bundled system): 9050A with 1.5 MB RAM, HP-UX operating system (single-user)							

	9050AM (bundled system): 9050A with 1.5 MB RAM, HP-UX operating system (multi- user)	
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HP 9000 500 computers in multi-processor configuration were called 600 series (some HP 9000 800 servers were later called 600 series for a time).

Possible I/O and expansion options

- ◇ HP-IB card for external HP-IB (HP Instrumentation Bus) devices
- ◇ GP-IO card for GP-IO (General Purpose I/O) devices with 8-bit or 16-bit DMA
- ◇ Asynchronous Serial
- ◇ I/O Expander for eight I/O channels/slots (CIO) for additional IOPs
- ◇ LAN 9000, 10 Mbit Ethernet (coax)

3.28.2 Software

Two operating systems were provided by HP for the HP 9000 520 in 1982: HP BASIC or HP-UX, while the later 530, 540 and 550 supported only HP-UX, which was supported between versions 1.0 and 5.3 on HP FOCUS hardware.

The operating systems were built on top of a common kernel, called **SUNOS** (no relation to Sun SunOS Unix) which provided basic operating primitives like memory, processor and I/O management. This was intended to be invisible to the user; the Unix operating system on top ran as a single process on it.

There were three revision of SUNOS:

SUN I OS

- ◇ Kernel for BASIC language system on Dawn (the 9000/520)
- ◇ Single user
- ◇ No virtual memory
- ◇ Supports only HP “Focus” (*i.e.*, HP’s own) memory boards
- ◇ Only for HP 9000/520

SUN II OS

- ◇ Supports both HP BASIC and HP-UX (at that time a port of System III Unix)
- ◇ Multiple users
- ◇ Virtual memory

- ◇ Supports only HP “Focus” (*i.e.*, HP’s own) memory boards
- ◇ For HP 9000/520, 530 and 540

SUN III OS

- ◇ Updates for new hardware
- ◇ Multiple users
- ◇ Virtual memory
- ◇ Supports both HP “Focus” (*i.e.*, HP’s own) and commercial third-party memory boards
- ◇ For HP 9000/520, 530, 540 and 550

HP-UX for the HP 9000 500 computers was the first commercial UNIX supporting a multi-processor, multi-user system in the early 1980s. SMP for PA-RISC was supported only much later in HP-UX.

3.28.3 Benchmarks

Assorted MIPS performance figures for early HP 9000 800 servers.

Table 3.100: Based on old HP data

System	CPU	MIPS
HP 9000 500	FOCUS 18 MHz	0.98

Comparison to SPEC benchmark data of other Unix servers:

Table 3.101: Based on old Dhrystone and MIPS archives

System	CPU	MIPS	SPEC89
HP Apollo DN10000	Apollo PRISM 18 MHz	22	19
DECstation 3100	MIPS R2000 16MHz	15.1	11.8
HP 9000 835	NS-1 PA-RISC 30 MHz	14	9.5
Intel	i386 33MHz	8	4.3
HP 9000 840	TS-1 PA-RISC 8 MHz	4.5	
IBM PC 6150	IBM ROMP 6MHz	2.1	
HP 9000 320	Motorola M68020 15MHz	2.0	
DEC VAX 11/780	KA780 3.4MHz	0.9	1.01.0 SPEC92
Apple Macintosh	68000 7.8MHz	0.4	
IBM PC AT	Intel 80286 6MHz	0.8	
IBM PC XT	Intel 8088 4.7MHz	0.2	
Commodore C64	MOS 6510 1MHz	0.02	

- ◇ FOCUS CPU and systems boards, FOCUS CPU and rear, NMOS-III, Wikipedia, Thomas Schanz 2013

3.28.4 Documentation

Manuals

- ◇ HP 9000 Series 500 Computers Models 520, 530, 540, 550 Hardware Technical Data (.pdf) Hewlett Packard (November 1984) **hp museum**
- ◇ 9050 CE Handbook for the HP 9000 Series 500 (.pdf) Hewlett-Packard Company (1985) **hp museum**
- ◇ *OVERVIEW SUN III O.S.*, Hewlett Packard (Version 1.0/September 1984: Hewlett Packard)

Articles

- ◇ An 18-MHz, 32-bit VLSI Microprocessor (.pdf, pp. 7-10) Kevin P. Burkhart (August 1983. Hewlett Packard Journal. Accessed January 2008) **hp museum**
- ◇ *HP-9020C/AN/UYK-43 Study*, US Navy (1987. Defense Technical Information Center. Unclassified, accessed at)
- ◇ Hewlett-Packard 9000 Series 520 Frank McConnell (1997. Accessed January 2008)
- ◇ HP Computer Museum - Technical Desktops - 9000/520 Jon Johnston (WordSong Communications P/L. Accessed 15 January 2008 and December 2019)
- ◇ Re: HP 9000/500 vs. Vectra with 386 CPU and 387 co-processor? Roger N. Clark (28 July 1988: USENET posting comp.sys.hp)
- ◇ Introducing more computing power per engineer - The HP 9000 Model 550 (PDF) Hewlett-Packard, Januar 1985, accessed January 2023 **100obit.it**
- ◇ HP 9825 Timeline - 1981, Steve Leibson, September 2006

Pictures

Pictures Hewlett Packard, scans from product brochures, from hpmuseum.net and 100obit.it

3.29 HP Apollo Domain 10000

The Apollo Domain 10000 from Apollo Computer were marketed as “personal supercomputer” geared for complex workstation applications like electronic design automation (EDA) and mechanical computer-aided design and engineering (MCAD/MCAE). The Domain 10000 were designed and sold by Apollo Computer, a technical computing market leader in the 1980s, based on their own PRISM RISC architecture, before HP bought Apollo and integrated it into the HP 9000 lineup.

Apollo Computer was bought by HP at the end of the 1980s, taking over their product lineup with a plan on integrating technical computers (HP 9000 and Apollo) and software ecosystem. The Apollo workstation series was carried on for a few years under HP/Apollo branding; HP integrated Apollo as their workstation business unit with Apollo co-branding on the HP 9000 RISC workstations for a while but Apollo products and technology were phased out soon after and HP concentrated on its own PA-RISC computers and architecture.

- ◇ Apollo DN10000 workstations were introduced in 1988 \$79,900-\$235,900
- ◇ Apollo DSP10000 servers were introduced in 1988 for \$69,900-\$225,900
- ◇ Apollo 10010 are single-CPU, 10020 dual-CPU, 10030 3-CPU and 10040 4-CPU

Even though DN10000 and PRISM were soon phased out in its product lineup, HP communicated an upgraded PRISM processor and Apollo hardware in 1989. HP envisaged double the computing power (from 22 to 44 MIPS), increased caches to 512/512 KB, increased memory to 512 MB using 4 Mb DRAMs and up to 18 GB of SCSI storage, called the “DN10000TX upgrade” in 1991 – which apparently never shipped.

3.29.1 System architecture

Processors

System	CPU	Speed	L1 Cache
Domain 10000	1-4 PRISM RISC 32-bit	18 MHz	128/64 KB on-chip

Chipset

Domain DN10000 and DSP10000 are based on Apollo PRISM, a 32-bit RISC architecture on a system backplane with central and expansion slots. Processors, memory and high-performance graphics are attached to the central X-bus. A central service processor (MC68020) also attaches to the X-bus and controls the VME and ISA I/O buses for devices and peripherals.

- ◇ PRISM processors 1-4 attach to X-bus
- ◇ Memory 1-3 attach to X-bus
- ◇ FDDI networking attaches to X-bus
- ◇ Graphics engine attaches to X-bus
- ◇ Service processor and I/O attaches to X-bus

System buses

- ◇ X-bus, processor/memory bus – system backplane with 160 MB/s data rate
- ◇ VME main bus for I/O – for disk and network controllers
- ◇ ISA (“PC/AT”) bus for I/O – graphics and peripherals
- ◇ ESDI for storage I/O, SCSI was an option

Memory

- ◇ Apollo proprietary memory boards plug into X-bus slots, each taking two slots
- ◇ Up to three memory boards with each up to four 64 MB daughter boards
- ◇ 16 MB minimum, 128 MB maximum with parity, (704/720 MB theoretically)

Expansion slots

- ◇ Eight X-bus slots (shared with processor and memory boards)
 - 40-plane graphics option for 3D drawing, using one slot (1280x1024)
 - 80-plane graphics option for 3D drawing, using two slots (1280x1024)
 - FDDI dual attach
 - 68020, 12 MHz on Utility board
 - Communications controller with 2 X.25 and SNA ports
- ◇ Four ISA slots (“PC-AT”)
 - IBM Token Ring card
 - Simple 8-plane graphics if configured as workstation (1024x800)
 - QIC tape controller: Western Digital WD7000
- ◇ Six or five VME slots (depending on VME extension)
 - Ethernet card (13837)
 - Apollo Token Ring card
 - ESDI drive controller: Interphase V/ESDI 4201
 - SCSI drive controller (X-ADD-TFC)
 - 80286 on ETH802.3_VME
- ◇ Up to six networking cards are supported, two of each type

Storage

- ◇ Up to four disk drives in the system, options:
 - 360 MB disk drives: Micropolis 1558 and Maxtor XT-4380E

- 760 MB disk drives: Maxtor XT-8760E
- 1/4" tape drives: Archive 5945C
- ◇ Up to two disks on each ESDI controller
- ◇ SCSI drives apparently possible in Domain OS SR10.4 with WD7000-ASC

3.29.2 External ports

- ◇ I/O depends on installed configuration
- ◇ 3 RS-232 serial

3.29.3 Operating systems

The only operating system for Apollo DN10000 is Domain/OS, Apollo's own operating system from the 1980s, originally called AEGIS. DN10000s were only supported by Domain/OS SR10, which allowed to select an environment on top of the OS – AEGIS and Unix (BSD or System V). There were no other operating systems available.

HP Apollo Domain operating system was discontinued by HP in 1997 and obsoleted in 2000 (by January 2001), the last versions were 10.3.5.15 and 10.4.1.2.

3.29.4 Benchmarks

Table 3.103: Based on Dhrystone and MIPS archives; * - scores unsure

System	Processor	SPEC89	MIPS
HP Apollo DN10000	Apollo PRISM 18 MHz	19	22
HP Apollo DN10000	4 Apollo PRISM 18 MHz		60-100
HP Apollo DN10000-TX	Apollo PRISM2 36 MHz		44*

Comparison to SPEC benchmark data from other contemporary Unix computers:

Table 3.104: Based on Dhrystone archives

System	Processor	SPEC89	MIPS
HP 9000 715	PA-7100 100 MHz		88
Siemens PCE-5S	Intel Pentium 100MHz		79
HP 9000 730	PA-7000 66 MHz	78	69
HP 9000 F10	PA-7000 32 MHz		35
Intel	i486DX2 66 MHz	25	31
Sun SPARCstation 2	SPARC 40MHz	25	28
DECstation 5000/200	MIPS R3000 25MHz	23	22
HP 9000 425e	Motorola M68040 25MHz	10.3	18*
DECstation 3100	MIPS R2000 16MHz	11.8	15.1
HP 9000 834	NS-1 PA-RISC 30 MHz	9.5	14
Intel	i386 33MHz	4.3	8
DEC VAX 11/780	KA780 3.4MHz	1.0	0.9

3.29.5 Documentation

- ◇ *The DN 10000TX: a new high-performance PRISM processor*, COMPCON Spring '91 Digest of Papers, 1991
- ◇ APOLLO COMPUTER LAUNCHES ITS 64-BIT PRISM RISC MACHINE, Tech Monitor archive, February 29, 1988
- ◇ WHY APOLLO COMPUTER RECKONS IT HAS OUTDONE SUN IN THE RISC STAKES, Tech Monitor archive, March 14, 1988
- ◇ Series 10000 Personal Supercomputer Workstation Systems, Apollo Brochure, July 1988
- ◇ Apollo Quick-reference Configuration Guide, Hewlett-Packard Co., June 1990, 5952-2149
- ◇ Apollo/DOMAIN Computers, zepa.net, 2022 (mirrors: archive.org from 1999 and 2022)
- ◇ Apollo Frequently Asked Questions, Nickolai Zeldovich, Mar 29, 2012
- ◇ Apollo part list, Tame Inc., 1997 (from 1998):
 - DN10000 SYSTEMS:
 - 10574: PRISM CPU
 - 10576:
 - 10578: MAIN MEMORY PCB, REQ'S MEMORY DAUGHTERCARDS
 - 10580: MAIN MEMORY PCB, REQ'S MEMORY DAUGHTERCARDS
 - 10582: ISA BUS INTERFACE PCB
 - 10597-000: 8MB MEMORY DAUGHTERCARD (USED WITH 10578 OR 10580)
 - 10597-001: 16MB MEMORY DAUGHTERCARD (USED WITH 10580)
 - 10640: ISA BUS MOTHERBOARD
 - 10644: 5-SLOT
 - 11755: 300VDC MAIN POWER SUPPLY, (7.5A/1500W)
 - 18156: SWITCHING POWER SUPPLY (POWER COMPONENTS P/N C-942)
- ◇ HP- Apollo Products Configuration Guide, Hewlett Packard, December 12, 1989 [bitsavers](#)
- ◇ Apollo Continental United States Product Price List, Apollo Computer, July 1988 [bitsavers](#)
- ◇ HP unveils plan for new PRISM CPU, Hewlett Packard, Press Release October 1989 [100obit.it](#)
- ◇ HP/Apollo Domain Operating System, HP Vintage Software , Hewlett-Packard Company (2000: mirror accessed January 2024)

3.30 Early HP 9000 PA-RISC Systems

HP 9000 800 were the first PA-RISC systems released by HP in the 1980s. All 800s are server systems, although some had graphics capabilities. The technical and product landscape was diverse in the 80s with HP selling many different server and microcomputer series. RISC and Unix servers as the HP 9000 800 were new niche products at that time, but soon became hugely successful for business, scientific and industrial uses.

Early PA-RISC servers were HP's first foray into the RISC and Unix market. 800s are very different to later HP 9000 workstations and servers, based on custom design in TTL, NMOS and CMOS PA-RISC 1.0 processors. They were big and loud departmental servers – and rather expensive. As these computers were sold in the pre-Internet era, available information is sparse.

System	a.k.a.	Processor	Design	Year	Price
HP 9000 840	840S	TS-1 PA-RISC 8 MHz	CTB and CIO	1986	\$113,500
HP 9000 825	825S	NS-1 PA-RISC 25 MHz	SMB and CTB	1987	\$42,500
HP 9000 850	850S	NS-1 PA-RISC 27.5 MHz	SMB and CTB	1987	\$220,500
HP 9000 835	835S	NS-1 PA-RISC 30 MHz	SMB and CTB	1988	\$45,000
HP 9000 822		NS-2 PA-RISC 25 MHz	SIU and CTB	1989	\$20,000
HP 9000 832		NS-2 PA-RISC 30 MHz	SIU and CTB	1989	\$30,000
HP 9000 845	845S	NS-2 PA-RISC 27.5 MHz	SMB and CTB	1989	\$42,500
HP 9000 860	860S	NS-2 PA-RISC 27.5 MHz	SMB and CTB	1989	\$291,000
HP 9000 855	855S	NS-2 PA-RISC 27.5 MHz	SMB and CTB	1990	\$340,500
HP 9000 842		PCX PA-RISC 32 MHz	SPI and SMB	1990	\$85,000
HP 9000 852		PCX PA-RISC 50 MHz	SPI and SMB	1990	\$143,000
HP 9000 808		PCX PA-RISC ? MHz	SIU and CTB	1990	\$16,000
HP 9000 815		PCX PA-RISC ? MHz	SIU and CTB	1990	\$14,900
HP 9000 865	865S	PCX PA-RISC 50 MHz	SPI and SMB	1991	\$275,000
HP 9000 870	870S	1-4 PCX PA-RISC 50 MHz	SPI and SMB	1991	\$440,000

The only operating system for early HP 9000 800 servers is the HP Unix HP-UX up to version 10.10. There were a few research and development projects during the 1980s that targeted some of these systems but none were made publically available.

With later PA-RISC 1.1 computers in the early 90s, HP standardized and unified HP 9000 products and more affordable computers were offered to a wider customer base like the HP 9000 720, 730 and 750 workstations and Nova servers.

3.30.1 HP 9000 840 – First PA-RISC

The first commercial PA-RISC product was released in 1986 with the HP 9000 840 Indigo server, based on a six-board TTL implementation of 32-bit PA-RISC 1.0 in the TS-1 processors at 8 MHz. HP 9000 840 were primarily marketed and used as servers – and only few versions of it remain in existence after the early PA-RISC days.

HP 9000 840 use two main buses: Central Bus (CTB, also called MidBus), a 32-bit 8 MHz 20 MB/s bus, connects the processor to the main memory and the secondary I/O bus. Seven card slots are available in the 840 on Channel I/O (CIO), the 16-bit central device I/O bus. CIO has a data rate of 5 MB/s with a clock speed of 4 MHz and supported CIO devices include HP-IB, Hewlett-Packard Interface-Bus, used for instrumentation, measurement and networking adapters.

Up to 112 MB of RAM was supported: 7×16 MB with 2-16 MB memory modules compatible. The optional graphics adapter used one I/O and one memory slot, reducing the maximum RAM to 96 MB. Included by default into the system was a separate Floating Point Coprocessor (FPC) board. Storage and media devices were attached to HP-IB, SCSI was available only later and with newer boot ROMs. 840 could be upgraded via CPU board swap to 825, 835 or 845, retaining the case, memory and I/O boards.

Originally priced for \$113,500 in 1986, HP 9000 840 with maximum options could go up to \$240,500. HP 9000 840 achieved about 4.5 MIPS and originally shipped in 1986 with HP-UX 1.0, heavily BSD-based. They were supported until HP-UX 10.10 in 1995.

3.30.2 HP 9000 825, 835 and 850 with NS-1

Between 1987 and 1988, HP released first systems with brand-new 32-bit PA-RISC 1.0 processors in NMOS-III, the NS-1: HP 9000 825, 835 and 850.

HP 9000 825S were marketed as minicomputer, 825SRX as Superworkstation and 835 and 850S as Super-minicomputer. Product numbers changed a few times and some systems were called HP 9000 600 series for a while – a name soon discontinued.

HP 9000 825 and 835 were packaged both as graphics workstations and as headless computing servers, both to be used with HP-UX Unix operating system. HP 9000 850 server was HP's most powerful technical computer at the time.

These systems used a similar PA-RISC server architecture with three main buses, expanding the original HP 9000 840 system design: Processor (CPU and FPU) and memory connect to the 64-bit wide System Main Bus (SMB, peak 220 MB/s), to which two bus converters attach. To these, two Central System Buses (CTBs, or Midbuses) attach with a throughput of each 27 MB/s. Each of the Midbuses (CTBs) connects two Channel Adapters (CA), to which I/O devices attach via so-called CIO/CIB boards.

HP 9000 825, 835 and 850 servers were supported in HP-UX from version HP-UX 2.0 in 1987 to HP-UX 10.10 in 1995. The CHX and SRX graphics workstations models were only supported until HP-UX 9.

Pictures

- ◇ 825 computer, side view, rear and with CRT monitor, Wikipedia, Thomas Schanz 2018
- ◇ 835 computer and 825 and 835 computers , Wikipedia, Thomas Schanz 2018
- ◇ 825/835 open cards and cabinets, Wikipedia, Thomas Schanz 2018
- ◇ 825/835 SCSI board, video board, Wikipedia, Thomas Schanz 2018
- ◇ 825 system board and 835 system board, Wikipedia, Thomas Schanz 2018
- ◇ 835 CPU NS-1, Wikipedia, Thomas Schanz 2018
- ◇ 825 boards, CPU, I/O, Wikipedia, Thomas Schanz 2018

HP 9000 825

HP 9000 825 and 825S FireFox are small 1980s Unix servers or minicomputers, also sold as 825SRX Superworkstation, based on 25 MHz NS-1 processor on two boards, with 16 KB cache and 2048-entry TLB.

HP 9000 825 central CTB buses run at 8.33 MHz with seven shared I/O CIO and memory slots. Maximum RAM was 112 MB or 96 MB with graphics adapter, which could be expanded with 16 MB arrays. HP 9000 825 had a performance of about 9 MIPS.

Models

- ◇ HP 9000 825: Base model, \$42,500 in 1987
- ◇ HP 9000 825CHX: Workstation for graphics, included a 2D adapter
- ◇ HP 9000 825SRX: 24-bit 3D graphics for \$69,500

HP 9000 835

HP 9000 835 and 835S TopGun are servers with 30 MHz NS-1 processor (maybe also NS-2 processor), with 128 KB cache and 4096-entry TLB, slightly bigger and faster than the 825 servers. Central CTB buses run at 10 MHz, their maximum, with seven shared I/O CIO and memory slots. Maximum RAM was 112 MB or 96 MB with graphics adapter, which could be expanded with 16 MB arrays.

HP 9000 835 were expensive computers for the time and sold for about US \$45,000 in 1988 for a performance of about 14 MIPS. HP 9000 835 had a SPEC89 score of 9.5 (1989).

Several different models were available:

- ◇ HP 9000 835: Base model
- ◇ HP 9000 835CHX: Workstation for graphics, with 2D adapter
- ◇ HP 9000 835SRX: Workstation with 32-bit 3D adapter
- ◇ HP 9000 834: Standard 835 with a two-user limit
- ◇ HP 9000 835SE: High-end version for 64 users with integrated CIO expander, 24 MB memory sold for US \$99,000.
- ◇ HP 9000 635SV: Server version without graphics

Server versions without graphics were shortly sold as 9000 635SV.

A port of early PA-RISC HPBSD ran on HP 9000 834 and 835 servers in the 1980s, as did the Mach 3.0 port from the University of Utah. Chorus was ported also in 1990-1991 as a research project to the HP 9000 834.

HP 9000 850

HP 9000 850 are big cabinet servers released by HP in 1987, marketed as “on top of the most advanced computing”. Sporting a 27.5 MHz NS-1 processor with 128 KB cache and 4096-entry TLB, the 850 server was the fastest PA-RISC computer at release and billed as *mimicomputer* for general purpose, engineering, scientific and industrial uses.

Based on SMB and CTB architecture, 850 had CTBs at 9.16 MHz with CIO for I/O devices and additionally two Memory Array Buses MAB, capable of linking up eight 16 MB memory modules arrays via a 72-bit data path to the SMB. Maximum RAM was 128 MB with one memory controller and 256 MB with two memory controllers.

Sold for a price of US \$220,500 in 1987 with a performance of about 14 MIPS, HP 9000 850 were HP’s most powerful technical computer in the late 80s.

3.30.3 HP 9000 845, 855 and 860 with NS-2

In 1989 HP 9000 computers based on the NS-2 processor, a revamped NS-1, appeared. These systems are all based on the same I/O architecture and facilitate the same CPU design—the PA-RISC 1.0 NS-2 processor with a SMB and CTB system design and CIO devices, similar to earlier systems like the 825 and 850 servers. These PA-RISC 1.0 servers include the following:⁵

HP 9000 845

HP 9000 845 ShoGun from 1989 have 27.5 MHz NS-2 processor with 256 KB cache and a 16384-entry TLB, based on a SMB/CTB system design.

CTB main buses run at 9.16 MHz for seven CIO and memory slots, I/O is handled by CIO expansion cards. Maximum RAM of 112 MB: 7×16 MB, 96 MB: 6×16 MB with graphics adapter. Performance was about 22 MIPS.

Special version

- ◇ HP 9000 645SV: Server versions without graphics

HP 9000 855

HP 9000 855 or 855S Jaguar are bigger servers than the 845, with a 27.5 MHz NS-2 processor with 256 KB cache and 16384-entry TLB.

System design is SMB/CTB, with the CTB buses at 9.16 MHz, maximum RAM of 128 MB or 256 MB with two memory controllers. Performance is about 22 MIPS for a serious price of US \$340,500 in 1990.

HP 9000 860

HP 9000 860 Cougar servers are cabinet, mainframe-like systems, based on 27.5 MHz NS-2 processor with 1024 KB cache and 16384-entry TLB.

CTB I/O buses run at 9.16 MHz, maximum RAM is 128 MB with one memory controller and 256 MB with two memory controllers. HP 9000 860 was released in 1989 for a price of \$291,000 and could be upgraded with newer CPU boards to a HP 9000 865 or 870 server.

3.30.4 HP 9000 822, 832, 808, 815 with NS-2 and PCX

HP released several compact PA-RISC servers between 1989 and 1990 for the lower-end Unix business server market. Two separate low-cost systems design were offered—HP 9000 822 and 832 servers with the NMOS NS-2 processor and HP 9000 808 and 815 servers based on the new CMOS PCX processor. For devices and I/O, the HP-PB bus was used.⁷

HP 9000 822 and 832

HP 9000 822 and 832 are PA-RISC servers released in 1989, based on single-chip VLSI processors for the first time, in HP NMOS manufacturing process. HP 9000 822 SilverFox Low are entry-level

PA-RISC business servers for Unix with 25 MHz NS-2 processor with 32 KB cache and a 4096-entry TLB.

HP 9000 832 SilverFox High are very similar to 822 but higher performance with faster 30 MHz NS-2 processor with 128 KB cache and 4096-entry TLB. System design is SIU/SMB for HP-PB cards used for expansion and I/O, maximum RAM is 64 MB.

Performance of HP 9000 822 is about 10 MIPS for a price of around \$20,000 in 1989, marketed for highly-reliable computational and data processing needs in a “normal office environment” on the floor without special AC or spacing requirements. Performance of 832 was slightly higher with 12 or 15 MIPS for a price of about US \$30,000 in 1989.

There was an CPU board upgrade path from 822 to 832 and to 842 and 852. Apparently I/O slots could also be upgraded from 6 to 12, but it is not totally clear how.

HP 9000 822 and 832 servers were supported in HP-UX possibly from version HP-UX 7.0 in 1989 to HP-UX 10.10 in 1995.

HP 9000 808 and 815

HP 9000 808 and 815 are low-cost PA-RISC servers released in 1990, apparently using PCX PA-RISC 1.0 processors in CMOS. They use a similar system design (SPI and SMB) which leaned on their predecessors and were an attempt by HP to capture the lower-cost late-1980s server market with more simpler and limited offerings.

Maximum RAM for 808 was 32 MB, for 815 slightly higher 56 MB, with expansion cards seemingly using HP-PB. HP 9000 808 had a performance of 7 MIPS (which seems rather low for the PCX) was sold for around \$16,000, the 815 with the same performance of 7 MIPS in 1990 for around \$14,900.

Both 808 and 815 were not distributed on a larger scale it seems— not many machines and even less documentation survived. There are a few inconsistencies in the available mentions of the 808 and 815. HP apparently offered a CPU board upgrade path from 815 to 825, and then to 835 and 845, although it is unclear if that makes sense, as the latter are based on older CPUs.

HP 9000 808 and 815 servers were supported in HP-UX possibly from version HP-UX 7.0 or 8.0 in 1989 to HP-UX 9 in 1992.

3.30.5 HP 9000 842, 852, 865 and 870 with PCX

HP 9000 842, 852, 865 and multi-processor 870 use the first PA-RISC processors implemented in CMOS—the PA-RISC 1.0 PCX. Released in 1990 and 1991, these servers are very similar to earlier NMOS NS-2 based servers with the same system and I/O architecture and slightly modified CPU/SPU design.⁶ These system use the same 16 MB memory arrays as earlier servers but could also use 64 MB boards.

HP 9000 842, 852, 865 and 870 servers were supported in HP-UX possibly from version HP-UX 8 in 1991 to HP-UX 10.10 in 1995.

HP 9000 842 and 852

HP 9000 842 SilverBullet Low used 32 MHz PCX processors with large 1024 KB cache, 8192-entry TLB and 256 MB maximum RAM. HP 9000 852 SilverBullet High were almost the same design, but

with a faster 50 MHz PCX processor.

Both machines use SPI/SMB system design and HP-PB expansion cards for I/O and devices. Performance of 842 was about 30 MIPS for a price of about \$85,000 at time of introduction in 1990, with the 852 having 50 MIPS for around \$143,000.

HP 9000 865

HP 9000 865 Panther servers are cabinet computers, with a larger design than the previous 800 series, based on the new CMOS-based 50 MHz PCX PA-RISC processor with 768 KB cache and a 8192-entry TLB. SPI/SMB system design and CIO bus was used for I/O, maximum RAM was 512 MB. HP 9000 865 sold for about \$275,000 in 1991 and was supposed to have a performance of 56 MIPS.

HP 9000 870

HP 9000 870 Panther servers are large cabinet computers and the first SMP multiprocessor PA-RISC systems, with up to four 50 MHz PCX processors with 1024 KB cache and a 8192-entry TLB each. HP 9000 870/100 was uni-CPU, 870/200 dual, 870/300 triple and 870/400 quad-CPU with 1 MB cache per CPU.

SPI/SMB system design and CIO bus is used for I/O, and maximum RAM was 1024 MB with two memory controllers in 16 slots. Performance was supposedly 50 or 56 MIPS for single-CPU, 90 or 112 MIPS for dual-CPU, up to 168 MIPS for triple-CPU and up to 224 MIPS for quad-CPU. Introduction prices were about \$440,000 for 870/300, \$530,000 for 870/400.

Later HP 9000 890 mainframes with up to four CPUs are possibly similar to the 870 and was an upgrade and technology enhancement path.

3.30.6 Operating systems

HP 9000 800 servers, especially the early versions from the 1980s, only really support HP-UX Unix, developed by HP, due to their custom and proprietary hardware.

Table 3.106: HP-UX support for early HP 9000 800 servers

HP-UX	Year	Servers	Comment
HP-UX 10.10	1995	HP 9000 840, 825, 835, 850 845, 855, 860, 822, 832 842, 852, 865 and 870 HP 9000 Nova, E-Class	UNIX95, CDE, Service-Guard
HP-UX 10.01	1995	HP 9000 840, 825, 835, 850 845, 855, 860, 822, 832 842, 852, 865 and 870 HP 9000 Nova, E-Class	System V, DCE, Streams, better I/O and memory unsupported: 635, 645, 808, 815 unsupported: 825CHX, 825SRX, 834CH, 835SRX
HP-UX 9.0	1992	HP 9000 840, 825, 835, 850 845, 855, 860, 822, 832, 808, 815 842, 852, 865 and 870 HP 9000 Nova, E-Class	PA-7100 and PA-7100LC support, LVM, VUE 9.02, 9.04 and 9.06 added hardware support 9.08 was B1 security release

HP-UX 8.0	1991	HP 9000 840, 825, 835, 850 845, 855, 860, 822, 832, 808, 815 842, 852, 865 and 870 HP 9000 Nova	8.02 added Nova support 8.04 and 8.08 were security versions 8.06 added SMP code
HP-UX 7.0	1989	some PA-RISC 1.0	PA-RISC only in 7.03, rest M68k
HP-UX 3.0	1988	HP 9000 825, 835, 850 +?	3.01 had "nasty bugs", X11
HP-UX 2.0	1987	HP 9000 840, 825, 835, 850	BSD, supports graphics
HP-UX 1.0	1986	HP 9000 840	First, prerelease

3.30.7 Benchmarks

Assorted MIPS performance figures for early HP 9000 800 servers.

Table 3.107: Based on HP, Dhrystone and MIPS archives

System	CPU	MIPS
HP 9000 840	TS-1 PA-RISC 8 MHz	4.5
HP 9000 808	PCX PA-RISC 12.5 MHz	6
HP 9000 815	PCX PA-RISC 12.5 MHz	6
HP 9000 825	NS-1 PA-RISC 25 MHz	9
HP 9000 822	NS-2 PA-RISC 25 MHz	10
HP 9000 850	NS-1 PA-RISC 27.5 MHz	14
HP 9000 835	NS-1 PA-RISC 30 MHz	149.5 SPEC89
HP 9000 832	NS-2 PA-RISC 30 MHz	12/15
HP 9000 845	NS-2 PA-RISC 27.5 MHz	22
HP 9000 855	NS-2 PA-RISC 27.5 MHz	22
HP 9000 842	PCX PA-RISC 32 MHz	30
HP 9000 852	PCX PA-RISC 50 MHz	50
HP 9000 865	PCX PA-RISC 50 MHz	56
HP 9000 870/100	PCX PA-RISC 50 MHz	56
HP 9000 870/200	2 PCX PA-RISC 50 MHz	112
HP 9000 870/300	3 PCX PA-RISC 50 MHz	168
HP 9000 870/400	4 PCX PA-RISC 50 MHz	224

Comparison to SPEC benchmark data of later HP 9000 800 servers:

Table 3.108: Based on old SPEC92, Dhrystone and MIPS archives

System	CPU	SPEC92 int	SPEC89	MIPS
HP 9000 G50	PA-7000 96 MHz	100.0	136.1	115
Siemens PCE-5S	Intel Pentium 100MHz	96.2		79
HP 9000 I40	PA-7000 64 MHz	65.2		70
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	71.2	58
HP 9000 712/80	PA-7100LC 80 MHz	97.1		97
HP 9000 750	PA-7000 66 MHz	48.1	77.5	69
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	25.6	37

HP 9000 F10	PA-7000 32 MHz	22.0		35
DECstation 5000	MIPS R3000 33MHz	20.9	25.5	29
HP Apollo DN10000	Apollo PRISM 18 MHz		19	22
DECstation 3100	MIPS R2000 16MHz	8.4*	11.8	15.1
HP 9000 425e	Motorola M68040 25MHz	12.2	10.3	18
Intel	i386 33MHz		4.3	8
IBM PC 6150	IBM ROMP 6MHz			2.1
HP 9000 320	Motorola M68020 15MHz			2
HP 9000 500	FOCUS 18 MHz			0.98
DEC VAX 11/780	KA780 3.4MHz	1	1	0.9
IBM PC AT	Intel 80286 6MHz			0.8

3.30.8 Documentation

Information on these early PA-RISC computers is fragmented and inconsistent, even in official sales and technical documentation, with sometimes divergent accounts of hardware, architecture and PA-RISC processors. Much of the information here was pieced together from old news articles and press releases, plus documentation available at the HP Computer Museum.

1. INFORMATION ON HP9000 SERVERS AND WORKSTATIONS Hewlett Packard Company (1999. Accessed January 2007) and *The HP 3000/HP 9000 model spreadsheet*, Allegro Consultants (2004. Accessed January 2007)
2. Wayne E. Holt (ed.), *Beyond RISC! An Essential Guide to Hewlett-Packard Precision Architecture*, p. 95-102. (January 1988: Software Research Northwest Inc.) and Hardware Design of the First HP Precision Architecture Computers (PDF) David A. Fotland et al (March 1987: Hewlett-Packard Journal) **hp museum**
3. HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook (PDF) Hewlett-Packard Company (October 1990. Accessed January 2008) **hp museum** and HP 9000 Series 800 Model 825S Hardware Technical Data (PDF) Hewlett-Packard Company (September 1988. Accessed January 2008) **hp museum** and HP 3000/925 and HP 9000/825/835 Computer Systems CE Handbook (PDF) Hewlett-Packard Company (May 1988. Accessed January 2008) **hp museum** and *New midrange members of the Hewlett-Packard Precision Architecture Computer Family* Thomas O. Meyer et al (June 1989: Hewlett Packard Journal. Accessed January 2008 at findarticles.com)
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8. For HP 9000/840: Interview with David Fotland, September/October 2008
9. HP REDUCES HP 9000 MINICOMPUTER PRICES (PDF) Hewlett-Packard Press Release, October 1989, accessed January 2023 **100bit.it**
10. A Broader Vision of Performance For Your Business - HP 9000 Multiuser Systems (PDF) Hewlett-Packard, 1990, 5952-0835, accessed January 2023 **100bit.it**

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12. HP-UX CE Handbook for Series 800 HP Precision Architecture-RISC Computer Systems Hewlett-Packard Company (May 1993, 5961-8364) [bitsavers](#)
13. HP 3000/930 and HP 9000/840 Computers CE Handbook Hewlett-Packard Company (November 1986, 09740-90023) [bitsavers](#)

Pictures Hewlett Packard, scans from product brochures, from [hpmuseum.net](#) and [100obit.it](#)

3.3.1 HP 9000 Series 800 Nova Servers

HP 9000 “Nova” F, G, H and I Class are HP 9000 800 PA-RISC servers from the early 1990s. They were based on 32-bit PA-7000 and PA-7100 processors and succeeded the 1980s early HP 9000 800 servers based on PA-RISC 1.0.

Nova servers were designed by the HP Technical Server division with distinct architecture to PA-RISC workstations, sharing few devices and I/O systems. Chipset was similar with HP ASP and Viper, but I/O was on special HP-PB.

Billed as HP 9000 Midrange Business Servers, Nova servers were targeted for business applications and transactions in a “compact” desktide and rack-mountable case. They offered lots of expansion and were often used for I/O and storage-heavy workloads. Entry Nova servers were often shipped without FPU, as floating-point performance was often not required.

- ◇ HP 9000 F10, HP 9000/807, were introduced in 1991 for \$12,895
- ◇ HP 9000 F20 and H20, HP 9000/807 and 827, were introduced in 1991 for \$20,000
- ◇ HP 9000 F30, G30/H30 and I30, HP 9000/807, were introduced in 1991
- ◇ HP 9000 G40/H40 and I40, HP 9000/867 and 877, were introduced in 1991 for \$112,500-\$140,000
- ◇ HP 9000 G50/H50 and I50, HP 9000/887 and 897, were introduced in 1992
- ◇ HP 9000 G60/H60 and I60, HP 9000/887 and 897, were introduced in 1993
- ◇ HP 9000 G70/H70 and I70, HP 9000/887 and 897, were introduced in 1993

Nova servers were succeeded by E Class servers with PA-7100LC that shared F Class cases and some of the proprietary I/O design. Many Nova servers became available second-hand in the 2000s at bargain prices, since few follow-on use cases were possible for the cumbersome machines with limited software options but HP-UX.

Some Nova servers could be upgraded to other configurations “through a range of easy processor board and slot upgrades,” as they had up “to 10.3 x performance headroom in the same chassis.” There were “performance upgrades on the vertical axis” and “I/O slot upgrades on the horizontal axis.”

3.3.1.1 System architecture

Processors

System	CPU	FPU	Speed	L1 Cache
HP 9000 F10	PA-7000 PA-RISC 32-bit	optional	32 MHz	32/64 KB off-chip
HP 9000 F20, H20	PA-7000 PA-RISC 32-bit	optional	48 MHz	64/64 KB off-chip
HP 9000 F30, G30, H30, I30	PA-7000 PA-RISC 32-bit	optional	48 MHz	256/256 KB off-chip
HP 9000 G40, H40, I40	PA-7000 PA-RISC 32-bit	optional	64 MHz	256/256 KB off-chip
HP 9000 G50, H50, I50	PA-7100 PA-RISC 32-bit	integrated	96 MHz	256/256 KB off-chip
HP 9000 G60, H60, I60	PA-7100 PA-RISC 32-bit	integrated	96 MHz	1024/1024 KB off-chip
HP 9000 G70, H70, I70	1-2 PA-7100 PA-RISC 32-bit	integrated	96 MHz	2048/2048 KB off-chip

[F, G, H, I] letters indicate I/O expansion options and case, [10, 20, ... 70] denote used processors and chipsets. G, H and I class shared the same case.

Picture of H20 (827) CPU Board (PA-7000) Thomas Schanz 2008

Chipset

The chipset is a variant of HP ASP with HP Viper memory controller, interfacing the processor to memory and HP-PB I/O bus. System I/O is implemented on so-called HP-PB Personality Boards with separate I/O devices and chips.

System buses

- ◇ PBus processor/memory bus
- ◇ VSC main system bus
- ◇ HP-PB bus for the general I/O
- ◇ SCSI-2 Narrow single-ended bus for main storage I/O

Memory

- ◇ HP proprietary modules like on 720, 730 and 750, and 735/755
- ◇ F10: 16 MB minimum, 128 MB (8×16 MB) maximum
- ◇ F20 and F30: 16 MB minimum, 192 MB (12×16 MB) maximum
- ◇ H20, H30, G30, I30, x40: 16 MB minimum, 384 MB (12×32 MB) maximum
- ◇ x50, x60, x70: 16 MB minimum, 768 MB (12×64 MB) maximum

Expansion slots

- ◇ Fx0: two HP-PB single-height/one double-height slots
- ◇ Gx0: six HP-PB single-height/three double-height slots
- ◇ Hx0: six HP-PB single-height/three double-height slots
- ◇ Ix0: twelve HP-PB single-height/six double-height slots

Storage

- ◇ Many, depending on the case

3.31.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ High-pin-count MUX connector
- ◇ Parallel DB25
- ◇ Rest depends on installed HP-PB cards

3.3.1.3 Operating systems

The only operating system for these servers was HP-UX, with all of them supported in HP-UX 10.20 for 800s servers and 11.00. First supported release was HP-UX 8.02, official support was dropped in 11.11 (11i vi).

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9 (9.00, 9.02, 9.04, 9.06), pre-Y2K
 - HP-UX 8 (8.02, 8.06), pre-Y2K

3.3.1.4 Benchmarks

Table 3.110: Based on old SPEC92, Dhrystone and MIPS archives

System	CPU	SPEC92 int	SPEC92 fp	MIPS
HP 9000 F10	PA-7000 32 MHz	22.0	36.6	35
HP 9000 F20, H20	PA-7000 48 MHz	33.6	56.1	53
HP 9000 F30, G30/H30, I30	PA-7000 48 MHz	37.8	62.4	53
HP 9000 G40/H40, I40	PA-7000 64 MHz	65.2	91.3	70
HP 9000 G50/H50, I50	PA-7000 96 MHz	100.0	158.5	115
HP 9000 G60/H60, I60	PA-7000 96 MHz	108.8	195.3	115
HP 9000 G70/H70, I70	PA-7000 96 MHz	108.8	195.3	115

Comparison to SPEC benchmark data from other contemporary Unix computers:

Table 3.111: Based on old SPEC92 archives

System	CPU	SPEC92 int	SPEC92 fp
HP 9000 755/125	PA-7150 125 MHz	136.0	201.0
IBM RS/6000 43P	PowerPC 604 100 MHz	128.0	120.2
Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2
HP 9000 E55	PA-7100LC 96 MHz	108.0	163.4
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2
SGI Indigo2	MIPS R4400 150MHz	85.9	93.6
HP 9000 E45	PA-7100LC 80 MHz	82.1	122.9
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2
HP 9000 712/60	PA-7100LC 60 MHz	67.0	85.3
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2
HP 9000 E25	PA-7100LC 48 MHz	45.0	66.7
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1
IBM RS/6000 355	IBM POWER 41MHz	40.7	83.3
Siemens PCE-4C	Intel 486DX2 66MHz	35.8	16.1
Motorola 8000	Motorola 88100 33MHz	27.7	18.8
HP 9000 425e	Motorola 68040 25MHz	12.2	9.3

Digital VAX4000	DEC KA46 22MHz	11.1	12.6
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3.31.5 Documentation

Manuals

- ◇ Owner's Guide to the HP 9000 8x7S Family (.pdf) Hewlett-Packard Company (1991, 5960-31110, Accessed January 2009) **hpmuseum**
- ◇ Owner's Guide to the HP 9000 8x7S Family (.pdf) Hewlett-Packard Company (1992, 5959-5273) **hpmuseum**
- ◇ CE Handbook Series 9x7 and Model 8x7S Family (.pdf) Hewlett-Packard Company (February 1992, A1707-90016, Accessed January 2009) **hpmuseum**
- ◇ HP-UX CE Handbook for Series 800 HP Precision Architecture-RISC Computer Systems Hewlett-Packard Company (May 1993, 5961-8364) **bitsavers**

Product sheets

- ◇ HP 9000 Series 800 Business Servers Models 807S/817S/827S/837S/847S/857S, product brief, Hewlett-Packard Company (Juni 1991, 5091-1631E) **hpmuseum**
- ◇ HP 9000 Midrange Business Brief HP 9000 G, H and I Class Servers, (.pdf) Hewlett-Packard Company (February 1994, 5962-8608E, Accessed January 2009 at hpmuseum.net)
- ◇ HP 9000/800 X Class Computer System Installation and Configuration Guide, Hewlett-Packard (1993, A1703-90041, E0893) **hpmuseum**

Other

- ◇ Pinout for the mini-DIN console connector at the back

3.32 HP i2000 Itanium workstation

HP i2000 was HP's first Itanium workstation with first generation *Merced* Itanium processor, released in 2001 as proof-of-concept to deliver first Itanium based on an early Intel 82460GX reference design (rebranded and sold by other vendors). Itanium had been long in development as joint HP-Intel project that promised a better CPU future with VLIW/EPIC architecture on HP-UX, Windows and Linux.

The HP i2000 workstation was the first Itanium computer to actually leave the gates of HP, released in parallel to almost the last PA-RISC workstations, C3650 and C3750, followed a few years later by c8000 and Itanium zx2000.

As HP put it in 2001, "when HP invited Intel into our lab, we showed them the architecture that will become the pervasive 64-bit architecture of the 21st century. They shared our vision and together we invented the Itanium processor family specification." The i2000 was the first, unhappy materialization of that vision.

- ◇ HP i2000 were introduced in 2001 for \$7,995-14,495

HP i2000 had an interesting set of possible operating systems: HP-UX Unix, Linux, OpenVMS on Itanium, Windows XP and 2000. OpenVMS was actually ported on i2000, with first boot in 2003.

3.32.1 System architecture

Processors

Table 3.112: Itanium CPUs have complex cache arrangements

System	CPU	Speed	L1 and L2 cache	L3 cache
HP i2000	Itanium <i>Merced</i> VLIW 64-bit	733 MHz	16/16 KB and 96 KB on-die	2.0-4.0 MB off-chip
HP i2000	I-2 Itanium <i>Merced</i> VLIW 64-bit	800 MHz	16/16 KB and 96 KB on-die	2.0-4.0 MB off-chip

Chipset

The i2000 had certain limitations due to chipset and/or operating system bugs and supported only first generation Itanium CPUs. It was rather slow for the time when contemporary PA-RISC workstations in most cases were significantly faster.

- ◇ Intel 82460GX chipset
- ◇ Two WXBs (Wide eXpansion Bridges) for each one PCI 64/66 bus
- ◇ PXB (PCI eXpansion Bridge) for one PCI 64/33 bus
- ◇ I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- ◇ Qlogic 12160 dual-channel Ultra3 SCSI controller (separate PCI card)
- ◇ Intel 82559 Fast Ethernet controller
- ◇ nVIDIA Quadro2 Pro video card (separate AGP card)
- ◇ ATA-33 IDE controller (on IFB)
- ◇ USB controller (on IFB)
- ◇ LPC47B27 Super I/O (serial and PS/2 ports controller)

System buses

- ◇ Memory bus, 266 MHz, 4.2 GB/s peak
- ◇ Two PCI 64/66 I/O buses (for expansion slots)
- ◇ PCI 64/33 I/O bus (for expansion slots)
- ◇ PCI 32/33 I/O bus (for onboard devices)

Memory

- ◇ PC100 registered SDRAM DIMMs
- ◇ Up to two memory expansion cards (MECs)
- ◇ Eight slots on each MEC
- ◇ Up to 1 GB modules
- ◇ 16 GB maximum (16×1 GB—8 GB on each MEC)

Expansion slots

- ◇ Five PCI 64-bit/66 MHz slots, 3.3 V
- ◇ Two PCI 64-bit/33 MHz slots, 5 V
- ◇ One AGP Pro 110 slot (supports AGP-1x, 3x, 4x, or AGPpro-110)

Storage

- ◇ Three (1.6") or five (1") internal 3.5" bays for hard drives
- ◇ Three half-height 5.25" bays for externally accessible drives
- ◇ One 3.5" bay for externally accessible drive (shipped with LS-120)

3.32.2 External ports

- ◇ 10/100 Ethernet TP/RJ45
- ◇ Four USB ports (two on front, two on rear)
- ◇ Serial RS232C DB9
- ◇ Two PS/2 for keyboard and mouse
- ◇ Three phone jacks (microphone, line-in and line-out)

3.32.3 Operating systems

- ◇ HP-UX Itanium VI.5 and VI.6 for Itanium. HP-UX had some binary compatibility for PA-RISC applications in its Itanium versions, however mostly emulated.
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ OpenVMS (supposedly)
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ Windows XP Professional 64-bit Edition
- ◇ Windows 2000 Server IA64 Edition (Beta Release)
- ◇ Windows Server 2003 Itanium-based Editions

OpenVMS for Integrity (Itanium) was apparently developed on HP i2000, “official time of the first boot of OpenVMS on Integrity was January 31, 2003 at 3:31 PM EST on an HP i2000 (Itanium1) system.”

3.32.4 Benchmarks

Some SPEC numbers for PA-RISC workstations as comparison.

Table 3.113: * SPEC scores were apparently higher on Windows XP

System	Processor	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
i2000	Itanium Merced 733 MHz 2 MB		623 (on XP)*		7.22
i2000	Itanium Merced 733 MHz 4 MB		577		
i2000	Itanium Merced 800 MHz 2 MB		655 (on XP)* 2P 658		7.6 2P 13.2
i2000	Itanium Merced 800 MHz 4 MB	365	610		

HP i2000 with first generation Itanium (Merced) CPU were beaten by most contemporary 2000s workstations in benchmarks other than floating point. HP claimed in 2001 that the “i2000 will outperform most, if not all, current architectures in floating point performance in the SPECfp benchmark”, which was true.

HP claimed the real-world relevant “Integer performance in applications such as encryption/decryption operations for secure web serving is **excellent**,” however Itanium was even beaten by the inhouse PA-RISC competition it was meant to replace.

Table 3.114: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP zx6000	McKinley 1.0 GHz	807	1422
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
HP Visualize C3750	PA-RISC PA-8700+ 875 MHz 2.2MB	678	674
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688

DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP Visualize P750C	Pentium III 750MHz	325	219
Compaq AlphaServer ES40	Alpha 21264 500MHz	311	382
HP Visualize C3000	PA-8500 400MHz	313	321
HP Visualize P500	Intel Pentium III 500MHz	231	191

3.32.5 Dimensions

Height	Width	Depth	Weight
457mm	254mm	645mm	38kg

3.32.6 Documentation

- ◇ HP Workstation i2000 Owner's Guide (URL gone)
- ◇ hp workstation i2000 summary, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ hp workstation i2000 data sheet (PDF) , Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ OpenVMS Technical Journal V6, Porting OpenVMS to HP Integrity Servers, (PDF) , Hewlett-Packard Company (June 2005)
- ◇ IBM AIX for IA64 (Itanium) aka Project Monterey runs again!, Virtually Fun blog, September 2022

3.33 HP Visualize J200, J210, J280, J2240

HP Visualize J-Class are large PA-RISC workstations from the mid-1990s, up to two-way SMP in deskside chassis. Introduced in 1995, the J200 and J210 were the first PA-RISC workstations not using the *Series 700* naming convention anymore. Together with the contemporary C-Class, the J-Class superseded earlier HP 9000 700 workstations like the 715 and 735.

J-Class later included a variety of 32- and 64-bit processors: J200 and J210 were 32-bit, the J280, J282 and J2240 were 64-bit. J280 was single-processor and could be upgraded to dual J282 – all others were two-way SMP-capable out of the box.

HP marketed J-Class against contemporary Unix and RISC offerings, specifically the Sun Ultra 2 U2 2200 and focused use cases of advanced 3D, computational analysis and “compute- and memory-intensive processing workloads.” J-Class workstations had solid expandability with multiprocessing and many I/O options, often used for Visualize graphics.

- ◇ HP 9000 J200, HP 9000/770, were introduced in 1995 for \$27,655
- ◇ HP 9000 J210, HP 9000/770, were introduced in 1995 for \$35,655
- ◇ HP 9000 J210XC, HP 9000/770, were introduced in 1995
- ◇ HP Visualize J280, HP 9000/780, were introduced in 1996 for \$38,520
- ◇ HP Visualize J282, HP 9000/780, were introduced in 1997
- ◇ HP Visualize J2240, HP 9000/782, were introduced in 1997 for \$55,900

J-Class were used in the military a lot during the 1990s, together with a variety of other PA-RISC computers like D-Class they were part of the US Navy TAC-4 program. HP was a TAC-4 vendor supplying RISC Unix computers for uses throughout the Navy and offered the J-Class as part of a technology refreshment of TAC-4 in 1996.

There were 64-bit successor J-Class around 2000: the J5000/J7000 and J6000, which then became some of the last PA-RISC workstations offered before HP fully switched to Itanium and soon ceased to offer RISC/Unix workstations altogether.

3.33.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 J200	1-2 PA-7200 PA-RISC 32-bit	100 MHz	256/256 KB off-chip, 2 KB on-chip “assist”
HP 9000 J210	1-2 PA-7200 PA-RISC 32-bit	120 MHz	256/256 KB off-chip, 2 KB on-chip “assist”
HP 9000 J210XC	1-2 PA-7200 PA-RISC 32-bit	120 MHz	1/1 MB off-chip, 2 KB on-chip “assist”
HP Visualize J280	1 PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
HP Visualize J282	1-2 PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
HP Visualize J2240	1-2 PA-8200 PA-RISC 64-bit	236 MHz	2/2 MB off-chip

Chipset

- ◇ J2x0 HP U2 chipset Runway to GSC bridge
- ◇ J28x HP UTurn chipset Runway to GSC bridge

- ◇ HP MMC/SMC memory controllers
- ◇ HP LASI I/O chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Wax EISA bridge
- ◇ NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ Other I/O (serial, parallel, Floppy, HP-HIL)
- ◇ Graphics could be extended through separate boards:
 - *Optional* HP HCRX GSC video adapters
 - *Optional* HP Visualize GSC video adapters
- ◇ J2240 HP Dino GSC-to-PCI bridge
- ◇ J2240 HP Cujo GSC-to-PCI bridge, 64-bit
- ◇ J2240 Symbios Logic 53C895 16-bit Ultra-Wide SCSI-2 controller
- ◇ J2240 DEC 21142/43 *Tulip* Fast-Ethernet controller

System buses

- ◇ Runway CPU/memory bus (100 MHz with 800 MB/s peak data rate on J200, 120 MHz 960 MB/s on all others)
- ◇ Cache:
 - J200 64-bit wide, 800 MB/s I/D fetch and load
 - J210 64-bit wide, 960 MB/s I/D fetch and load
 - J28x 128-bit wide, 2.88 GB/s fetch, 1.44 GB/s D-store
- ◇ GSC system level I/O bus
- ◇ EISA additional expansion I/O bus
- ◇ SCSI-2 Fast-Wide high-voltage differential bus, main storage I/O
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ J2240 SCSI-3 Ultra-Wide single-ended bus, main storage I/O
- ◇ J2240 PCI bus

Memory

- ◇ 72-pin ECC SIMMs, 60ns or faster
- ◇ Bus width: 128 data bits with 16 check bits
- ◇ Up to 8-way interleaving

- ◇ 16 slots for 16-128 MB modules
- ◇ 32 MB to 2 GB supported
- ◇ J2240 4 GB maximum (with 256 MB modules)

Expansion slots

- ◇ One slot for a GSC (EISA formfactor) card
- ◇ Two slots for EISA cards
- ◇ Two slots for GSC (EISA formfactor) or EISA cards
- ◇ Slot layout, from bottom to top:
 1. GSC (for primary graphics)
 2. EISA or GSC
 3. EISA or GSC
 4. EISA
 5. EISA

J2240 Expansion slots

- ◇ One slot for a PCI 32-bit/33 MHz, 5 V card
- ◇ One slot for a PCI 32-bit/33 MHz, 5 V or EISA card
- ◇ One slot for a GSC or PCI 32-bit 32-bit/33 MHz, 5 V card
- ◇ Two slots for GSC or PCI 64-bit/66 MHz, 3.3 V cards
- ◇ Slot layout, from bottom to top:
 1. PCI-64/66, 3.3 V or GSC (for primary graphics)
 2. PCI-32/33, 5 V or GSC
 3. PCI-64/66, 3.3 V or GSC
 4. PCI-32/33, 5 V
 5. PCI-32/33, 5 V or EISA

Storage

- ◇ One tray for two 3.5" Fast-Wide HVD 68-pin SCSI hard drives
- ◇ One tray for two half-height 5.25" Fast-Narrow SE 50-pin SCSI drives, external accessible

3.33.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ SCSI-3 68-pin Fast-Wide high-voltage differential (HVD)
- ◇ *J2240* SCSI-3 68-pin Ultra-Wide single-ended
- ◇ Two serial RS232C DB9 (up to 460.8Kb/s)
- ◇ Parallel DB25
- ◇ Ethernet RJ45 and AUI
- ◇ *J2240* Fast Ethernet RJ45
- ◇ Graphics port depends on installed framebuffer
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ HP-HIL for input device loop
- ◇ Four phone jacks (microphone, headphones, line-in and ?)

3.33.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit (*J2x0*) or 64-bit (*J28x*), TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit (*J2x0*) or 64-bit (*J28x*)
 - HP-UX 10.20 32-bit (ACE 9804 for *J2240*)
 - *J200, J210*HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - *J200, J210*HP-UX 9.07 (possibly), pre-Y2K
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC
- ◇ *J200, J210*HPBSD research Unix operating system (closed)
- ◇ *J200, J210*OSF MK-PA commercial Unix alternative (rare)

J200

3.33.4 Dimensions

Height	Width	Depth	Weight
470mm	330mm	541mm	50kg

3.33.5 Benchmarks

Table 3.118: Results with HP-UX 10.20

System	SPEC95 int	SPEC95 fp	SPECrate95, int	SPECrate95, fp
HP 9000 J200 2-CPU	4.98	4.50	44.8 64.5	61.3 105
HP 9000 J210 2-CPU	6.00	5.40	54.0 77.5	73.4 126
HP 9000 J210XC 2-CPU	6.40	5.70	57.6 82.8	81.5 142
HP Visualize J280 2-CPU	11.80	19.30	107	174
HP Visualize J282 2-CPU	11.90	19.30	107.2	174
HP Visualize J2240 2-CPU	17.40	26.30	157 307	237 349

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.119: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
HP Visualize C240	PA-8200 236 MHz	17.1	25.4
DEC Alphastation 500	DEC Alpha 21164 500MHz	15.0	20.4
SGI Origin 2000	MIPS R10000 250MHz 4MB	14.7	24.5
Sun Ultra 5 333	Sun UltraSPARC Ili 333MHz	14.1	18.3
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.78
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
HP Visualize C160L	PA-7300LC 160 MHz	7.75	7.56
IBM RS/6000 F50	PowerPC 604e 166 MHz	7.52	8.52
DEC Alphastation 600	DEC Alpha 21164 300MHz	7.33	12.2
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 250	DEC Alpha 21064A 266MHz	4.18	6.27
SGI Indy	MIPS R5000 150MHz	3.97	4.20
HP 9000 712/100	PA-7100LC 100 MHz	3.76	4.06

3.33.6 Documentation

Manuals

- ◇ Visualize J200, J210 technical reference manual (URL gone)
- ◇ Visualize J280 Owner's Guide (URL gone)
- ◇ Visualize J280 workstation upgrade instructions (URL gone)
- ◇ Visualize J280, J282, J2240 Service Handbook (URL gone)
- ◇ Visualize J282, J2240 Owner's Guide (URL gone)
- ◇ Visualize J282 workstation upgrade instructions (URL gone)
- ◇ Visualize J2240 workstation upgrade instructions (URL gone)

Articles

- ◇ Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost, Hewlett-Packard Journal (February 1996: HP)
- ◇ A New Memory System Design for Commercial and Technical Computing Products (.pdf) Thomas R. Hotchkiss, Norman D. Marschke, and Richard M. McClosky (Februar 1996: Hewlett-Packard Journal)
- ◇ HP 9000 J-Class Workstation Family Models J200, J210 and J210XC, HP Technical Computing, Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP VISUALIZE Workstation Deskside Model J280, HP Technical Computing, Hewlett-Packard Company (1997: mirror accessed January 2024)

3.34 HP Visualize J5000, J5600, J7000

HP Visualize J5000 and J7000 were PA-RISC workstations for the 3D graphics workstations market of the late 1990s. They were quipped with up to two 64-bit PA-8500 processors with large on-chip L1 caches and were basically the bigger brothers of HP Visualize C3000/C3600 with better expandability.

Their architecture was a major change from earlier J-Class workstations: New I/O devices were integrated, LASI I/O chipset and old GSC buses were removed. All devices now attach to PCI buses, I/O devices are connected to USB ports.

J5000 and J7000 shared the same case and architecture while J7000 supported more processors (four PA-8600) and more RAM (16 GB).

An upgrade path to HP Itanium (IA64 EPIC) was envisaged for Visualize workstations but not offered in the end. J5000 and J7000 were some of the last PA-RISC workstations offered by HP, before the ultimate HP c8000.

- ◇ HP Visualize J5000, HP 9000/785, were introduced in 1999 for \$13,118 (single) and \$24,313 (dual processor)
- ◇ HP Visualize J5600, HP 9000/785, were introduced in 2000 for \$21,108 (dual)
- ◇ HP Visualize J7000, HP 9000/785, were introduced in 1999
- ◇ HP Visualize J7600, HP 9000/785, were introduced in 2000?

3.34.1 System architecture

Processors

System	CPU	Speed	L1 Cache
HP Visualize J5000	1-2 PA-8500 PA-RISC 64-bit	440 MHz	512/1024 KB on-chip
HP Visualize J5600	1-2 PA-8600 PA-RISC 64-bit	552 MHz	512/1024 KB on-chip
HP Visualize J7000	1-4 PA-8500 PA-RISC 64-bit	440 MHz	512/1024 KB on-chip
HP Visualize J7600	1-4 PA-8600 PA-RISC 64-bit	552 MHz	512/1024 KB on-chip

Chipset

- ◇ HP Astro chipset, memory/Runway controller
- ◇ Four HP Elroy PCI bridges
- ◇ National 87560 (*SuperI/O*) for USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

System buses

- ◇ Runway CPU/memory bus
- ◇ PCI-64/33 high-performance device I/O bus
- ◇ PCI-64/66 high-performance graphics I/O bus
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ SCSI-3 Ultra2-Wide LVD bus main storage I/O
- ◇ IDE bus; CD/floppy I/O

Memory

- ◇ 278-pin 120 MHz ECC SDRAM DIMMs
- ◇ Takes 256/512/1024 MB modules
- ◇ J5000 8 slots
- ◇ J7000 16 slots
- ◇ 256 MB minimum, J5000: 8 GB (8×1024) maximum; J7000: 16 GB (16×1024) maximum.

Expansion slots

- ◇ Five PCI 64-bit/33 MHz, 5 V slots
- ◇ Two PCI 64-bit/66 MHz, 3.3 V slots
- ◇ I/O slots layout (from top to bottom):
 1. EMPTY
 2. PCI-64/33, 5 V
 3. PCI-64/33, 5 V
 4. PCI-64/66, 3.3 V
 5. PCI-64/33, 5 V
 6. PCI-64/33, 5 V
 7. PCI-64/66, 3.3 V
 8. PCI-64/33, 5 V

Storage

- ◇ Four SCSI 3.5" Ultra2-Wide LVD hard drives with 80-pin SCA connector
- ◇ 3.5" Floppy drive
- ◇ SCSI half-height 5.25" drive, external accessible

3.34.2 External ports

- ◇ SCSI-2 50-pin Ultra-Narrow single-ended
- ◇ SCSI-3 68-pin Ultra2-Wide LVD
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Fast Ethernet RJ45
- ◇ Two USB ports for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

3.34.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 11i v1 64-bit in version TCOE
 - 11.00 64-bit from version ACE9911
 - 10.20 32-bit from version ACE9912
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC, in 32-bit mode
- ◇ NetBSD open-source Unix-like, ported to PA-RISC, in 32-bit mode

3.34.4 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp
HP Visualize J5000	PA-8500 440 MHz	32.50	54.00	302	486
HP Visualize J5000	2 PA-8500 440 MHz			579	744
HP Visualize J5600	PA-8600 552 MHz	42.60	62.70	384	564
HP Visualize J5600	2 PA-8600 552 MHz	42.60	64.70	758	847
HP Visualize J7000	PA-8500 440 MHz	32.40	54.00	302	486
HP Visualize J7000	2 PA-8500 440 MHz			579	744

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.122: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP zx6000	McKinley 1.0 GHz	807	1422
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
SGI Origin 3200	MIPS R14000 600MHz	483	499
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359

HP i2000	Itanium Merced 800MHz 4MB	365	610
HP Visualize P750C	Pentium III 750MHz	325	219
Compaq AlphaServer ES40	Alpha 21264 500MHz	311	382
HP Visualize P500	Intel Pentium III 500MHz	231	191

3.34.5 Documentation

Manuals

- ◇ J5x00/J7x00 Owner's Guide (PDF, 4.5 MB) [parisc linux](#)
- ◇ J5x00/J7x00 Service Handbook (PDF, 4.4 MB) [parisc linux](#)
- ◇ VISUALIZE Workstation Memory Subsystem (PDF, 120 KB) [parisc linux](#)

3.35 HP Visualize J6000, J6700

HP Visualize J6000 and J6700 computers were small HP RISC workstations from the early 2000s aimed at the Unix graphics market, equipped with 64-bit PA-8600 and PA-8700 processors and usually shipped with HP Visualize FX graphics adapters.

The architecture was a major change from its J-Class predecessors. New I/O devices were integrated, the LASI I/O chip and old GSC bus were discarded. All devices now attach to PCI buses, I/O devices to USB.

The J6000 case can be used as desktop or fitted in a 19" rack 2U. An upgrade path to HP Itanium (IPF) was envisaged for Visualize workstations but not offered in the end. These were some of the last PA-RISC workstations offered by HP.

- ◇ HP Visualize J6000, HP 9000/785, were introduced in 2000 for \$13,118 (single) and \$22,575 (dual processor)
- ◇ HP Visualize J6700, HP 9000/785, were introduced in 2001 for \$26,454 (dual)
- ◇ HP Visualize J6750, HP 9000/785, were introduced in 2001

3.35.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP Visualize J6000	1-2 PA-8600 PA-RISC 64-bit	552 MHz	512/1024 KB on-chip
HP Visualize J6700	1-2 PA-8700 PA-RISC 64-bit	750 MHz	768/1536 KB on-chip
HP Visualize J6750	1-2 PA-8700+ PA-RISC 64-bit	875 MHz	768/1536 KB on-chip

Chipset

The system is built around the HP Astro chipset:

- ◇ HP Astro connects to the two processors via the Runway processor bus (2.0 GB/s), the memory bus (2.0 GB/s) and eight I/O channels ("ropes" — aggregate 2.0 GB/s) and contains both memory, I/O and cache controllers
- ◇ Four HP Elroy PCI bridges connect the PCI slots and I/O devices on the onboard PCI bus to the Astro with seven I/O channels
- ◇ National 87560 ("Super I/O"), integrates USB, RS232, parallel, floppy and IDE
- ◇ National 87415 IDE controller
- ◇ National USB controller
- ◇ Analog Devices AD1889 sound chip
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- ◇ Graphics through PCI boards:
 - *Optional* HP FireGL-UX 128 MB, PCI

- *Optional* HP Visualize FX10pro 128 MB, PCI
- *Optional* HP Visualize FXe 18 MB, PCI

System buses

- ◇ Runway CPU bus with 2.0 GB/s
- ◇ Memory bus, about 2.0 GB/s
- ◇ I/O bandwidth of around 1.75 GB/s with seven channels
 1. PCI 64/66 I/O slot on two channels—0.5 GB/s
 2. PCI 64/66 I/O slot on two channels—0.5 GB/s
 3. PCI 64/66 I/O slot on two channels—0.5 GB/s
 4. Onboard I/O devices (Fast Ethernet, SCSI, audio, IDE/USB etc.) on one channel—250 MB/s
- ◇ Three PCI-64/66 buses for expansion slots
- ◇ PCI-64/33 bus for onboard I/O devices
- ◇ SCSI-3 Ultra2-Wide LVD buses main storage I/O
- ◇ IDE bus for CD/DVD removable media

Memory

- ◇ 278-pin 120 MHz ECC SDRAM DIMMs
- ◇ 16 slots for 512 MB/1 GB DIMMs
- ◇ 1 GB to 16 GB supported

Expansion slots

- ◇ Three PCI 64-bit/66 MHz, 3.3 V slots

Storage

- ◇ Two SCSI 3.5" Ultra2-Wide LVD hard drives with 80-pin SCA connector
- ◇ Slim-line ATAPI CD-ROM

3.35.2 External ports

- ◇ SCSI-3 68-pin Ultra2-Wide LVD connector (SE)
- ◇ Two serial RS232C DB9
- ◇ Parallel DB25
- ◇ Fast Ethernet RJ45

- ◇ Two USB ports for keyboard & mouse
- ◇ Four phone jacks (microphone, headphones, line-in and line-out)

3.35.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 11i vi 64-bit only in TCOE and MTOE versions (j6700: September 2001)
 - 11.00 64-bit from version ACE9911 (j6700: July 2001 plus PHKL_24484)
 - 10.20 32-bit from version ACE9912 (j6700 will not work)
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC, in 32-bit mode
- ◇ NetBSD open-source Unix-like, ported to PA-RISC, in 32-bit mode

3.35.4 Benchmarks

System	CPU	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int fp
HP Visualize J6000	PA-8600 552 MHz	42.60	62.70	441	433	
HP Visualize J6000	2 PA-8600 552 MHz					9.7 8.0
HP Visualize J6700	PA-8700 750 MHz	57.60	85.90	603	581	
HP Visualize J6700	2 PA-8700 750 MHz					13.4 10.5
HP Visualize J6750	PA-8700+ 875 MHz			676	651	
HP Visualize J6750	2 PA-8700+ 875 MHz					14.9 11.5

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.125: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP zx6000	McKinley 1.0 GHz	807	1422
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
SGI Origin 3200	MIPS R14000 600MHz	483	499
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610
HP Visualize P750C	Pentium III 750MHz	325	219
Compaq AlphaServer ES40	Alpha 21264 500MHz	311	382
HP Visualize P500	Intel Pentium III 500MHz	231	191

3.35.5 Documentation

Manuals

- ◇ J6000 Service Handbook (PDF, 4.5 MB) Hewlett Packard
- ◇ J6000 Service Handbook, (PDF), Hewlett Packard
- ◇ HP Workstation j6750, Product Brief, Hewlett Packard (2003)
- ◇ J6000 Technical Reference (URL gone)
- ◇ J6700 Service Handbook (URL gone)
- ◇ J6700 Technical Reference (URL gone)

3.36 HP 9000 K-Class

HP 9000 K-Class are multiprocessor PA-RISC servers from the mid- to late-1990s. They were part of the HP 9000 800 server series with many expansion, I/O and processor options.

Based on U2/UTurn architecture, K-Class used 32-bit PA-7200 and 64-bit PA-8000 processors with four-way or six-way multiprocessing, depending on the specific model. They were very powerful and compact Unix servers in the 1990s.

Typical K-Class consisted of System Processing Unit (SPU), separate system console and optional UPS bundled into a single 19" rack. HP 9000 D-Class were technically very similar servers, smaller in size and slightly cheaper.

HP marketed also K-Class "Power Deskside Models", K260-EG, K460-EG and K460-XP, to be used as Visualize workstations with graphics adapters. These were at the time HP's "most expandable workstations" with "ultimate performance for engineering and scientific applications." K460-XP used HP Visualize-48XP graphics adapter for heavy 3D.

The first digit in the model number after "K" (1-5) indicates overall server type:

- ◇ K100: single-CPU with limited expandability
- ◇ K2x0: up to four CPUs, better expandability and memory
- ◇ K3x0: up to six CPUs and more I/O slots
- ◇ K4x0: up to four CPUs, more I/O slots and more memory
- ◇ K5x0: up to six CPUs and a different I/O configuration

The number after "K1/2/3/4/5" (00, 10, ... 80) indicates design, CPUs and chipset.

- ◇ 00/10/20: PA-7200 processor and UTurn architecture
- ◇ 50/60: PA-8000 processor and U2 architecture
- ◇ 70/80: PA-8200 processor and U2 architecture

In the 1990s, K-Class servers were part of the US Navy TAC-4 program technology refreshment, in which HP supplied HP 9000 RISC Unix computers to the Navy.

System	Model number	Introduced	Price
K100, K200, K400	HP 9000/809, HP 9000/819, HP 9000/829	March 1995	
K210, K410	HP 9000/839, HP 9000/849	September 1995	
K220, K420	HP 9000/859, HP 9000/869	March 1996	
K250, K450	HP 9000/802, HP 9000/804	August 1996	
K260, K460	HP 9000/879, HP 9000/889	August 1996	
K370, K570	HP 9000/898, HP 9000/899	May 1997	
K380, K580	HP 9000/800	February 1998	

3.36.1 System architecture

Processors

System	CPU	Speed	L1 Cache
HP 9000 K100	1 PA-7200 PA-RISC 32-bit	100 MHz	256/256 KB off-chip, 2 KB on-chip "assist"
HP 9000 K200/K400	1-4 PA-7200 PA-RISC 32-bit	100 MHz	256/256 KB off-chip, 2 KB on-chip "assist"

HP 9000 K210/K410	1-4 PA-7200 PA-RISC 32-bit	120 MHz	256/256 KB off-chip, 2 KB on-chip "assist"
HP 9000 K220/K420	1-4 PA-7200 PA-RISC 32-bit	120 MHz	1/1 MB off-chip, 2 KB on-chip "assist"
HP 9000 K250/K450	1-4 PA-8000 PA-RISC 64-bit	160 MHz	1/1 MB off-chip
HP 9000 K260/K460	1-4 PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
HP 9000 K370/K570	1-4 PA-8200 PA-RISC 64-bit	200 MHz	2/2 MB off-chip, picture CPU board
HP 9000 K380/K580	1-4 PA-8200 PA-RISC 64-bit	240 MHz	2/2 MB off-chip

Chipset

- ◇ PA-7200 HP U2 I/O adapter Runway to GSC bridge
- ◇ PA-8000/8200 HP UTurn I/O adapter Runway to GSC bridge
- ◇ HP MMC/SMC memory controllers
- ◇ HP Gecko BOA BC GSC+ Port
- ◇ HP LASI I/O chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Eole CAP/MUX
- ◇ Other I/O (serial, parallel)

System buses

- ◇ Runway CPU/memory, 100 MHz with 800 MB peak on Kx00, 120 MHz 960 MB/s on all others
- ◇ GSC+ bus for general system level I/O
- ◇ HSC bus for expansion I/O
- ◇ HP-PB bus for expansion I/O
- ◇ SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- ◇ SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Memory

- ◇ K100 512 MB maximum RAM
- ◇ K200, K210, K220 2 GB maximum RAM
- ◇ K250, K260, K370, K380, K400, K410, K420 4 GB maximum RAM
- ◇ K450, K460, K570, K580 8 GB maximum RAM
- ◇ 72-pin ECC SIMMs on special RAM boards

- ◇ Systems with a PA-8x00 need 50ns access time modules, PA-7200 models can take up to 60ns. Slower modules could work.

Expansion slots

- ◇ One slot for a GSC/HSC card on the core I/O board
- ◇ Four slots for HP-PB cards
- ◇ *K3x0* With 2-slot HSC I/O expansion module two more GSC/HSC cards possible
- ◇ *K4x0 and K4x0* With 2- or 4-slot HSC I/O expansion module two or four more GSC/HSC cards possible
- ◇ *K4x0* Four more HP-PB slots (eight in all)

Storage

- ◇ One tray for four Fast-Wide 68-pin SCSI-2 high-voltage differential hard drives
- ◇ One vertical tray for two 5.25" half-height drives, external accessible

3.36.2 External ports

- ◇ 68-pin HD SCSI-2 Fast-Wide high-voltage differential
- ◇ TP/RJ45 10BaseT 10 Mbit Ethernet
- ◇ Ethernet AUI 15-pin
- ◇ Two serial RS232C DB9, one for console, one for UPS
- ◇ DB25 male RS232C serial, for remote console via modem
- ◇ Parallel DB25
- ◇ Two PS/2 connectors for keyboard und mouse
- ◇ MDP-connector for a serial MUX
- ◇ *Kx50/Kx60/Kx70/Kx80* Four audio jacks

3.36.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit or 64-bit mode, in EOE, FOE, MCOE version
 - HP-UX 11.00 in 32-bit or 64-bit mode
 - HP-UX 10.20 32-bit, server version
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC (on K100, K200, K210, K220, K400, K410, K420)

- ◇ NetBSD, open-source Unix-like, ported to PA-RISC (on K100, K200, K210, K220, K400, K410, K420)

3.36.4 Dimensions

System	Height	Width	Depth	Weight
Stand-alone	635mm	432mm	698mm	59kg
Packaged	870mm	889mm	775mm	77kg

3.36.5 Benchmarks

System	SPEC95 int	SPEC95 fp	SPECrate95, int	SPECrate95, fp
HP 9000 K400	4.92	6.804P: 10.9	44.3 2P:87.9 4P:174	61.2 2P:117 4P:198
HP 9000 K410	5.92	8.154P: 13.0	53.3 2P:106 4P:210	73.4 2P:140 4P:238
HP 9000 K420	6.41	9.114P: 14.7	57.7 2P:114 4P:228	82.0 2P:157 4P:412
HP 9000 Kx50	10.7	18.8	96 2P:189 4P:375	169 2P:279 4P:383
HP 9000 K460	11.8	20.2	107 2P:212 4P:418	182 2P:418 4P:398
HP 9000 K570	14.6	23.0	1322P:2614P:5196P:767	2072P:3224P:4346P:489
HP 9000 K580	17.4	28.5	1572P:3124P:6106P:902	2572P:3984P:5326P:604

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.130: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
DEC Alphastation 500	DEC Alpha 21164 500MHz	15.0	20.4
SGI Origin 2000	MIPS R10000 250MHz 4MB	14.7	24.5
Sun Ultra 5 333	Sun UltraSPARC Ili 333MHz	14.1	18.3
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
IBM RS/6000 43P 150	PowerPC 604e 250 MHz	11.1	8.78
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
Siemens PCE-5S	Intel Pentium 100MHz	4.04	2.35
IBM RS/6000 43P	PowerPC 604 100 MHz	3.59	3.20

3.36.6 Documentation

- ◇ Service Manual HP 9000 K-Class Enterprise Servers and HP 3000 Model 9x9KS (PDF, 2.1 MB) [parisc linux](#)
- ◇ K-Class Installation Guide (HP 9000/Kxx0) (PDF) [parisc linux](#)
- ◇ K-Class Installation Guide (HP 3000/9x9KS) (PDF) [parisc linux](#)
- ◇ K-Class Owner's Guide (PDF) [parisc linux](#)
- ◇ Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and

Low Cost (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)

- ◇ J/K-Class Memory System description (PDF, HP Journal 2/96)
- ◇ HP VISUALIZE Workstations Power Deskside Models K260-EG and K460-EG, HP Technical Computing , Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ HP VISUALIZE Workstation Power Deskside Model K460-XP, HP Technical Computing , Hewlett-Packard Company (1997: mirror accessed January 2024)

3.37 HP L1000 and L2000 (rp5400/rp5450)

HP 9000 L-Class L1000 and L2000 are two or four-way multi-processor PA-RISC servers for rack-mounting, 7U in height. They are based on 64-bit processors and a rather conservative system architecture with an Astro/Elroy system design used in HP Visualize workstations like B2000, C3000 and C3600.

L-Class from 2000 was billed by HP as “Smart, Simple, and Stress-free” servers for “Internet-Age Computing”, i.e. dot-com boom e-commerce. They were slightly smaller solutions than the N4000 servers but still had a scalable architecture and functionality plus both “Unparalleled Internet manageability” and “The Internet edge”.

As with other HP 9000 servers of the late-1990s, L-Class were renamed to **rp** but stayed part of the HP 9000 series. Their L1500 and L3000 successors used a completely different system architecture. The L1000 and L2000 could be upgraded with a board-swap to Itanium 2-based rx5670 servers.

- ◇ HP L1000 rp5400 were introduced in 2000 for \$16,000
- ◇ HP L2000 rp5450 were introduced in 2000 for \$21,000

3.37.1 System architecture

Processors

The L1000/rp5400 systems support up to 2-way and the L2000/rp5450 up to 4-way SMP, with processors designated by the [-36, -44, -5X] suffix.. There two different system boards (A and B) in both systems, which supported different types of processors.

System	Suffix	CPU	Speed	L1 Cache
L1000 rp5400 A5576A	-36 -44	1-2 PA-8500 PA-RISC 64-bit 1-2 PA-8500 PA-RISC 64-bit	360 MHz 440 MHz	512/1024 KB on-chip 512/1024 KB on-chip
L1000 rp5400 A5576B	-36 -44 -5X	1-2 PA-8500 PA-RISC 64-bit 1-2 PA-8500 PA-RISC 64-bit 1-2 PA-8600 PA-RISC 64-bit	360 MHz 440 MHz 550 MHz	512/1024 KB on-chip 512/1024 KB on-chip 512/1024 KB on-chip
L2000 rp5400 A5191A	-36 -44	1-4 PA-8500 PA-RISC 64-bit 1-4 PA-8500 PA-RISC 64-bit	360 MHz 440 MHz	512/1024 KB on-chip 512/1024 KB on-chip
L2000 rp5400 A5191B	-36 -44 -5X	1-4 PA-8500 PA-RISC 64-bit 1-4 PA-8500 PA-RISC 64-bit 1-4 PA-8600 PA-RISC 64-bit	360 MHz 440 MHz 550 MHz	512/1024 KB on-chip 512/1024 KB on-chip 512/1024 KB on-chip

Upgrading between processors models required sometimes replacing other parts besides the processor, like the mainboard or power supply.

Chipset

- ◇ Astro memory/Runway controller, connects the memory, CPU bus and I/O
- ◇ Eight Elroy PCI bridges
- ◇ Two HP Diva Serial [GSP] Multiport UARTs
- ◇ DEC 21142/43 Fast Ethernet controller (*Tulip*)
- ◇ Two Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

System buses

- ◇ Runway CPU bus, 82.5 MHz with 1.36 GB/s bandwidth for up to four CPUs
- ◇ Memory bus, 1.36 GB/s
- ◇ Eight I/O data channels, each 133 MHz 256 MB/s — 2.1 GB/s aggregate
- ◇ Two PCI-64/33 I/O buses
- ◇ Six PCI-64/66 I/O buses
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ◇ ECC SDRAM DIMMs
- ◇ Take 256 MB/512 MB modules
- ◇ 16 slots (*8 of these slots are disabled on L1000s, namely slots 4a/b, 5a/b, 6a/b and 7a/b*)
- ◇ 256 MB (1×256) minimum, L1000: 8 GB (8×1 GB) maximum; L2000: 16 GB (16×1 GB) maximum.

Expansion slots

- ◇ Six PCI 64-bit/33 MHz slots on two independent buses:
 - pcio: Slots 1 and 2 are reserved for the Core I/O cards
 - pci1: Slots 3, 4, 5 and 6
 - All of the above slots are not hot-plug capable
- ◇ Six PCI 64-bit/66 MHz slots, each on an independent bus. These are hot-plug capable.
- ◇ *On L1000s only the slots 1, 2, 3, 8, 9, 10, 11 and 12 are usable!*
- ◇ Slot layout (from bottom to top):
 1. PCI-64/33, pcio, reserved for core I/O

2. PCI-64/33, pcio, reserved for core I/O
3. PCI-64/33, pci1
4. PCI-64/33, pci1
5. PCI-64/33, pci1
6. PCI-64/33, pci1
7. PCI-64/66, pci2, hot-pluggable
8. PCI-64/66, pci3, hot-pluggable
9. PCI-64/66, pci4, hot-pluggable
10. PCI-64/66, pci5, hot-pluggable
11. PCI-64/66, pci6, hot-pluggable
12. PCI-64/66, pci7, hot-pluggable

Storage

- ◇ Four trays for each one 3.5" Ultra2-Wide LVD SCSI hard drive with 80-pin SCA connector
- ◇ One tray for a half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external accessible

3.37.2 External ports

- ◇ SCSI-2 50-pin Ultra-Narrow single-ended
- ◇ 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- ◇ Serial RS232C DB9
- ◇ Fast Ethernet RJ45
- ◇ Ethernet RJ45 *Web Console*

3.37.3 Operating systems

- ◇ HP-UX: 64-bit 11.00, 11i v1 and 11i v2
- ◇ PA-RISC Linux: works.

3.37.4 Benchmarks

System	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp
L2000-44	33.70	47.20	?	?

3.37.5 Dimensions

System	Height	Width	Depth	Weight

	368mm	482mm	774mm	68kg
Rack-mounted	7U	482mm	774mm	68kg

3.37.6 Documentation

- ◇ rp5400 User Guide (URL gone)
- ◇ L-Class Home, Hewlett-Packard Company (2000: mirror accessed January 2024)

3.38 HP L1500 and L3000 (rp5430/rp5470)

The second version of HP 9000 L-Class are multi-processor Unix servers based on the Stretch chipset, also used in rp7400 N4000 servers. They are similar to L1000 and L2000, 7U rack-mountable with up to two or four processors, 8 GB or 16 GB RAM and a large set of I/O options and expandability.

L1500 have the same chassis and mainboards as L3000 with some I/O, memory and processors sockets deactivated in hardware, limiting the L1500 to about half of the L3000 capacity. Both could be upgraded to Itanium 2-based rx5670 servers.

- ◇ HP L1500 rp5430 were introduced in 2001
- ◇ HP L3000 rp5470 were introduced in 2001 for \$39,000

3.38.1 System architecture

Processors

rp5430 L1500 support up to 2-way and rp5470 L3000 up to 4-way multi-processing (SMP). There are several classes of possible processors, both shipped with the systems or later upgraded, designated by the [-5X, -7X, ..., -9X] suffix, based on different L3000 board configurations (A6144A, A6144B, A6840A).

System	Suffix	CPU	Speed	L1 cache
L1500 rp5430	-5X -6X -7X	1-2 PA-8600 PA-RISC 64-bit 1-2 PA-8700 PA-RISC 64-bit 1-2 PA-8700 PA-RISC 64-bit	550 MHz 650 MHz 750 MHz	512/1024 KB on-chip 768/1536 KB on-chip 768/1536 KB on-chip
L3000 rp5470 A6144A	-5X	1-4 PA-8600 PA-RISC 64-bit	550 MHz	512/1024 KB on-chip
L3000 rp5470 A6144B	-5X -6X -7X	1-4 PA-8600 PA-RISC 64-bit 1-4 PA-8700 PA-RISC 64-bit 1-4 PA-8700 PA-RISC 64-bit	550 MHz 650 MHz 750 MHz	512/1024 KB on-chip 768/1536 KB on-chip 768/1536 KB on-chip
L3000 rp5470 A6840A	-5X -6X -7X	1-4 PA-8600 PA-RISC 64-bit 1-4 PA-8700 PA-RISC 64-bit 1-4 PA-8700 PA-RISC 64-bit	550 MHz 650 MHz 750 MHz	512/1024 KB on-chip 768/1536 KB on-chip 768/1536 KB on-chip
Possible options (and/or upgradable):				
	-8X	PA-8700 PA-RISC 64-bit	875 MHz	768/1536 KB on-chip

Chipset

The chipset is based around the HP Stretch chipset:

- ◇ HP Prelude memory controller, the main crossbar of the system

- ◇ HP DEW Runway converters, attach the CPUs to the system bus
- ◇ HP IKE I/O controller connects the PCI bridges to the system main bus
- ◇ *rp5430* Seven HP Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- ◇ *rp5470* Ten HP Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- ◇ DEC 21142/43 Fast Ethernet controller (Tulip)
- ◇ Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

System buses

- ◇ Two Itanium system buses, 133 MHz DDR, each 2.1 GB/s peak, combined 4.3 GB/s aggregate. Both system buses connect to the central Prelude memory controller.
- ◇ Runway+/Runway DDR CPU buses, each 2.1 GB/s peak. Either two or four buses depending on the number of CPUs, with a combined aggregate 4.3 or 8.6 GB/s
- ◇ Two memory buses with combined 4.3 GB/s peak. 133 MHz DDR at 64-bit with ECC
- ◇ *rp5430* Eight I/O channels, each 133 MHz 256 MB/s — 2.1 GB/s aggregate
 - Five PCI-64/66 I/O buses for expansion slots
 - One PCI-64/33 I/O bus for core I/O
- ◇ *rp5470* Twelve I/O channels, each 133 MHz 256 MB/s — 3.2 GB/s aggregate
 - Eight PCI-64/66 I/O buses for expansion slots
 - Two PCI-64/33 I/O buses for expansion slots and core I/O
- ◇ SCSI-2 Ultra-Narrow single-ended bus
- ◇ Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ◇ ECC SDRAM DIMMs
- ◇ 256 MB, 512 MB and 1 GB modules supported
- ◇ 16 slots
- ◇ *rp5430* 8.0 GB maximum (system will not boot if more than 8.0 GB is installed)
- ◇ *rp5470* 16.0 GB maximum

Expansion slots

- ◇ Two *Twin-Turbo* PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via two I/O channels (aggregate 512 MB/s), hot-plug capable
- ◇ *rp5430*

- Four *Turbo* PCI 64-bit/66 MHz slots on three PCI buses, each on one I/O channel (256 MB/s), three of four slots are hot-plug capable
- ◇ *rp5470*
 - Six *Turbo* PCI 64-bit/66 MHz slots, each on an independent PCI bus, each on one I/O channel (256 MB/s), hot-plug capable
 - Two PCI 64-bit/33 MHz slots, shared bus on one I/O channel (256 MB/s)
- ◇ Two PCI 64-bit/33 MHz slots, reserved for LAN/SCSI and GSP (management) cards, on a shared bus, on one I/O channel (256 MB/s)
- ◇ All PCI slots are 5 V keyed
- ◇ Slot layout (from bottom up):
 1. PCI-64/33, pci0, reserved (LAN/SCSI)
 2. PCI-64/33, pci0, reserved (GSP)
 3. PCI-64/33, pci1, shared [not available on rp5430]
 4. PCI-64/33, pci1, shared [not available on rp5430]
 5. PCI-64/66, pci2, Turbo, hot-pluggable [not available on rp5430]
 6. PCI-64/66, pci3, Turbo, hot-pluggable [not available on rp5430]
 7. PCI-64/66, pci4, Turbo, hot-pluggable
 8. PCI-64/66, pci5, Turbo, hot-pluggable
 9. PCI-64/66, pci6, Turbo, hot-pluggable
 10. PCI-64/66, pci7, Turbo, hot-pluggable
 11. PCI-64/66, pci8, Twin-Turbo, hot-pluggable
 12. PCI-64/66, pci9, Twin-Turbo, hot-pluggable

Storage

- ◇ Four trays for 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA, hot-plug
- ◇ One tray for half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external

3.38.2 External ports

- ◇ SCSI-2 50-pin Ultra-Narrow single-ended
- ◇ 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- ◇ Three serial RS232C DB9 (local console, remote console, general purpose)
- ◇ Fast Ethernet RJ45
- ◇ Fast Ethernet RJ45 *Web Console*

3.38.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - 11.00 64-bit version
 - 11i v1 64-bit version
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s

3.38.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
L3000-5Xrp2470	388	376	4.52-CPU: 8.94-CPU: 17.4	4.42-CPU: 8.34-CPU: 14.5
L3000-7Xrp2470	581		6.7 2-CPU: 12.9	

3.38.5 Dimensions

System	Height	Width	Depth	Weight
	368mm	482mm	775mm	68kg
Rack-mounted	7U	482mm	775mm	68kg

3.38.6 Documentation

Manuals

- ◇ User Guide rp5400 Family of Servers (URL gone)

Articles

- ◇ hp server rp5400 series entry-level UNIX servers technical whitepaper (URL gone)

3.39 HP N4000 (rp7400)

N4000 were mid-range PA-RISC servers with up to eight processors, the original N-Class from the turn of the century, later renamed rp7400. They were based on HP Stretch architecture, also used in L1500 and L3000 and HP Itanium (IA64) platforms.

N4000 were released during the dot-com boom between 1999 and 2000 and sold as “Server for the Internet-Age”, focused on e-commerce and web-ready features like QoS, control and security for “the Web”.

HP claimed “HP 9000 N-Class servers give you more of what you need to meet” for the “new Internet business paradigm” which “is having an enormous impact on enterprise IT systems—more applications, more users, and more traffic than ever before.”

N4000 were shipped in two models with different system boards: A3639A and A3639B, the later renamed rp7400 was shipped with another mainboard, model A3639C.

- ◇ HP 9000 N4000, A3639A and A3639B, were introduced in 1999 for \$40,000
- ◇ HP Integrity rp7400, A3639C were introduced in 2001 for \$39,000

Later HP rp7405 and rp7410 servers were also called N4000 with similar I/O options and expandability in almost the same chassis with a different architecture (Cell). Itanium 2/IA64 processors were planned for N4000 but apparently never offered.

3.39.1 System architecture

Processors

rp7400 N4000 support one to eight processors, denoted by [-36, -44 ... -7X] suffix. Not all earlier N4000 support the later processors and maximum number of CPUs.

System		CPU	Speed	LI cache
HP 9000 N4000 A3639A	-36	1-8 PA-8500 PA- RISC 64-bit	360 MHz	512/1024 KB on-chip
	-44	1-8 PA-8500 PA- RISC 64-bit	440 MHz	512/1024 KB on-chip
HP 9000 N4000 A3639B	-36	1-8 PA-8500 PA- RISC 64-bit	360 MHz	512/1024 KB on-chip
	-44	1-8 PA-8500 PA- RISC 64-bit	440 MHz	512/1024 KB on-chip
	-5X	1-8 PA-8500 PA- RISC 64-bit	550 MHz	512/1024 KB on-chip
HP rp7400 A3639C	-36	1-8 PA-8500 PA- RISC 64-bit	360 MHz	512/1024 KB on-chip
	-44	1-8 PA-8500 PA- RISC 64-bit	440 MHz	512/1024 KB on-chip
	-5X	1-8 PA-8500 PA- RISC 64-bit	550 MHz	512/1024 KB on-chip
	-6X	1-8 PA-8500 PA- RISC 64-bit	650 MHz	768/1536 KB on-chip
	-7X	1-8 PA-8600 PA- RISC 64-bit	750 MHz	768/1536 KB on-chip
		1-8 PA-8700 PA- RISC 64-bit		
	1-8 PA-8700 PA- RISC 64-bit			

Chipset

rp7400 are based on HP Stretch chipset, which is also used in L1500 and L3000 servers. Stretch has four main components:

1. HP Prelude memory controller is the main crossbar of the system
2. Four HP DEW Runway converters attach the processors to the main buses
3. Two HP IKE I/O controllers connect PCI bridges via I/O channels
4. 14 HP Elroy PCI bridges (LBAs) convert the IKE I/O to PCI buses

The rest of the system is implemented with common parts:

- ◇ DEC 21142/43 Fast Ethernet controller
- ◇ Dual-channel Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- ◇ Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

System buses

The system bus architecture provides more bandwidth than could be used under practical circumstances. The designers probably counted on future IA64 CPU upgrades.

- ◇ Two Itanium system buses, 133 MHz, each 2.1 GB/s peak, 4.3 GB/s aggregate
- ◇ Eight Runway+ CPU buses, each 2.1 GB/s peak, aggregate 17.0 GB/s
- ◇ Four Memory buses, each 2.1 GB/s peak, aggregate 8.5 GB/s
- ◇ 24 I/O channels, each 133 MHz 265 MB/s, aggregate 6.4 GB/s
- ◇ 14 PCI-64/66 I/O buses for expansion slots
- ◇ Three SCSI-3 Ultra2-Wide LVD main storage I/O buses, one for each internal drive and one for external devices

Memory

- ◇ ECC SDRAM DIMMs
- ◇ 16 slots
- ◇ 256 MB, 512 MB, 1 GB and 2 GB modules supported
- ◇ 32 GB maximum

Expansion slots

- ◇ Ten *Twin-Turbo* PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via two I/O links/ropes (aggregate 530 MB/s), hot-plug capable
- ◇ Two *Turbo* PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via one I/O link/rope (265 MB/s), hot-plug capable (one of these two Turbo slots is reserved for Core I/O LAN/SCSI)

- ◇ All slots keyed for 5.0 V (support either 5.0 V or universal PCI cards)

Storage

- ◇ Two internal Ultra SCSI LVD 3.5" drives with SCA connector, hot-pluggable

3.39.2 External ports

- ◇ 68-pin VHDCI Ultra2 LVD external SCSI
- ◇ Three serial RS232C DB9 (local console, remote console, general purpose) via a DB25 "M cable"
- ◇ Fibre channel
- ◇ 10/100 Mbit Ethernet TP/RJ45
- ◇ 10/100 Mbit Ethernet TP/RJ45 *Web console*

3.39.3 Operating systems

- ◇ HP-UX: 64-bit 11.00 (ACE 9911), 11i v1, 11i v2 and 11i v3
- ◇ PA-RISC Linux

3.39.4 Benchmarks

System	SPECrate95, int	SPECrate95, fp	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
N4000-36	215 4-CPU: 830 8-CPU: 1650	355 4-CPU: 1055 8-CPU: 1720				
N4000-44	306 4-CPU: 1209 8-CPU: 2408	462 4-CPU: 1495 8-CPU: 2075				
N4000-5X	376 4-CPU: 1479 8-CPU: 2939	528 4-CPU: 1682 8-CPU: 2336				
N4000-6X rp7400			493	489	5.7 2-CPU: 11.3 4-CPU: 22.1 8-CPU: 42.6	5.7 2-CPU: 10.4 4-CPU: 19.3 8-CPU: 30.5
N4000-7X rp7400			551	524	6.4 2-CPU: 12.5 4-CPU: 24.6 8-CPU: 46.7	6.1 2-CPU: 11.0 4-CPU: 20.5 8-CPU: 32.1

3.39.5 Documentation

- ◇ rp7400 Hardware Manual Hewlett-Packard Company (May 2002)
- ◇ hp server rp7400 system architecture and design guide, Hewlett-Packard Company (February 2002, product number 5981-0154EN) (URL gone)

- ◇ N-Class - The Server for the Internet-Age, Hewlett-Packard Company (2000: mirror accessed January 2024)

3.40 HP N4000 (rp7405/rp7410)

HP rp7405/rp7410 N4000 N-Class servers are up to 8-way multiprocessing servers which could be hardware-partitioned into logical servers, two nPartitions. Based on the same 10U rack chassis as rp7400/N4000, these newer rp7405 and rp7410 have a completely overhauled system and I/O architecture.

The *Core Electronic Complex* is a modified HP Superdome cell system architecture for two cells with each up to four processors, sixteen RAM slots and central chipset.

rp7405 were apparently an entry-level version of rp7410, based on the same hardware with the same capabilities but shipped in smaller configurations. Upgrades to a “full” rp7410 were possible, probably with a modified firmware for unlocking.

- ◇ HP rp7405 N4000, A7111A, A7112A and A7113A, were introduced in 2002 for \$50,959
- ◇ HP rp7410 N4000, A6752A, were introduced in 2002 for \$92,250

3.40.1 System architecture

Processors

rp7405 and rp7410 support two to eight processors, based on their system board, designated by the [-6X, -7X ... -9X] suffix.

System		CPU	Speed	L1 cache	L2 cache
rp7405 A7111A	-6X -7X	1-2 PA-8700 PA-RISC 64-bit 1-2 PA-8700 PA-RISC 64-bit	650 MHz 750 MHz	768/1536 KB on-chip 768/1536 KB on-chip	
rp7405 A7112A	-6X -7X	1-4 PA-8700 PA-RISC 64-bit 1-4 PA-8700 PA-RISC 64-bit	650 MHz 750 MHz	768/1536 KB on-chip 768/1536 KB on-chip	
rp7405 A7113A	-6X -7X	1-8 PA-8700 PA-RISC 64-bit 1-8 PA-8700 PA-RISC 64-bit	650 MHz 750 MHz	768/1536 KB on-chip 768/1536 KB on-chip	
rp7410 A6752A	-6X -7X -8X	2-8 PA-8700 PA-RISC 64-bit 2-8 PA-8700 PA-RISC 64-bit 2-8 PA-8700+ PA-RISC 64-bit	650 MHz 750 MHz 875 MHz	768/1536 KB on-chip 768/1536 KB on-chip 768/1536 KB on-chip	

Chipset

- ◇ HP Cell controller (CC), central chipset and crossbar, provides links for four processors, two memory banks, I/O via SBA, PDH and firmware, and second cell.
- ◇ HP Master I/O controller (SBA) on I/O backplane on each cell, provides up to 32 links that connect to slave I/O controllers LBA.

- ◇ Core I/O for I/O functions on two cards MP/SCSI and LAN/SCSI:
 - Two dual-channel Symbios Logic 53C1010 Ultra160 SCSI controllers
 - Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 (MP/SCSI)
 - Gigabit Ethernet networking (LAN/SCSI)
 - Fast-Ethernet (DEC 21142/43) Management LAN (MP/SCSI)
 - Optional second Core I/O card, for redundancy or partitioning
- ◇ 18 Elroy PCI bridges (LBAs) convert links/ropes from the SBA to PCI bus (only 9 of these 18 LBAs are used when only one cell board is installed)

System buses

- ◇ Runway+ DDR CPU bus, 125 MHz DDR 64-bit, 2.0 GB/s per CPU, 16.0 GB/s max
- ◇ Memory bus 4.0 GB/s for each cell, aggregate 8.0 GB/s max
- ◇ XBC cell-to-cell link 8.0 GB/s aggregate
- ◇ SBA cell-to-I/O link 2.0 GB/s on each cell, aggregate 4.0 GB/s max
- ◇ 32 I/O links (ropes), 12-bit wide, 265 MB/s, 8.5 GB/s I/O peak
 - 28 ropes link to 14 *Twin-Turbo* slots via 14 LBAs
 - Two ropes link to two *Turbo* PCI slots via two LBAs
 - Two ropes connect via two LBAs to Core I/O MP/SCSI cards
- ◇ 14 PCI-64/66 I/O buses for expansion slots
- ◇ Two PCI-64/33 I/O buses for expansion slots for Core I/O SCSI/LAN
- ◇ Two PCI-64/33 I/O buses for Core I/O MP/SCSI
- ◇ Two SCSI-3 Ultra160 LVD main storage I/O buses one on each cell
- ◇ Ultra SCSI SE for removable media

Memory

- ◇ ECC DIMMs, low-voltage TTL, 125 MHz frequency
- ◇ 256 MB, 512 MB and 1 GB modules supported
- ◇ 16 slots on each cell board
- ◇ 32 GB maximum, 64 GB with “future” memory modules

Expansion slots

There are up to 16 PCI 64-bit/66 MHz slots in the I/O cage, which can be fully accessed when using a system with two cells. With one cell board only seven slots are available. One PCI slot is dedicated to Core I/O card set.

Storage

- ◇ Four trays for low-profile 3.5" Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector, hot-plug
- ◇ One tray for a half-height 5.25" 50-pin Ultra-Narrow SE SCSI drive, external accessible

3.40.2 External ports

- ◇ 68-pin VHDCI Ultra160 LVD external SCSI external channel from LAN/SCSI board
- ◇ Three serial RS232C DB9 local console, remote console, UPS via DB25 "M cable" on MP/SCSI board
- ◇ 10/100 Mbit Ethernet TP/RJ45 Management LAN on MP/SCSI board
- ◇ Gigabit Ethernet TP/RJ45 on LAN/SCSI board

3.40.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.00 (maybe), 64-bit (1997)
 - HP-UX 11i v1, 64-bit (2000)
 - 11i v2, 64-bit (2005)
 - 11i v3, 64-bit (2007)

3.40.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
N4000-7Xrp7410			4-CPU: 25.38-CPU:49.9	4-CPU: 18.98-CPU:36.8

3.40.5 Documentation

Manuals

- ◇ User Guide hp rp7405/7410 Servers (URL gone)
- ◇ hp server rp7410 whitepaper (URL gone)

3.4.1 HP Integrity rp3410 and rp3440

HP Integrity rp3410 and rp3440 were some of the last PA-RISC-based HP servers, released in 2004 in a 2U rack-mountable case for data centers.

The rp34x0 use dual-core PA-8800 or PA-8900 PA-RISC processors in a HP zx1 (Itanium) system design that was also used for Itanium 2 systems. There was an upgrade path to Intel/HP IA64 Itanium 2 processors by swapping CPUs and boards.

The HP 9000 rp4410 and rp4440 servers are technically similar with more computing and I/O options.

rp	Introduced	Price
rp3410rp3410-2	2004	\$4,000
rp3440rp3440-4	2004	\$7,000

HP dropped PA-RISC from its computer (server) portfolio soon after, replacing it with Itanium.

3.4.1.1 System architecture

Processors

The rp3410 (rp3410-2) supports a single processor, the rp3440 (rp3440-4) up to 2-way multi-processing (SMP).

- ◇ rp3410:
 - 1 dual-core PA-8800 800 MHz with 3 MB L1 and 32 MB off-chip L2 cache
- ◇ rp3440:
 - 1 or 2 dual-core PA-8800 900 MHz-1.0 GHz with 3 MB L1 and 32 MB off-chip L2 cache
 - 1 or 2 dual-core PA-8900 800 MHz-1.1 GHz with 3 MB L1 and 64 MB off-chip L2 cache
- ◇ On some entry-level versions only one of the two CPU cores per processor is active
- ◇ An upgrade path to HP Itanium 2 processors was available

Chipset

The systems are based on the HP zx1 chipset with two main components, the memory and I/O controller (MIO) and the I/O adapters (IOAs). zx1 is almost a crossbar chipset: the memory controller acts as the crossbar switch which links processors, memory and I/O.

- ◇ Pluto (MIO) is the zx1 memory and I/O controller and connects the central system buses:
 1. Processor bus of 6.4 GB/s for one or two CPUs
 2. Two independent memory buses, each 4.25 GB/s
 3. I/O channels, six on rp3410 with 3.0 GB/s and eight on rp3440 with 4.0 GB/s

The MIO also contains both memory and cache controllers.

- ◇ rp3410: Five Mercury I/O adapters IOAs for PCI-X slots
- ◇ rp3440: Seven Mercury I/O adapters IOAs for PCI-X slots

- ◇ PCI-X slots and I/O channels:
 1. PCI-X 64/133 I/O slot on two channels—1.0 GB/s
 2. PCI-X 64/133 I/O slot on one channel—0.5 GB/s
 3. *rp3440* PCI-X 64/133 I/O slot on one channel—0.5 GB/s
 4. *rp3440* PCI-X 64/133 I/O slot on one channel—0.5 GB/s
 5. Management LAN and serial ports (iLO card) on one channel—0.5 GB/s
 6. Ultra160 SCSI and Gigabit Ethernet controllers on one channel—0.5 GB/s
 7. IDE and USB controllers one channel—0.5 GB/s
- ◇ Dual-channel Ultra160 SCSI controller, LSI Logic 53C1030
- ◇ Gigabit Ethernet controller, Broadcom Tigon 3
- ◇ IDE controller, PCI649
- ◇ USB2.0 controller

System buses

- ◇ Itanium 2/zx1 processor bus, 128-bit, 200 MHz, 6.4 GB/s
- ◇ Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s, aggregate 8.5 GB/s
- ◇ *rp3410*:
 - Six zx1 I/O channels/buses, aggregate 3.0 GB/s
 - Two PCI-X 64/133 I/O buses
- ◇ *rp3440*:
 - Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
 - Four PCI-X 64/133 I/O buses
- ◇ SCSI-3 Ultra160 LVD storage I/O bus
- ◇ IDE secondary storage I/O bus

Memory

- ◇ PC2100 DDR CL2 SDRAM DIMMs
- ◇ Twelve slots
- ◇ 1 GB minimum memory
- ◇ *rp3410*: 6 GB maximum memory
- ◇ *rp3440*: 32 GB maximum memory
- ◇ 8.5 GB/s memory bandwidth
- ◇ 80ns memory latency

Expansion slots

- ◇ One PCI-X 64-bit/133 MHz slot with 1 GB/s data rate
- ◇ rp3410: One PCI-X 64-bit/133 MHz slot with 512 MB/s data rate
- ◇ rp3440: Three PCI-X 64-bit/133 MHz slots with 512 MB/s data rate
- ◇ All PCI slots are 3.3 V

Storage

- ◇ Three 3.5" Ultra160 LVD SCSI hard drives, 1" height, 68-pin
- ◇ Slimline IDE CD or DVD drive

3.41.2 External ports

- ◇ Three serial RS232C DB9 for local console, remote console, general purpose
- ◇ Four USB 2.0 ports
- ◇ TP/RJ45 Gigabit Ethernet
- ◇ HP Integrated Lights Out iLO system management card with Fast-Ethernet Web console
- ◇ Ultra160 SCSI 68-pin

3.41.3 Operating systems

- ◇ HP-UX11i v1, 11i v2, 11i v3
- ◇ PA-RISC Linux

3.41.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
rp3440 1.0 GHz dualcore			2-core: 18.7 2-CPU/4-core: 37.1	2-core: 19.2 2-CPU/4-core: 32.6

3.41.5 Dimensions

System	Height	Width	Depth	Weight
Rack-mounted	2U	483mm	680mm	23kg
Stand-alone	495mm	295mm	675mm	26kg

3.41.6 Documentation

Manuals

- ◇ User Service Guide HP 9000 rp3410 and HP 9000 rp3440 (.pdf) Hewlett-Packard Development Company (2010, sixth edition)
- ◇ Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers URL gone)

3.42 HP Integrity rp4410 and rp4440

HP Integrity rp4410 and rp4440 were some of the last PA-RISC-based HP servers, based on up to four dual-core PA-8800 or PA-8900 processors and HP zx1 chipset, released by HP in 2004.

The rp44x0 are technically very similar to the like the HP 9000 rp3410 and rp3440 servers, based on the same zx1 architecture and PA-RISC processors. The systems can be rack-mounted in 4U or be used stand-alone.

rp	Introduced	Price
rp4410rp4410-4	2005	
rp4440rp4440-8	2004	\$21,000

3.42.1 System architecture

Processors

The rp4410 (rp4410-4) supports 2-way multi-processing (SMP), the rp4440 (rp4440-8) up to 4-way multi-processing (SMP).

- ◇ Dual-core PA-8800 900 MHz-1.0 GHz with 3 MB on-chip L1 and 32 MB off-chip L2 cache
- ◇ Dual-core PA-8900 800 MHz-1.1 GHz with 3 MB on-chip L1 and 64 MB off-chip L2 cache
- ◇ There probably was an upgrade path to Itanium 2/IA64 processors.

Chipset

The systems are based on the HP zx1 chipset with three main components — the MIO memory and I/O controller, the IOAs I/O adapters and the SMEs scalable memory expanders.

- ◇ Pluto is the zx1 MIO memory and I/O controller and connects the system buses:
 1. Processor bus of 6.4 GB/s for one or two dual-CPU modules
 2. Two independent memory buses with each 6.4 GB/s
 3. Eight I/O channels with aggregate 4.0 GB/s
- ◇ Six zx1 SMEs scalable memory expanders attach to two independent zx1 memory buses
- ◇ Six Mercury zx1 IOAs I/O adapters connect the PCI-X slots
 1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
 3. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
 4. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
 5. Core I/O adapters like SCSI, Ethernet etc. on two channels — 1.0 GB/s
- ◇ Dual-channel Ultra320 SCSI controller
- ◇ Dual-port Gigabit Ethernet
- ◇ USB2.0 controller

- ◇ IDE controller

System buses

An interesting aspect of the rp4400's bus setup is that the same 6.4 GB/s processor bus is shared between up to two CPUs on the rp4410 and up to four CPUs on the rp4440.

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s
- ◇ Two independent zx1 memory buses, 200 MHz, each 6.4 GB/s
- ◇ Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- ◇ Two PCI-X 64/133 I/O buses
- ◇ Two PCI-X 64/66 I/O buses
- ◇ SCSI-3 Ultra320 LVD storage I/O bus
- ◇ IDE secondary storage I/O bus

Memory

- ◇ PC2100 parity ECC DDR CL2 SDRAM DIMMs
- ◇ 16- or 32-DIMM carrier board
- ◇ 1 GB minimum memory
- ◇ 128 GB maximum memory
- ◇ 12.8 GB/s memory bandwidth
- ◇ 105ns memory latency

Expansion slots

- ◇ Two PCI-X 64-bit/133 MHz slots, each on an independent bus, hot-plug
- ◇ Four PCI-X 64-bit/66 MHz slots, on two shared buses, hot-plug
- ◇ All PCI slots are 3.3 V

Storage

- ◇ Two bays for 3.5" Ultra320 LVD SCSI hard drives, hot-plug
- ◇ Slimline bay for optional IDE CD or DVD drive

3.42.2 External ports

- ◇ Three serial RS232C DB9 for local console, remote console, general purpose
- ◇ Two USB 2.0 ports

- ◇ Two Gigabit Ethernet, TP/RJ45
- ◇ Two Ultra320 SCSI ports
- ◇ HP Integrated Lights Out iLO system management card with Fast-Ethernet Web console

3.42.3 Operating systems

- ◇ HP-UX_{III} v1, v2, v3
- ◇ PA-RISC Linux could be a possibility, as the similar rp3400s are supported, albeit unofficially

3.42.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
rp4440 1.0 GHz dualcore			2-core: 18.6 2-CPU/4-core: 37.0 4-CPU/8-core: 73.2	2-core: 19.3 2-CPU/4-core: 34.7 4-CPU/8-core: 55.4

3.42.5 Dimensions

System	Height	Width	Depth	Weight
Rack-mounted	4U	440mm	690mm	53kg
Stand-alone	530mm	261mm	695mm	53kg

3.42.6 Documentation

Manuals

- ◇ User Service Guide HP 9000 rp4410 and HP 9000 rp4440 (.pdf, 17 MB) Hewlett-Packard Development Company (2009, fifth edition)
- ◇ Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers (URL gone)

3.43 HP Integrity rx1600 and rx1620

The rx1600 (later rx1600-2) is a 1U rack-mountable server with up to two Itanium 2 Deerfield processors. The later introduced rx1620 supported newer Fanwood Itanium 2 processors. Both classes of CPUs are specified/ marketed as “low-voltage.”

3.43.1 System architecture

Processors

Table 3.147: All caches are on-die (L1, L2 and L3).

CPU	Speed	L1 Cache	L2 Cache	L3 Cache
rx1600 and rx1600-2				
1-2 Itanium 2 <i>Deerfield</i>	1.0 GHz	16/16 KB	256 KB	1.5 MB
rx1620				
1-2 Itanium 2 <i>Fanwood</i>	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2 Itanium 2 <i>Fanwood</i>	1.6 GHz	16/16 KB	256 KB	3.0 MB

Chipset

The systems are based on the HP zx1 chipset with two central components — Pluto and Mercury.

◇ Pluto: main chipset controller connects to three system buses:

1. Processor bus
2. Two independent memory buses
3. Seven I/O channels

It contains both memory and cache controllers as well.

◇ Five Mercury I/O adapters: connect PCI-X slots and I/O devices to Mercury

1. PCI-X 64/133 slot on two channels with 1.0 GB/s
2. PCI-X 64/133 slot on two channels with 1.0 GB/s
3. Gigabit Ethernet and Ultra320 SCSI (Core I/O) on PCI on one channel with 0.5 GB/s
4. IDE, USB, Fast-Ethernet LAN (Core I/O) on PCI on one channel with 0.5 GB/s
5. Management Ethernet LAN, VGA, serial (Core I/O) on PCI on one channel with 0.5 GB/s

The remained consists of standard third-party I/O chipsets:

- ◇ Gigabit Ethernet (Broadcom 5701)
- ◇ rx1600: Fast Ethernet
- ◇ Two-channel Ultra320 SCSI controller (LSI 53C1030)
- ◇ Ultra ATA-100 IDE controller (PCI649)
- ◇ Serial controller, DUART (16550A-compatible)
- ◇ 10/100 Ethernet for management (Intel 82550)

- ◇ Management processor card included by default
- ◇ Processor Dependent Hardware (PDH) Controller
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)
- ◇ EHCI USB controller

System buses

- ◇ Itanium 2/zx1 processor bus—200 MHz DDR with 6.4 GB/s bandwidth on 1.0 and 1.3 GHz processors, 266 MHz DDR with 8.5 GB/s on 1.6 GHz processors (rx1620)
- ◇ Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s—aggregate 8.5 GB/s memory bandwidth
- ◇ Seven zx1 I/O channels/buses, aggregate 3.5 GB/s
- ◇ Four PCI-X 64/133 I/O buses for expansion cards
- ◇ Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 ECC DDR CL2 SDRAM DIMMs
- ◇ Takes up to 2 GB modules
- ◇ Eight slots
- ◇ DIMMs must be installed in quads
- ◇ 1 GB minimum (4×256 MB)
- ◇ 16 GB maximum (8×2 GB)
- ◇ 8.5 GB/s memory bandwidth

Expansion slots

- ◇ PCI-X 64-bit/133 MHz slot, full-length
- ◇ PCI-X 64-bit/133 MHz slot, half-length
- ◇ All PCI slots are 3.3 V

Storage

- ◇ Two internal 3.5" bays for 1" height Ultra320 SCSI SCA 80-pin hard drives, hot-plug;
- ◇ Slimline bay for optional IDE CD or DVD drive

3.43.2 External ports

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ rx1600: 10/100 Ethernet, TP/RJ45
- ◇ rx1620: Second Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Ultra320 SCSI 68-pin HDCI
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Two USB 2.0 ports
- ◇ Two serial RS232C DB9

3.43.3 Operating systems

- ◇ HP-UX: 11i v1, 11i v2 and 11i v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

3.43.4 Benchmarks

System	Processor	SPEC2000int	SPEC2000fp	SPEC2000rate int	SPEC2000rate fp
rx1600	Deerfield 1.0 GHz	837	1382	9.71 2-CPU: 19.1	16.02-CPU: 27.6
rx1620-2	Fanwood 1.3 GHz	1178	2214	13.7 2-CPU: 27.0	25.72-CPU: 42.7
rx1620-2	Fanwood 1.6 GHz	1452	2692	16.8 2-CPU: 33.2	31.22-CPU: 50.4

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.149: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
i2000	Itanium Merced 800 MHz	365	610
C3750	PA-RISC PA-8700+ 875 MHz	678	674
zx6000	McKinley 1.0 GHz	807	1422
c8000	PA-RISC PA-8800 1.0 GHz	1001 (est.)	
AMD	Athlon XP 2.2GHz	1080	873
HP ProLiant	Intel Xeon 2.8GHz	1249	1081

Intel	Pentium 4 520 2.8GHz	1290	
zx6000	Madison 1.5 GHz	1315	2106
AMD	Opteron 250 2.4GHz	1619	1652
Sun Ultra 40	AMD Opteron 256 3.0GHz	1957	

3.43.5 Documentation

Manuals

- ◇ HP Integrity rx1600 Operation and Maintenance (PDF) Hewlett-Packard Development Company (2010)
- ◇ HP Integrity rx1620 Operations Guide (PDF) Hewlett-Packard Development Company (2012)
- ◇ HP Integrity rx1620 Maintenance Guide (PDF) Hewlett-Packard Development Company (2012)
- ◇ Overview of the HP Integrity rx1600, rx2600, rx4640, and rx5670 servers technical whitepaper (URL gone)
- ◇ Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers (URL gone)

3.43.6 Dimensions

Height	Width	Depth	Weight
1U	482mm	680mm	22kg

3.44 HP Integrity rx2600 and rx2620

HP Integrity rx2600 were rack-mountable HP Itanium workstations and servers based on the HP zx6000 workstation. Released between 2003 and 2004, rx2600 were marketed as entry-level servers for “technical and commercial applications” with “superior java and web benchmark as well leading integer and floating point performance.”

HP rx2600 *servers* and zx6000 *workstations* were closely related, with some minor technical differences in system design – cooling, AGP slots, management ports. Both have a similar system design and can be mounted either 19” racks (2U) or placed in a desktop tower-like enclosure

Integrity rx2600 supports up to two Itanium 2 processors with up to 1.5 GHz (Madison processor) and is targeted for PCI-X devices and thus does not feature the AGP port of the workstation-oriented zx6000. System design was based on HP zx1 chipset which was used for Itanium and PA-RISC computers in the early 2000s.

The rx2600 was later marketed as rx2600-2 and superseded by the rx2620, which supported newer processors.

3.44.1 System architecture

Processors

Table 3.151: All caches are on-die (L1, L2 and L3).

CPU	Speed	L1 Cache	L2 Cache	L3 Cache
rx2600 and rx2600-2				
1-2 Itanium 2 <i>Deerfield?</i>	1.0 GHz	16/16 KB	256 KB	1.5 MB
1-2 Itanium 2 <i>Madison</i>	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2 Itanium 2 <i>Madison</i>	1.4 GHz	16/16 KB	256 KB	1.5 MB
1-2 Itanium 2 <i>Madison</i>	1.5 GHz	16/16 KB	256 KB	6.0 MB
rx2620				
1-2 Itanium 2 <i>Madison?</i>	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2 Itanium 2 <i>Madison?</i>	1.6 GHz	16/16 KB	256 KB	3.0 MB
1-2 Itanium 2 <i>Montecitodual-core</i>	1.4 GHz	16/16 KB	1024/256 KB	12 MB
1-2 Itanium 2 <i>Montecitodual-core</i>	1.6 GHz	16/16 KB	1024/256 KB	18 MB

Chipset

The systems are based on HP’s zx1 chipset, which consists of two main components — the MIO (memory and I/O controller) and the IOAs (I/O adapters):

- ◇ HP zx1 chipset, Itanium design with MIO and IOA
- ◇ HP Plutozx1 MIO is the main chipset controller and connects processor bus, two memory buses and seven I/O channels. Contains memory and cache controllers.
- ◇ Seven HP Mercuryzx1 IOAs connect PCI-X slots and I/O devices to the zx1 MIO
- ◇ Gigabit Ethernet (Broadcom 5701)
- ◇ Two-channel Ultra320 SCSI controller (LSI 53C1030), PCI-64 66 MHz
- ◇ Ultra ATA-100 IDE controller (PCI649)

- ◇ Serial controller, DUART (16550A-compatible)
- ◇ 10/100 Ethernet for management (Intel 82550)
- ◇ Management processor card (“ECI card”) — serial/remote management and VGA
- ◇ Radeon VGA graphics onboard
- ◇ EHCI USB controller
- ◇ Processor Dependent Hardware (PDH) Controller
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard Management Controller for IPMI management interface (ARM7 RISC)

System buses

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- ◇ Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s — aggregate 8.5 GB/s memory bandwidth
- ◇ Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
 1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
 2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 4. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 5. Core I/O: IDE, USB, serial, (rx2600: Fast-Ethernet) on PCI 64/133 on one channel — 0.5 GB/s
 6. Core I/O: Gigabit Ethernet and Ultra320 SCSI on PCI 64/133 on one channel — 0.5 GB/s
 7. Management: Ethernet LAN, VGA, serial on PCI 64/133 on one channel — 0.5 GB/s
- ◇ Four PCI-X 64/133 I/O buses for expansion cards
- ◇ Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 ECC DDR CL2 SDRAM DIMMs
- ◇ rx2600 up to 2 GB modules
- ◇ rx2620 up to 4 GB modules
- ◇ Twelve slots
- ◇ DIMMs must be installed in quads
- ◇ 1 GB minimum (4×256 MB)
- ◇ rx2600 24 GB maximum (12×2 GB)

- ◇ *rx2620* 32 GB maximum (8×4 GB—the remaining four slots cannot be used)
- ◇ 8.5 GB/s memory bandwidth

Expansion slots

- ◇ Four PCI-X 64-bit/133 MHz slots, full-length
- ◇ All PCI slots are 3.3 V

Storage

- ◇ Three internal 3.5" bays for Ultra320 SCSI SCA 80-pin hard drives, hot-plug; drives 1 and 2 are on one SCSI channel, drive 3 on the second SCSI channel
- ◇ Slimline bay for optional IDE CD or DVD drive

3.44.2 External ports

- ◇ *rx2600* Gigabit Ethernet, TP/RJ45
- ◇ *rx2620* Dual-Port Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor, needs break-out cable for serial ports
- ◇ Four USB 2.0 ports
- ◇ Two serial RS232C DB9

3.44.3 Operating systems

- ◇ *rx2600*: HP-UX11i v1.6, 11i v2 and 11i v3
- ◇ *rx2620* HP-UX11i v2 and 11i v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit Enterprise Edition
- ◇ OpenVMS, minimum V8.2

3.44.4 Dimensions

System	Height	Width	Depth	Weight
Tower	495mm	297mm	673mm	25kg
Rack-mounted	2U	482mm	680mm	22kg

3.44.5 Benchmarks

System	Processor	SPEC2000int	SPEC2000 fp	SPEC2000rate int	SPEC2000rate fp
rx2600900 MHz 1.5 MB	674	1151	7.8 2-CPU: 15.5	2-CPU:	
rx2600 1.0 GHz 3.0 MB	810	1427	9.4 2-CPU: 18.7	2-CPU:	
rx2600 1.3 GHz 3.0 MB	1073	1808	12.42-CPU: 24.8	2-CPU:	
rx2600 1.5 GHz 6.0 MB	1408	2119	15.32-CPU: 30.5	2-CPU:	
rx2620-2 1.3GHz 3.0 MB	1170	2229	13.62-CPU: 26.9	15.9 2-CPU: 27.7	
rx2620-2 1.6GHz 3.0 MB	1408	2553	16.32-CPU: 32.3	29.6 2-CPU: 48.5	
rx2620-2 1.6GHz 6.0 MB	1535	2675	17.82-CPU: 35.5	31.0 2-CPU: 51.5	

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.154: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
i2000	Itanium Merced 800 MHz	365	610
C3750	PA-RISC PA-8700+ 875 MHz	678	674
zx6000	McKinley 1.0 GHz	807	1422
c8000	PA-RISC PA-8800 1.0 GHz	1001 (est.)	
AMD	Athlon XP 2.2GHz	1080	873
HP ProLiant	Intel Xeon 2.8GHz	1249	1081
Intel	Pentium 4 520 2.8GHz	1290	
zx6000	Madison 1.5 GHz	1315	2106
AMD	Opteron 250 2.4GHz	1619	1652
Sun Ultra 40	AMD Opteron 256 3.0GHz	1957	

3.44.6 Documentation

- ◇ Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000
- ◇ HPE Integrity rx2620 Server User Service Guide (PDF) Hewlett-Packard Enterprise (2015)
- ◇ HPE Integrity rx2600 Servers - Product Information Reference, HPE Support Center
- ◇ HP Integrity rx2600 Server Quick Specs, HPE, HP DA-11716 April 2006
- ◇ HP Integrity rx2600 Server Getting Started Guide, HP June 2003, A9664-90020
- ◇ HP Integrity rx2600 server and HP workstation zx6000 Quick Setup, HP 2003, A9664-90001
- ◇ ATI RADEON 7500 PCI Graphics Controller Installation Guide, HP 2005, AB551-96002
- ◇ HP Integrity and HP 9000 Integrated Lights-Out, HP 2005, 5971-4274
- ◇ HP Integrity rx2600 server data sheet, HP 2003, 5981-7543EN
- ◇ Overview of the HP Integrity rx1600-2, rx2600-2, and rx4640-8 servers Whitepaper, HP 2004, 5982-5031EN
- ◇ The HP Integrity server family, HP 2004, 5982-4741EN

3.45 HP Integrity rx4610

The Integrity rx4610 were HP's first-generation Itanium servers based on up to four *Merced* Itanium processors in an 7U rack-mountable case. The rx4610 offered many I/O and expansion options with ten PCI slots on four PCI buses (attached to 2.1 GB/s I/O bandwidth) and up to 64 GB of main memory but was limited to only two internal SCSI drives.

The rx4610 is based on the Intel Itanium reference architecture—the 82460GX chipset, which looks like a mix of PC-style (Frontside Bus to the processor) and PA-RISC (I/O “ropes” from the central chipset to PCI converters) platforms. The other HP system with *Merced* processors and the 82460GX was the HP i2000 workstation. Both the i2000 and rx4610 were rather slow and buggy when compared to contemporary PA-RISC systems.

3.45.1 System architecture

Processors

Table 3.155: All caches are on-die (L1, L2 and L3).

CPU	Speed	L1 Cache	L2 Cache	L3 Cache
2-4 Itanium 1 <i>Merced</i>	733 MHz	16/16 KB	96 KB	2.0 MB
2-4 Itanium 1 <i>Merced</i>	800 MHz	16/16 KB	96 KB	4.0 MB

Chipset

The rx4610 is based on Intel's 82460GX chipset with four main components:

1. **82460GX SAC** (System Address Chip) is the central chipset part:
 - ◇ System bus (FSB) for up to four processors — 2.1 GB/s (the SAC connects to the address and control parts of the FSB)
 - ◇ Four I/O channels to which the PCI buses attach (via the WXBs/PXB)—each channel is 533 MB/s
 - ◇ Connection to the SDC
 - ◇ Address/control access to the main memory
2. Three **82460GX WXBs** (Wide eXpansion Bridges) which connect the PCI 64/66 buses via three I/O channels to the SAC
 - ◇ One I/O channel connects to two PCI 64/66 slots
 - ◇ One I/O channel connects to three PCI 64/66 slots
 - ◇ One I/O channel connects to three PCI 64/66 slots and the SCSI controller
3. **82460GX PXB** (PCI eXpansion Bridge) connects the PCI 64/33 bus and core I/O (Ethernet LAN, PS/2, parallel, serial, IDE, USB, VGA) and the baseboard management controller via one I/O channel to the SAC
4. **82460GX SDC** (System Data Chip) is the central memory data controller:
 - ◇ It connects to the data part of the FSB system main bus

- ◇ Has a private link to the SAC (PD)
- ◇ Connects to the memory subsystem (data transfers, in contrast to the SAC's Address/control access)

The rest of the chipset is made up of standard (third-party) I/O components:

- ◇ Dual-channel Ultra3 SCSI controller
- ◇ Intel 82559 Fast Ethernet controller
- ◇ ATI Rage 128VR 64-bit SVGA with 16 MB video memory
- ◇ Baseboard management controller (BMC) for IPMI, EMP and WoL
- ◇ I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- ◇ ATA-33 IDE controller (on IFB)
- ◇ USB controller (on IFB)
- ◇ LPC47B27 Super I/O (serial and PS/2 ports controller)

System buses

- ◇ System bus, 32bit 133 MHz DDR (“double-pumped”), 2.1 GB/s, ECC-protected
- ◇ Memory bus, 266 MHz, 4.2 GB/s peak
- ◇ 2.1 GB/s aggregate I/O bandwidth with four 533 MB/s I/O channels
- ◇ Three PCI 64/66 I/O buses for expansion slots
- ◇ PCI 64/33 I/O bus for expansion slots and onboard devices

Memory

- ◇ Two memory boards, each supports up to 32 GB of memory
- ◇ 72-bit DIMMs
- ◇ 32 slots on each memory board
- ◇ Up to 1 GB modules
- ◇ 1 GB minimum (*i.e.*, one board)
- ◇ 64 GB maximum (64×1 GB— 32 modules on two boards)

Expansion slots

- ◇ Eight PCI 64-bit/66 MHz slots, full-length, hot-plug, 3.3 V
 - Two slots are on one I/O channel
 - Three slots are on one I/O channel
 - Three slots are on one I/O channel which is shared with the SCSI subsystem
- ◇ Two PCI 64-bit/33 MHz slots, full-length, 5.0 V

Storage

- ◇ Two internal 3.5" bays for 1" height LVD SCA2 SCSI hard drives
- ◇ Optional IDE DVD drive in 0.5" carrier
- ◇ Optional IDE floppy drive (LS120) in 0.5" carrier

3.45.2 External ports

- ◇ 10/100 Ethernet, TP/RJ45
- ◇ VGA graphics
- ◇ External SCSI
- ◇ Two PS/2 for keyboard and mouse
- ◇ Parallel port
- ◇ Two 9-pin serial
- ◇ Two USB

3.45.3 Operating systems

- ◇ HP-UX11i v1.5,
- ◇ Linux for Itanium
- ◇ Windows 64-bit

3.45.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000rate int	SPEC2000 rate fp
rx4610733 MHz 2 MB		625		7.22-CPU; 12.74-CPU; 20.1
rx4610800 MHz 4 MB	379	701	4.4	8.12-CPU; 14.24-CPU; 22.4

3.45.5 Dimensions

Height	Width	Depth	Weight
7U	444mm	711mm	68kg

3.45.6 Documentation

Manuals

- ◇ hp server rx4610 User Guide (URL gone)
- ◇ An overview of the Itanium-based hp rx4610 server whitepaper (URL gone)

3.46 HP Integrity rx4640

The Integrity rx4640 (rx4640-8) are second-generation Itanium servers from HP with up to four Itanium 2 processors in a 4U rack-mountable case. In contrast to the rx4610 predecessors (7U, first-generation Itanium) the rx4640 is a completely new design based on the HP zx1 Itanium chipset, with double the I/O bandwidth and three times the processor and memory bandwidth. The rx4640 features a large amount of maximum memory (128 GB) but fewer PCI slots (six) and only the same small number of two internal SCSI drives.

The rx4640 was later marketed as rx4640-8.

3.46.1 System architecture

Processors

Table 3.158: L1 and L2 caches are on-die, L3 is off-chip

CPU	Speed	L1 Cache	L2 Cache	L3 Cache
rx4640 original				
1-4 Itanium 2 <i>Madison</i>	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-4 Itanium 2 <i>Madison</i>	1.5 GHz	16/16 KB	256 KB	6.0 MB
rx4640 later versions				
1-4 Itanium 2 <i>Madison</i>	1.6 GHz	16/16 KB	256 KB	6.0 MB
1-4 Itanium 2 <i>Madison</i>	1.6 GHz	16/16 KB	256 KB	9.0 MB
1-4 Itanium 2 <i>Montvale</i> dual-core	1.6 GHz	16/16 KB	1024/256 KB	18 MB
1-4 Itanium 2 <i>Montvale</i> dual-core	1.6 GHz	16/16 KB	1024/256 KB	24 MB
1-4 Itanium 2 mx2 <i>Hondodual-CPU</i>	1.1 GHz	16/16 KB	256 KB	4.0 MB _{32 MB L4}

Chipset

The rx4640 are based on HP's zx1 chipset, which consists of three main components — the MIO (memory and I/O controller), the IOAs (I/O adapters) and the SMEs (scalable memory expanders):

- ◇ Pluto zx1 MIO (memory and I/O controller) is the main chipset controller and connects the three central system buses:
 1. Processor bus (6.4 GB/s at 200 MHz DDR)
 2. Two independent memory buses (each 6.4 GB/s)
 3. Eight I/O channels (aggregate 4.0 GB/s, via the IOAs, see below)

The zx1 MIO also contains both memory and cache controllers.

- ◇ Six zx1 SMEs (scalable memory expanders) attach to two independent zx1 memory buses (each 6.4 GB/s with three SMEs)
- ◇ Six Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0 GB/s on eight 0.5 GB/s channels
 1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
 2. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s

3. Two PCI-X 64/66 I/O slots on one channel—0.5 GB/s
4. Two PCI-X 64/66 I/O slots on one channel—0.5 GB/s
5. Core I/O: SCSI and Gigabit Ethernet on one channel—0.5 GB/s
6. Core I/O: Management LAN, IDE, USB, serial and VGA on one channel—0.5 GB/s

The rest are standard third-party I/O chips:

- ◇ Gigabit Ethernet (Broadcom 5701)
- ◇ Two-channel Ultra320 SCSI controller (LSI 53C1030)
- ◇ Ultra ATA-100 IDE controller (PCI649)
- ◇ EHCI USB controller
- ◇ Serial controller, DUART (16550A-compatible)
- ◇ “Diva” remote management processor—serial and LAN
- ◇ Processor Dependent Hardware (PDH) Controller
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)

System buses

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- ◇ Two independent zx1 memory buses, 200 MHz, each 6.4 GB/s—aggregate 12.8 GB/s memory bandwidth
- ◇ Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- ◇ Two PCI-X 64/133 I/O buses
- ◇ Two PCI-X 64/66 I/O buses
- ◇ PCI-X 64/66 I/O bus (for SCSI/Gigabit Ethernet onboard)
- ◇ PCI 32/33 I/O bus (for IDE/USB/management onboard devices)
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ DDR200 CL2 registered ECC SDRAM DIMMs, 200 MHz, 184-pin 2.5 V
- ◇ Takes up to 4 GB modules
- ◇ 16-DIMM or 32-DIMM memory carrier board
- ◇ DIMMs must be installed in quads
- ◇ 1 GB minimum (4×256 MB)

- ◇ 64 GB maximum with 16-DIMM board (16×2 GB), 128 GB maximum with 32-DIMM board (32×4 GB)
- ◇ 12.8 GB/s memory bandwidth

Expansion slots

- ◇ Four PCI-X 64-bit/66 MHz slots, hot-plug. 3.3 V
- ◇ Two PCI-X 64-bit/133 MHz slots, hot-plug. 3.3 V

Storage

- ◇ Two internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug; each drive can be configured on one separate channel—if they are on the same channel the second can be used for external SCSI devices
- ◇ Slimline bay for optional IDE CD or DVD drive

3.46.2 External ports

- ◇ Dual-port Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- ◇ VGA graphics
- ◇ Two external Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor card, needs break-out cable for three serial ports
- ◇ Four USB 2.0 ports
- ◇ Two (three?) serial RS232C DB9

3.46.3 Operating systems

- ◇ HP-UX11i v2 and 11i v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

3.46.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
rx4640 1.3 GHz 3.0 MB	1132	1891	13.1 2-CPU: 25.8 4-CPU: 51.4	21.9 2-CPU: 37.9 4-CPU: 57.4

rx4640 1.5 GHz 6.0 MB	1404	2161	16.3 2-CPU: 32.5 4-CPU: 64.2	25.1 2-CPU: 43.2 4-CPU: 65.6
rx4640-8 1.5 GHz 4.0? MB	1372	2502	15.9 2-CPU: 31.7 4-CPU: 62.2	29 2-CPU: 48.3 4-CPU: 70.5
rx4640-8 1.6 GHz 9 MB	1590	2712	4-CPU: 72.5	4-CPU: 77.9

3.46.5 Dimensions

Height	Width	Depth	Weight
4U	482mm	690mm	45kg

3.46.6 Documentation

Manuals

- ◇ User Service Guide HP Integrity rx4640 Server (URL gone)
- ◇ Overview of the HP Integrity rx1600-2, rx2600-2, and rx4640-8 servers technical whitepaper (URL gone)
- ◇ Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper (URL gone)

3.47 HP Integrity rx5670

The HP Integrity rx5670 are rack-mountable multi-processor Itanium 2 servers with up to four processors. Closely matching the rx4640 system architecture, the rx5670 is based on HP's zx1 Itanium chipset. PA-RISC L-Class servers (built into the same system/chassis) could be upgraded by a "board-swap" — changing the main system board, processors and support hardware — to Itanium 2 rx5670s (applies to HP rp5400/rp5450 (L1000/L2000) and HP rp5430/rp5470 (L1500/L3000)).

3.47.1 System architecture

Processors

Table 3.161: All caches are on-die (L1, L2 and L3).

CPU	Speed	L1 Cache	L2 Cache	L3 Cache
1-4 Itanium 2 <i>Madison</i>	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-4 Itanium 2 <i>Madison</i>	1.3 GHz	16/16 KB	256 KB	6.0 MB

All caches are on-die (L1, L2 and L3).

Chipset

The rx5670 is based on HP's zx1 chipset, which consists of three main components — the MIO (memory and I/O controller), the IOAs (I/O adapters) and the SMEs (scalable memory expanders):

- ◇ Pluto zx1 MIO (memory and I/O controller) is the main chipset controller and connects the three central system buses:
 1. Processor bus (6.4 GB/s at 200 MHz DDR)
 2. Two independent memory buses (each 6.4 GB/s with six SMEs)
 3. Eight I/O channels (aggregate 4.0 GB/s, via the IOAs, see below)

The zx1 MIO also contains both memory and cache controllers.

- ◇ Twelve zx1 SMEs (scalable memory expanders), six on each DIMM/memory carrier board, attach to two independent zx1 memory buses (each 6.4 GB/s)
- ◇ Eight Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0 GB/s on eight 0.5 GB/s channels
 1. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
 4. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
 5. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
 6. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s

7. One PCI 64/66 slot for Gigabit Ethernet and one SCSI controller (Core I/O) on one channel — 0.5 GB/s
8. One PCI 64/66 slot for management LAN, serial and one SCSI controller (Core I/O); and one PCI 64/33 slot for optional graphics/USB on one channel (with the other slot) — 0.5 GB/s

The rest are standard third-party I/O chips, implemented on Core I/O cards in two or three PCI slots

- ◇ Dual-channel Ultra160 SCSI controllers (LSI 53C1010)
- ◇ SCSI controller (LSI 53C896)
- ◇ Gigabit Ethernet (Broadcom 5701)
- ◇ Serial controller, DUART (16550A-compatible)
- ◇ IBM PCI-X to PCI-X bridge
- ◇ “Diva” remote management processor — serial and LAN
- ◇ Optional Radeon VGA graphics (with USB on one card)
- ◇ Optional EHCI USB controller

System buses

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- ◇ Two independent zx1 memory buses, 266 MHz, each 6.4 GB/s — aggregate 12.8 GB/s memory bandwidth
- ◇ Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- ◇ Three PCI-X 64/133 I/O buses for expansion slots
- ◇ Three PCI-X 64/66 I/O buses for expansion slots
- ◇ PCI-X 64/66 I/O bus for Core I/O expansion slots
- ◇ PCI 64/33 I/O bus for graphics/USB slot
- ◇ Two SCSI-3 Ultra160 (LVD) storage I/O buses

Memory

- ◇ PC2100 ECC DDR CL2 SDRAM DIMMs
- ◇ Takes up to 2 GB modules
- ◇ One or two 24-DIMM memory carrier boards
- ◇ DIMMs must be installed in quads
- ◇ 1 GB minimum (4×256 MB)
- ◇ 96 GB maximum with two 24-DIMM boards (48×2 GB)
- ◇ 12.8 GB/s memory bandwidth

Expansion slots

- ◇ Three PCI-X 64-bit/133 MHz slots
- ◇ Six PCI-X 64-bit/66 MHz slots
- ◇ Two PCI slots preloaded with core I/O cards
- ◇ One PCI 64/33 MHz slot for graphics/USB card (optional)

Storage

- ◇ Four internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug, each pair of drives is connected to one separate controller and each drive in each pair is on a separate channel
- ◇ One open bay for removable SCSI media drives — DVD/DDS

3.47.2 External ports

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 management network with web console (on management processor card)
- ◇ Ultra160 SCSI 68-pin
- ◇ Three serial RS232C DB9 (console, remote console, general purpose)
- ◇ Four USB 2.0 ports (optional)
- ◇ VGA graphics (optional)

3.47.3 Operating systems

- ◇ HP-UX11i v1.6, 11i v2 and 11i v3
- ◇ Linux for Itanium
- ◇ Windows Server 2003 64-bit
- ◇ OpenVMS

3.47.4 Benchmarks

System	SPEC2000 int	SPEC2000 fp	SPEC2000 rate int	SPEC2000 rate fp
rx5670 900 MHz 1.5 MB	673	1151	7.81 2-CPU: 15.5 4-CPU: 30.4	13.3 2-CPU: 24.5 4-CPU: 38.7
rx5670 1.0 GHz 3.0 MB	807	1431	9.36 2-CPU: 18.6 4-CPU: 36.8	16.6 2-CPU: 30.7 4-CPU: 49.3

rx5670 1.3 GHz 3.0 MB	1066	1814	12.4 2-CPU: 24.5 4-CPU: 48.6	21.0 2-CPU: 37.3 4-CPU: 57.2
rx5670 1.5 GHz 6.0 MB	1312	2108	15.2 2-CPU: 30.3 4-CPU: 60.0	24.5 2-CPU: 42.6 4-CPU: 66.4

3.47.5 Dimensions

Height	Width	Depth	Weight
7U	482mm	740mm	72kg

3.47.6 Documentation

Articles

- ◇ Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper (PDF) Hewlett-Packard Development Company (October 2003, first edition, 5982-1595EN)

3.48 Convex Exemplar SPP1000, SPP1200, SPP1600

Convex Exemplar SPP1000, SPP1200 and SPP1600 are scalable 32-bit PA-RISC mainframes with HP PA-7100 or PA-7200 processors, released by Convex in 1994. Previous Convex designs used custom Convex processors. With the new SPP mainframes, Convex switched to using HP PA-RISC processors, first 32-bit and later 64-bit, utilizing its partnership with HP (and PRO).

In the early 1990s, Convex and HP started a close collaborating, which began with jointly marketed cluster-computing solutions based on HP 9000 in 1992. Soon after, HP licensed HP-UX Unix to Convex in 1993 and finally HP become a value-added reseller (VAR) for Convex before acquiring the company outright in 1995. SPP1200 were quickly taken over into the HP product portfolio, the later jointly developed Exemplar SPP2000 was a plain HP product by the Exemplar division.

Convex SPP1000, SPP1200 and SPP1600 were available in different types: the CD Compact Design, XA eXtended Architecture hypernodes and XA clusters.

- ◇ SPP1000/CD, SPP1200/CD, SPP1600/CD: Single compact systems with up to sixteen processors or two SPP XA Hypernodes coupled together, sold as a single, non-clusterable system.
- ◇ SPP1000/XA, SPP1200/XA, SPP1600/XA: Single XA hypernode with up to eight processors and provisions for linking other systems via SCI.
- ◇ SPP1000/XA, SPP1200/XA, SPP1600/XA: Cluster of up to sixteen XA hypernodes coupled via SCI/TCI rings with up to 128 processors, ccNUMA.

Convex Exemplar architecture is based on a 5x5 *crossbar*, a central internal switching component that connects resources to each other by forming matrix connections between input and output ports. “5x5” because the crossbar has five ports for processors, memory and I/O.

Nodes and clusters are controlled by separate workstations, often IBM RS/6000 workstation with AIX. In a cluster only one node had a control workstation. HP 9000/715 workstations were also used as so-called teststations.

- ◇ SPP1000/CD were introduced in 1994 for \$145,000-\$750,000
- ◇ SPP1000/XA were introduced in 1994 for \$550,000-\$8 million
- ◇ SPP1200/CD were introduced in 1995 for \$160,000 and up
- ◇ SPP1200/XA were introduced in 1995 for \$586,000 and up
- ◇ SPP1600 were introduced in 1996

Development of the HP Convex *Exemplar architecture* peaked later with HP 9000 V-Class servers: non-clusterable HP 9000/V2200 and V2250 and up to four-way clusterable HP 9000/V2500 and V2600.

3.48.1 System architecture

Processors

Table 3.164: PA-7100 CPUs had a very unusual 2MB “expanded” primary cache

System		CPU	Speed	L1 cache
Convex SPP1000/CD Compact	2-16	PA-7100 PA-RISC 32-bit	100 MHz	2 MB off-chip
Convex SPP1000/XA Hypernode	2-8	PA-7100 PA-RISC 32-bit	100 MHz	2 MB off-chip

Convex SPP1000/XA Cluster	8-128	PA-7100 PA-RISC 32-bit	100 MHz	2 MB off-chip
Convex SPP1200/CD Compact	2-16	PA-7200 PA-RISC 32-bit	120 MHz	512 KB off-chip
Convex SPP1200/XA Hypernode	2-8	PA-7200 PA-RISC 32-bit	120 MHz	512 KB off-chip
Convex SPP1200/XA Cluster	8-128	PA-7200 PA-RISC 32-bit	120 MHz	512 KB off-chip
Convex SPP1600/CD Compact	2-16	PA-7200 PA-RISC 32-bit	120 MHz	1 MB off-chip
Convex SPP1600/XA Hypernode	2-8	PA-7200 PA-RISC 32-bit	120 MHz	1 MB off-chip
Convex SPP1600/XA Cluster	8-128	PA-7200 PA-RISC 32-bit	120 MHz	1 MB off-chip

It is not quite clear how CD models relate to XA models—XA clusters consist of several 2-8 CPU hypernodes while CD models were shipped with up to 16 processors. Either CDs are different machines than XA hypernodes or they are simply two XA hypernodes coupled together without additional SCI/CTI expansion possibilities.

Chipset

Exemplar chipset is based on a custom Convex design with Convex five-port crossbar, later improved on the SPP2000 with eight ports and used in HP V-Class.

- ◇ **5x5 nonblocking crossbar**, with five crossbar ports, is the central part of the system, connects to four “functional units” (memory, SCI links and processor) and with the fifth port to the local system I/O.
 - The four functional units contain each a memory controller, SCI controller and an “agent” for two processors.
 - Memory and processor use different data links to the crossbar—memory access *always* goes over the crossbar, even from a processor to the memory in the same functional unit.
 - The crossbar is implemented in Gallium arsenide gate arrays, GaAs with 250K transistors, a rarity, very expensive and difficult to handle.
- ◇ Four **CPU Agents** attach to the crossbar and provide access for the processors to the memory via the crossbar port shared with the memory controller.
- ◇ Four **Convex Coherent Memory Controllers CCMCs** attach each one four-way interleaved memory board to the crossbar. The CCMCs additionally do cache coherency and interface to Convex SCI (CTI) link for inter-hypernode connection. CTI interface and/or CCMC were apparently also GaA chips.
- ◇ **Exemplar I/O subsystem** connects to the fifth crossbar port and attaches I/O subsystem controllers to the crossbar and memory and processors.

System buses

- ◇ Total crossbar bandwidth 1.25 GB/s, five 250 MB/s ports
- ◇ CPU/Memory bandwidth 1.0 GB/s, four 250 MB/s ports shared with memory
- ◇ I/O bandwidth 250 MB/s with one crossbar port
- ◇ *SPP1000* Four SBus I/O buses for expansion slots
- ◇ *SPP1200/SPP1600* Eight SBus I/O buses for expansion slots

- ◇ Attachments to SCI rings, interconnection via four one-dimensional rings bandwidth of 2.4 GB/s
- ◇ SCSI-2 storage I/O bus

Memory

- ◇ DRAM, memory is up to eight-way interleaved per node
- ◇ Two to eight memory boards per node
- ◇ *XA single nodes* up to 2 GB of memory (512 MB per memory board)
- ◇ *CD nodes* up to 4 GB of memory

Expansion slots

- ◇ *XA single nodes* 8 SBus slots
- ◇ *CD nodes* 16 SBus slots
- ◇ Apparently really the same SBus used by Sun in their SPARC workstations

Storage

- ◇ 20 internal SCSI drives

3.48.2 Clustering

Multiple SPP1000/XA systems can be connected to form a single large system.

- ◇ Up to sixteen SPP1000/SPP1200/SPP1600 XA models can be clustered together to form a system with up to
 - 128 processors
 - 32 GB of RAM
 - 64 SBus slots
 - 320 SCSI drives
- ◇ Clustered SPP Exemplar are ccNUMA computers.
- ◇ Multiple systems (nodes) are connected via four CTI rings: each uni-directional ring attaches to the same CCMC memory controller on different nodes.
- ◇ The four rings are implementations of the IEEE Standard 1596-1992 SCI, called by Convex CTI — Convex Toroidal Interconnect.
- ◇ Each ring is only unidirectional and has a bandwidth of 600 MB/s, 16-bit differential, 300 MHz clock
- ◇ Complete CTI bandwidth is thus 2.4 GB/s.
- ◇ Each node's main memory is globally accessible from other nodes on the CTI network: local memory is globally shared.

- ◇ Memory access to global memory goes from the processor through the local crossbar to the local functional unit whose memory controller is associated with the remote memory

3.48.3 External ports

- ◇ SCSI depending on installed controller
- ◇ Console/control connections for the control workstation, the teststation

3.48.4 Operating systems

The Exemplar Operating System, SPP-UX, was a scalable Unix based on Mach developed by Convex for its SPP1000 and SPP2000 mainframe computers with up to 128 or 512 processors, released between 1993 and 1999. SPP-UX implemented a distributed architecture that was supposed to look like (emulate) HP-UX for developers but was very different below the userland.

SPP-UX kernel and architecture were based on a Mach 3.0 distributed microkernel and was taken over by HP during the acquisition of Convex and its Exemplar SPP computers. Each hypernode of the SPP computers ran an independent instance of the Mach microkernel.

There were three (four) main layers for SPP-UX:

1. **Distributed kernel:** Based on an enhanced Mach 3.0 microkernel, supposedly OSF 1/AD Mach from OSF RI, that was targeted for coupled SMP systems to support highly parallel applications; message-passing paradigm for NUMA computers
2. **HP-UX compatibility:** Second operating system layer compatible to HP-UX, to enable running HP-UX applications on SPP-UX, supposedly emulated HP-UX APIs and ABIs; management of distributed resources, processors, simultaneous users, process scheduler; supported parallel jobs as well as multiprocessing of single-thread
3. **Extensions and features:** Central management, open systems and standards like POSIX, specialized programming and development environment
4. Lastly, the **applications:** Possible were “HP Series 700” (stock HP-UX), “C Series” and “MPP” applications

3.48.5 Benchmarks

System	Processor	SPEC92 fp	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
Convex SPP1000	2-CPU PA-7100 100 MHz		3.27	3.98		
Convex SPP1200	2-CPU PA-7200 120 MHz	185				

Convex SPP1600	8-CPU PA-7200 120 MHz 16-CPU PA-7200 120 MHz 32-CPU PA-7200 120 MHz				290 541 996	383 744 1444
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Comparison to SPEC benchmark data from other Unix workstations and servers:

Table 3.166: Based on old SPEC95rate archives

System	Processor	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
DG AViiON AV 20000	16-CPU Pentium Pro 200 MHz			1007	
DEC Al- phaServer 8400 5/300	12-CPU 21164 300 MHz	33 (8P)		767	919
Siemens RM600 720	24-CPU R4400 250 MHz			921	
HP 9000 D380	2-CPU PA-8000 180 MHz	12	17	210	221
HP 9000 K580	6-CPU PA-8200 240 MHz	17 (1P)	28 (1P)	902	849
Convex SPP20000	8-CPU PA-8000 180 MHz 16-CPU PA-8000 180 MHz			713 1307	935 1413
HP 9000 T600	12-CPU PA-8000 180 MHz	12	15	1192	1151
HP Visualize C3600	1-CPU PA-8600 552 MHz	42	64	379	576

3.48.6 Dimensions

System	Height	Width	Depth	Weight
SPP1200/XA	71cm	112cm	178cm	404kg
SPP1200/CD	46cm	99cm	89cm	159kg

3.48.7 Documentation

Manuals

- ◇ *SPP1200/CD Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation) (URL gone)
- ◇ *SPP1200/XA Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation) (URL gone)

Articles

- ◇ A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a mirrored PDF version from citeseer (accessed August 2008)])
- ◇ Characterizing Shared Memory and Communication Performance: A Case Study of the Convex SPP-1000 (Postscript) Gheith A. Abandah and Edward S. Davidson (January 1996: University of Michigan. Accessed August 2008)
- ◇ An Empirical Evaluation of the Convex SPP-1000 Hierarchical Shared Memory System (PDF) Thomas Sterling, et al. (1995: Proceedings of the IFIP WG10.3 working conference on Parallel architectures and compilation techniques. Citeseer mirror accessed April 2009)
- ◇ Exemplar 1200 Architecture presentation (FTP, Postscript) Beth Richardson? (N.d.: NCSA. Google archive accessed August 2008)
- ◇ Convex Division Data Sheets, Hewlett-Packard Company (1996: mirror accessed January 2024)

3.49 HP Convex SPP2000 S-Class, X-Class

The Convex Exemplar SPP2000 and SP2200 are large scalable PA-RISC servers based on Convex Exemplar technology, integrated into HP's lineup after the acquisition of Convex. They were called **S-Class** and **X-Class** by HP and are the predecessors of the later HP 9000 V-Class V2200 and V2500 servers.

Originally developed based on the Convex Exemplar SPP1000, the SPP2000 and later S-Class use a similar crossbar architecture. This crossbar uses central internal “switching” to connect resources to each other by forming matrix connections between input and output ports. A SPP2000 can hold up to sixteen 64-bit PA-8000 processors with 16 GB memory in a single *Node*, called *S-Class*.

SPP2000s can form large-scale systems by connecting single nodes with SCI links into larger clusters of up to 32 nodes and 512 processors. The resulting system is called *X-Class*, ccNUMA computers. The clustering capabilities of their successors, the V2500, were reduced significantly—in contrast to the 32-node maximum of SPP2000 clusters, V2500s only can be clustered into groups of four.

SPP2000/S-Class were operated and controlled via so-called “teststations,” Unix workstations that connect to a central management board in single nodes which provides booting, system monitoring and diagnostics and console. Teststations were either IBM RS/6000 AIX systems or more commonly HP 9000 workstation running HP-UX.

- ◇ SPP2000 S-Class were introduced in 1997, with 4 CPUs for \$189,000
- ◇ SPP2000 X-Class were introduced in 1997, with 16 CPUs for \$720,000
- ◇ SPP2000 X-Class were introduced in 1997, with 64 CPUs for \$3 million

3.49.1 System architecture

Processors

System	Type		CPU	Speed	L1 Cache
SPP2000 S-Class	Node	4-16	PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
SPP2000 X-Class	Cluster/Wall	32-512	PA-8000 PA-RISC 64-bit	180 MHz	1/1 MB off-chip
SPP2200 X-Class	Cluster/Wall	32-512	PA-8200 PA-RISC 64-bit	200 MHz	1/1 MB off-chip

Chipset

SPP2000 are based on Exemplar crossbar architecture which connects CPU and I/O to system main memory.

- ◇ **8x8 nonblocking crossbar**, the central part of an Exemplar, connects memory to processor buses and I/O channels. Eight ports for agents connect to each two CPUs and one I/O channel, and eight ports for memory. Each port has 64-bit 960 MB/s bandwidth, combined 15.3 GB/s for the crossbar, built in CMOS with 1.1M transistors (GaA in SPP1X00 Exemplar).
- ◇ **Eight Data Mover/Agents** attach to the crossbar and provide access for the processors with Runway buses and I/O controllers to the memory via the crossbar over a 1.9 GB/s datapath with four 32-bit, unidirectional buses from two ports on the Agent connect to two crossbar ports. The I/O channels on the agent have a maximum bandwidth of 240 MB/s. Each Agent has two Runway processors buses with an aggregate bandwidth of 960 MB/s.

- ◇ **Eight PCI controller** connect 240 MB/s I/O channels/PCI buses to agents.
- ◇ **Eight Memory controllers** attach each one four-way interleaved memory board to the Hyperplane crossbar. Each memory controller has a bandwidth of 1.9 GB/s.

System buses

- ◇ Total crossbar bandwidth 15.3 GB/s (intra-crossbar)
- ◇ CPU bandwidth 7.5 GB/s (CPU-to-Agent, eight Runway 960 MB/s buses)
- ◇ Memory bandwidth 15 GB/s (memory-to-crossbar, sixteen 960 MB/s links)
- ◇ I/O bandwidth 1.9 GB/s (eight 240 MB/s channels, I/O channel-to-Agent)
- ◇ Eight PCI-32 I/O buses for expansion slots (each 240 MB/s)
- ◇ Attachments to SCI rings/CTI (“Coherent Toroidal Interconnect”) via two rings (X-ring and Y-ring), Node-to-Node bandwidth of 3.84 GB/s, the rings operate at a clock of 120 MHz with a width of 32 bit
- ◇ SCSI-2 Ultra main storage I/O bus

Memory

- ◇ SDRAM DIMMs
- ◇ Two to eight memory boards per node
- ◇ Memory is up to four-way interleaved per memory board and up to 32-way interleaved per node
- ◇ SPP2000 Node/S-Class: 1 GB minimum, 16 GB maximum
- ◇ SPP2000 Wall/X-Class: 512 GB maximum (with 32 nodes)

Expansion slots

- ◇ 24 PCI 32-bit slots on eight PCI 32-bit channels

Storage

- ◇ 20 internal Ultra SCSI drives

3.49.2 Clustering

Multiple Exemplar SPP2000/HP S-Class systems can be connected together to form a single large system, a “Wall” /X-Class.

- ◇ Up to 32 single nodes can be clustered together to form a system with up to
 - 512 processors
 - 512 GB of RAM

- 768 PCI slots
- 640 SCSI drives
- ◇ Clustered SPP2000s/X-Class are ccNUMA computers; they are not fully conformant to the PA-RISC 2.0 specification (and thus do not run standard HP-UX).
- ◇ Multiple systems are connected via two CTI rings: these links attach to the eight memory controllers of a node. A single system attaches to other single “nodes” and their respective crossbars with a node-to-node data rate of 3.8 GB/s.
- ◇ The two rings are called X-ring and Y-ring.
- ◇ The links are implementations of the IEEE *SCI* from Convex — Convex Toroidal Interconnect.
- ◇ Each node’s main memory is globally accessible from other nodes on the CTI network (that is, local memory is globally shared).
- ◇ A part of each system’s main memory is reserved for cache memory for the CTI network (configured statically at boot time).

3.49.3 External ports

- ◇ 68-pin VHDCI Ultra LVD external SCSI
- ◇ Three serial RS232C DB9 (local console, remote console, general purpose) via a DB25 “M cable”
- ◇ 10/100 Mbit Ethernet TP/RJ45
- ◇ 10/100 Mbit Ethernet TP/RJ45 *LAN console*

3.49.4 Operating systems

The Exemplar Operating System, SPP-UX, was a scalable Unix based on Mach developed by Convex for its SPP1000 and SPP2000 mainframe computers with up to 128 or 512 processors, released between 1993 and 1999. SPP-UX implemented a distributed architecture that was supposed to look like (emulate) HP-UX for developers but was very different below the userland.

SPP-UX kernel and architecture were based on a Mach 3.0 distributed microkernel and was taken over by HP during the acquisition of Convex and its Exemplar SPP computers. Each hypernode of the SPP computers ran an independent instance of the Mach microkernel.

There were three (four) main layers for SPP-UX:

1. **Distributed kernel:** Based on an enhanced Mach 3.0 microkernel, supposedly OSF 1/AD Mach from OSF RI, that was targeted for coupled SMP systems to support highly parallel applications; message-passing paradigm for NUMA computers
2. **HP-UX compatibility:** Second operating system layer compatible to HP-UX, to enable running HP-UX applications on SPP-UX, supposedly emulated HP-UX APIs and ABIs; management of distributed resources, processors, simultaneous users, process scheduler; supported parallel jobs as well as multiprocessing of single-thread
3. **Extensions and features:** Central management, open systems and standards like POSIX, specialized programming and development environment
4. Lastly, the **applications:** Possible were “HP Series 700” (stock HP-UX), “C Series” and “MPP” applications

3.49.5 Benchmarks

System	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
SPP2000/S-Class/X-Class	11.8	18.7	92.5 2-CPU: 183 4-CPU: 363 6-CPU: 539 8-CPU: 713 10-CPU: 867 12-CPU: 1012 16-CPU: 1307	141 2-CPU: 276 4-CPU: 524 6-CPU: 739 8-CPU: 935 10-CPU: 1085 12-CPU: 1220 16-CPU: 1413

Comparison to SPEC benchmark data from other Unix workstations and servers:

Table 3.170: Based on old SPEC95rate archives

System	Processor	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
DG AViON AV 20000	16-CPU Pentium Pro 200 MHz			1007	
DEC AlphaServer 8400 5/300	12-CPU 21164 300 MHz	33 (8P)		767	919
Siemens RM600 720	24-CPU R4400 250 MHz			921	
HP 9000 D380	2-CPU PA-8000 180 MHz	12	17	210	221
HP 9000 K580	6-CPU PA-8200 240 MHz	17 (1P)	28 (1P)	902	849
HP 9000 T600	12-CPU PA-8000 180 MHz	12	15	1192	1151
Convex SPP1600	8-CPU PA-7200 120 MHz 16-CPU PA-7200 120 MHz 32-CPU PA-7200 120 MHz			290 541 996	383 744 1444
HP Visualize C3600	1-CPU PA-8600 552 MHz	42	64	379	576

3.49.6 Dimensions

Height	Width	Depth	Weight
736mm	914mm	889mm	250kg

3.49.7 Documentation

Articles

- ◇ Exemplar System Architecture Hewlett-Packard/Convex (Januar 1997, access August 2008)

- ◇ SPP 2000 Architecture presentation (FTP, Postscript) Beth Richardson (N.d.: NCSA. Google archive accessed August 2008)
- ◇ A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a mirrored PDF version from citeseer (accessed August 2008)])

3.50 HP 9000 T500, T520, T600 and 890

HP 9000 T-Class were PA-RISC “high-end, datacenter-class servers” from the early 1990s, multi-processors built with modular system cards for processors, memory or I/O devices. Part of the HP 9000 800 server range, 890, T500 and T520 used 32-bit PA-RISC processors, later T600 moved on to 64-bit PA-RISC 2.0.

HP marketed T-Class as “Corporate Business Servers” that were the “most capable and expandable UNIX-based systems” with “high-end performance scalability” to meet growing business needs. Designed for business Unix applications and the corporate processing market of the 1990s, T-Class had massive expansion options for an Unix server of the time with I/O and communications cards.

T500, T520, T600 and 890 share a similar system architecture with differences in specific processors and options. The main system backplane has sixteen slots, eight of which can be used for memory or processor boards and the other eight for I/O boards and converters. These boards plug into the main system VSC bus.

HP 9000/890 were an earlier iteration of the mainframe architecture, based on 1980s HP 9000 870 servers and apparently PA-RISC 1.0 PCX CPUs. Later T500/T600 were updated successors with newer technology and hardware. After the 64-bit T600, HP discontinued the T-Class design for mainframes in favor of the more flexible Cell-based Superdome systems. Apparently 890 and T500 were board-upgradable to T520, with another board-upgrade path to PA-8000 processors as well.

- ◇ HP 9000 890 were introduced in 1992 for \$340,000
- ◇ HP 9000 T500, HP 9000/891 were introduced in 1993 for \$165,000 (uni) and \$660,000 12-way
- ◇ HP 9000 T520, HP 9000/892 were introduced in 1995 for \$145,000 (uni) and \$520,000 14-way
- ◇ HP 9000 T600, HP 9000/893 were introduced in 1997

3.50.1 System architecture

Processors

Table 3.172: The 890 CPU is probably PCX, some sources indicate PA-7000. Off-chip caches are generally pretty large, especially on 890 T600 is apparently the only system with PA-8000 processor with L2 cache, not mentioned in the PA-8000 documentation

System	CPU	Speed	L1 cache	L2 cache
HP 9000 890	1-4 PCX PA-RISC 32-bit	60 MHz	4 MB off-chip ²	
HP 9000 T500	1-12 PA-7100 PA-RISC 32-bit	90 MHz	2 MB off-chip	
HP 9000 T520	1-14 PA-7150 PA-RISC 32-bit	120 MHz	2 MB off-chip	
HP 9000 T600	1-12 PA-8000 PA-RISC 64-bit	180 MHz	2 MB off-chip	8 MB off-chip L2 ³

Architecture

Separate processor cards attach processors and support chips to main system bus. There are slots for processors, memory and I/O cards. HP 9000 890 and T-Class have slightly different architecture.

HP 9000 890

- ◇ Processor cards contain eight VLSI CMOS chips with the main processor and cache chips
 1. PCX PA-RISC 1.0 processor
 2. Cache chips ICMUX, DCMUX₀ and DCMUX₁ for 2 MB Instruction and 2 MB Data cache, ECC
 3. Floating point processor FPC, MUL and ADD
 4. Viper system bus VSC interface
- ◇ Up to four processor cards per system

HP 9000 T500, T520 and T600

- ◇ Processor cards contain each up to two processor modules with the actual CPUs
- ◇ Up to six cards in T500/T600 or seven in T520 per system
- ◇ Processor card chips:
 1. Two Viper system bus VSC interface
 2. Bus support chips
 3. T600 4 MB L2 I cache and 4 MB L2 D cache, each two modules
- ◇ Processor module chips:
 1. T520/T500PA-7100 PA-RISC 1.1 processor
 2. T600PA-8000 PA-RISC 1.1 processor
 3. 1 MB L1 I cache
 4. 1 MB L1 D cache

Chipset

Chipsets in T-Class and 890 depends on I/O cards and ordered options.

- ◇ HP Viper processor to system bus interface, integrated on processor cards
- ◇ HP-PB to VSC bus converter, integrated on the HP-PB interface cards
- ◇ Common HP-PB plug-in cards:
 - Fast/Wide SCSI
 - MUX
 - LAN/console
 - HP-FL fiber link interface
- ◇ T600 HP-HSC I/O Bus Converter
- ◇ Service processor, controls all hardware and power of the system, integrated into a single-board located in the main cardcage

System buses

- ◇ PBus processor/memory bus, 60 MHz, 32-bit data path between single CPUs and their Viper main bus interfaces, that means one PBus per processor card on 890 servers, two PBus per card on all others, 240 MB/s each
- ◇ VSC central system bus, 60 MHz clock
 - 890: 32-bit wide with 240 MB/s data rate
 - T500/T520: 64-bit wide with 480 MB/s data rate
 - T600: 128-bit wide with 960 MB/s data rate
- ◇ PBus and VSC are configured for PBus Variant 2 “Scalable MP” multiprocessing attachment
- ◇ T600Runway CPU/memory bus, although not mentioned in documentation
- ◇ T600GSC+ expansion bus in HSC variant
- ◇ HP-PB for “up to 168 high-speed HP Precision Bus I/O channels with 1 GB/s throughput”
- ◇ SCSI depends on installed I/O cards

Memory

- ◇ Memory cards, in sizes of 64-768 MB, not all systems support all cards
- ◇ Up to eight cards in PMB card slots 1-14
- ◇ Memory attaches to shared VSC system bus, 64-bit data path, and 128-bit data path on T600
- ◇ Cards operate at VSC bus frequency and have on-card interfaces to VSC bus
- ◇ 890 up to 2 GB main memory
- ◇ T500/T520 up to 3.75 GB main memory
- ◇ T600 apparently up to 16 GB main memory

Expansion slots

- ◇ T600 24 HSC/GSC+ slots, depends on HP-PB slot usage
- ◇ 14 HP-PB slots single-height — 7 double-height
- ◇ Up to 98 additional HP-PB slots can be added through “expansion cabinets”

Storage

- ◇ Drives located in external drive bays or racks
- ◇ T600 Marketed as up to 30TB with RAID arrays, huge amount for the time
- ◇ T500/T520 up to 20 TB with RAID

3.50.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ TP/RJ45 10BaseT 10Mbit Ethernet
- ◇ Two serial RS232C DB9, one for console, one for USV
- ◇ Parallel DB25
- ◇ Two PS/2 connectors for keyboard und mouse

3.50.3 Operating systems

HP 9000 890

- ◇ HP-UX 10.20 32-bit (possibly unsupported)
- ◇ HP-UX 10.00 and HP-UX 10.10, pre-Y2K
- ◇ HP-UX 9 (9.00, 9.02, 9.04, 9.06), pre-Y2K

HP 9000 T-Class

- ◇ HP-UX 11i v1 in 32-bit or 64-bit mode
- ◇ HP-UX 11.00 in 32-bit or 64-bit mode
- ◇ HP-UX 10.20 32-bit
- ◇ HP-UX 10.00 and HP-UX 10.10, pre-Y2K
- ◇ HP-UX 9, pre-Y2K, unsure

3.50.4 Benchmarks

System	SPEC92 rate int	SPEC92 rate fp	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
HP 9000 890	1-CPU: 1215 2-CPU: 2253 3-CPU: 3306 4-CPU: 4301	1-CPU: 1180 2-CPU: 2360 3-CPU: 3529 4-CPU: 4685				
HP 9000 T520			5.2		1-CPU: 47 2-CPU: 93 4-CPU: 186 8-CPU: 363 12-CPU: 531	
HP 9000 T600			11.8	14.9	1-CPU: 106 2-CPU: 211 4-CPU: 418 6-CPU: 617 8-CPU: 814 10-CPU: 1003 12-CPU: 1192	1-CPU: 134 2-CPU: 263 4-CPU: 510 6-CPU: 735 8-CPU: 915 10-CPU: 1043 12-CPU: 1151

Comparison to SPEC benchmark data from other Unix workstations and servers:

Table 3.174: Based on old SPEC95rate archives

System	Processor	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
DG AViiON AV 20000	16-CPU Pentium Pro 200 MHz			1007	
DEC AlphaServer 8400 5/300	12-CPU 21164 300 MHz	33 (8P)		767	919
Siemens RM600 720	24-CPU R4400 250 MHz			921	
HP 9000 D380	2-CPU PA-8000 180 MHz	12	17	210	221
HP 9000 K580	6-CPU PA-8200 240 MHz	17 (1P)	28 (1P)	902	849
Convex SPP1600	8-CPU PA-7200 120 MHz 16-CPU PA-7200 120 MHz 32-CPU PA-7200 120 MHz			290 541 996	383 744 1444
Convex SPP20000	8-CPU PA-8000 180 MHz 16-CPU PA-8000 180 MHz			713 1307	935 1413
HP Visualize C3600	1-CPU PA-8600 552 MHz	42	64	379	576

3.50.5 Dimensions

Height	Width	Depth	Weight
1620mm	750mm	905mm	360kg

3.50.6 Documentation

Manuals

- ◇ CE Handbook HP 3000 99x Family, HP T-Class Family (URL gone)
- ◇ Operators Guide T-Class HP 3000 99x Family Systems, HP 9000 Enterprise Servers (1997: Hewlett-Packard, A1809-96019) **3kranger**
- ◇ Installation Guide T-Class HP 3000 99x Family, HP 9000 Systems (1999: Hewlett-Packard, A1809-90001) **3kranger**
- ◇ Operator's Guide HP 3000 99x Family, HP 9000 T-Class Systems (June 1997: Hewlett-Packard, A1809-90009)

Articles

- ◇ Corporate Business Servers: An Alternative to Mainframes for Business Computing (.pdf) Thomas B. Alexander et al (June 1994: Hewlett-Packard Journal)

- ◇ HEWLETT-PACKARD MOVES T-CLASS SERVERS UP TO PA-7150 RISCs, Computer Business Review September 1995
- ◇ *Multiprocessor features of the HP Corporate Business Servers*, K. Chan et al., Comcon 93
- ◇ HP T-Class Corporate Business Servers HP Computer Buyer's Guide , Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ *Implementing HP 9000-890 Platforms: A Case Study*, Portland Community College, INTEREX 1993, Paper #4032

3.51 HP 9000 V2200 and V2250

HP 9000 V2250 and V2250 are large-scale scalable PA-RISC servers, with up to sixteen 64-bit PA-RISC processors in a single cabinet. The architecture is a direct continuation from the Convex *Exemplar*. V2200 and V2250 use HP's own HyperPlane crossbar chipset, consisting of four central crossbar ASICs and various other chipset components to attach memory, processors and I/O.

V2200/V2250 use a very similar crossbar-based system design to 64-bit SPP2000 S-Class/X-Class, minus the SCI/TCI links for interconnecting several nodes into a larger system. Their V2500/V2600 successors were delivered again with interconnection technology.

V2200 and V2250 are controlled via so-called "teststations" with its own HP-UX operating system to control and monitor V-Class servers. This teststation is a standard HP 9000/712 workstation with special teststation hardware such as a second ethernet and serial boards and software. The teststation connects to the Core Utilities Board (CUB), which provides booting, system monitoring and diagnostics, and console connections via one LAN and one special serial link.

- ◇ HP 9000 V2200 were introduced in 1997 for \$157,000
- ◇ HP 9000 V2250 were introduced in 1998

3.51.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 V2200	4-16 PA-8200 PA-RISC 64-bit	200 MHz	2/2 MB off-chip
HP 9000 V2250	4-16 PA-8200 PA-RISC 64-bit	240 MHz	2/2 MB off-chip

Chipset

1. **HP HyperPlane 8x8 crossbar**, non-blocking, four Exemplar Routing Attachment controllers (ERACs), the central part of the system connects memory to processor buses and I/O channels. Eight ports for CPUs and I/O agents, each connects to two or four CPUs and one I/O channel, and eight ports for memory.
2. Eight **Exemplar Processor Agent controllers** (EPACs) attach processors to the crossbar and provide access for each two processors Runway buses and one I/O controller to memory via the crossbar. Each EPAC communicates with two ERACs.
3. Eight **Exemplar PCI-bus Interface controller** (EPICs) connect I/O channels and PCI buses to the EPACs.
4. Eight **Exemplar Memory Access controllers** (EMACs) attach each an interleaved memory board to the Hyperplane crossbar.
5. **Exemplar Core Utilities board** (ECUB) provides interrupts and the central system logic, it connects to the Exemplar system Routing board ENRB. The Core Logic Bus from the ECUB attaches to the devices on the EPACs. Included on the ECUB are two custom FPGAs, the Exemplar Processor Utilities controller EPUC and the Exemplar Monitoring Utilities controller EMUC.

The remainder of the system I/O consist of standard HP PCI controllers:

- ◇ PCI Fast-wide FWD SCSI controller, high-voltage differential/HVD)

- ◇ PCI fibrechannel FC controller

System buses

- ◇ Total crossbar bandwidth 15.3 GB/s, intra-crossbar
 - Each crossbar port has a data path of 64-bit, giving it 960 MB/s peak bandwidth.
 - The peak bandwidth of the HyperPlane crossbar/ERACs is 15.3 GB/s combined.
- ◇ CPU bandwidth 7.5 GB/s, CPU-to-EPAC, eight Runway 960 MB/s buses
- ◇ Memory bandwidth 15 GB/s, memory-to-crossbar, sixteen 960 MB/s links
 - Each EMAC has a bandwidth of 1.9 GB/s for four 32-bit, unidirectional buses from two ports on the EMAC to two Hyperplane crossbar ERACs.
- ◇ I/O bandwidth 1.9 GB/s, eight 240 MB/s channels, I/O channel-to-EPAC
- ◇ Eight PCI-64/33 I/O buses for expansion slots, each 240 MB/s
- ◇ SCSI/storage buses depend on the installed SCSI adapter

Memory

- ◇ Two to eight memory boards, each memory board has 16 slots
- ◇ SDRAM DIMMs
- ◇ Memory is up to 32-way interleaved
- ◇ 16 GB maximum

Expansion slots

- ◇ 24 PCI 64-bit 33 MHz slots on eight PCI 64-bit channels

Storage

- ◇ 16 internal SCSI drives, exact type depending on installed SCSI adapter

3.5.1.2 External ports

- ◇ External SCSI connection
- ◇ Serial and two Ethernet for the console/Teststation

3.5.1.3 Operating systems

- ◇ HP-UX: 11.00 and 11i v1 (v1)

3.51.4 Benchmarks

System	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
V2200	13.8	16-CPU: 22.1	1-CPU: 125 4-CPU: 484 8-CPU: 964 12-CPU: 1442 16-CPU: 1865	1-CPU: 4-CPU: 755 8-CPU: 1380 12-CPU: 1909 16-CPU: 2312
V2250	16-CPU: 16.4	16-CPU: 24.8	16-CPU: 2209	16-CPU: 2471

Comparison to SPEC benchmark data from other Unix workstations and servers:

Table 3.178: Based on old SPEC95rate archives

System	Processor	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
DG AViiON AV 20000	16-CPU Pentium Pro 200 MHz			1007	
DEC Al- phaServer 8400 5/300	12-CPU 21164 300 MHz	33 (8P)		767	919
Siemens RM600 720	24-CPU R4400 250 MHz			921	
HP 9000 D380	2-CPU PA-8000 180 MHz	12	17	210	221
HP 9000 K580	6-CPU PA-8200 240 MHz	17 (1P)	28 (1P)	902	849
HP 9000 T600	12-CPU PA-8000 180 MHz	12	15	1192	1151
Convex SPP1600	8-CPU PA-7200 120 MHz 16-CPU PA-7200 120 MHz 32-CPU PA-7200 120 MHz			290 541 996	383 744 1444
Convex SPP20000	8-CPU PA-8000 180 MHz 16-CPU PA-8000 180 MHz			713 1307	935 1413
HP Visualize C3600	1-CPU PA-8600 552 MHz	42	64	379	576

3.51.5 Dimensions

Height	Width	Depth	Weight
1006mm	998mm	859mm	250kg

3.51.6 Documentation

- ◇ Site Preparation Guide: HP 9000 V-Class Server Hewlett-Packard Development Company (March 1998, second edition, A3725-96021) **parisc linux**
- ◇ Upgrade Guide HP V2200 to V2250 (PDF) Hewlett-Packard Company (March 1998, edition 1,

A5083-90001) **parisc linux**

- ◇ Architecture HP 9000 V-Class Server (PDF) Hewlett-Packard Company (March 1998, second edition, A3725-96022) **parisc linux**
- ◇ HP Exemplar Technical Servers, Hewlett-Packard Company (1997: mirror accessed January 2024)

3.52 HP 9000 V2500 and V2600

HP 9000 V2500 and V2600 are scalable PA-RISC V-Class servers based on Convex Exemplar architecture with up to 32 64-bit PA-RISC processors in a single cabinet. Up to four systems can be interconnected via CTI to form a combined system of up to 128 CPUs – a single computer to the operating system. Interconnected V2500s/V2500s are ccNUMA computers.

V-Class servers are based on a crossbar, a central internal switch that links computing resources to each other by forming matrix connections. V2500 and V2600 use HP HyperPlane chipset with four central ASICs and other components to attach memory, processors and I/O.

The architecture is a direct continuation of Convex *Exemplar*, used in HP Convex SPP1X00 and SPP2000 S-Class and X-Class in a similar crossbar design with GaA chips. This was upgraded for V-Class with faster processors and memory. A multi-node V2500/V2600 system architecture (SCA) does not conform fully to PA-RISC 2.0 reference architecture – the firmware layer emulates a reference-compliant PA-RISC system for the operating system. Several changes had to be made to the HP-UX kernel to accommodate the V-Class's special architecture.

V2500 and V2600 are controlled via a “teststation”, also called SSP, Service Support Processor, that runs its own operating system and controls and monitors the V-Class server, a HP 9000/712 or B180L workstation. The SSP/teststation connects to the Core Utilities Board (CUB) for booting, system monitoring and diagnostics, console connections, connected via one LAN and one special serial link.

- ◇ HP 9000 V2500 were introduced in 1998
- ◇ HP 9000 V2600 were introduced in 1999

3.52.1 System architecture

Processors

System	CPU	Speed	L1 cache
HP 9000 V2500	2-32 PA-8500 PA-RISC 64-bit	440 MHz	512/1024 KB on-chip
HP 9000 V2600	2-32 PA-8500 PA-RISC 64-bit	552 MHz	512/1024 KB on-chip

Chipset

1. **HP HyperPlane 8x8** crossbar, non-blocking, four Exemplar Routing Attachment controllers (ER-ACs), the central part of the system connects memory to processor buses and I/O channels. Eight ports for CPUs and I/O agents, each connects to two or four CPUs and one I/O channel, and eight ports for memory.
2. Eight **Processor Agent controllers** (PAC, also SPAC), attach processors to the crossbar and provide access for processor Runway buses and I/O controllers to the memory via the crossbar; each PAC communicates with two RACs.
3. Eight **PCI-bus Interface controller** (SAGA) connect I/O channels and PCI buses to the PACs.
4. Eight **Memory Access controllers** (MAC, also SMAC), attach an interleaved memory board to the Hyperplane crossbar.
5. The **Core Utilities board** (CUB) provides interrupts and the central system logic, it connects to the Midplane Interconnect Board MIB. The Core Logic Bus from the CUB attaches to the devices

on the PACs.

6. Eight **Toroidal Access Controller (STACs)** connect to a variation of the Scalable Coherent Interconnect SCI to one or two “rings.” The combination of STACs and SCI rings is referred to as Coherent Toroidal Interconnect CTI.

The remainder of the system I/O consist of standard HP PCI controllers, frequently shipped in default configuration with one of the following:

- ◇ PCI Fast-wide SCSI controller high-voltage differential/HVD
- ◇ PCI Ultra2-wide SCSI controller low-voltage differential/LVD
- ◇ PCI fibrechannel (FC) controller

System buses

- ◇ Total crossbar bandwidth 15.3 GB/s, intra-crossbar
 - Each crossbar port has a data path of 64-bit, giving it 960 MB/s peak bandwidth.
 - The peak bandwidth of the HyperPlane crossbar/ERACs is 15.3 GB/s combined.
- ◇ CPU bandwidth 7.5 GB/s, CPU-to-PAC, eight Runway 960 MB/s buses
- ◇ Memory bandwidth 15 GB/s, memory-to-crossbar, sixteen 960 MB/s links
 - Each EMAC has a bandwidth of 1.9 GB/s for four 32-bit, unidirectional buses from two ports on the EMAC to two Hyperplane crossbar ERACs.
- ◇ I/O bandwidth 1.9 GB/s, eight 240 MB/s channels, I/O channel-to-PAC
- ◇ PAC bandwidth, PAC-to-crossbar is also 15 GB/s theoretically, with sixteen 960 MB/s links for the eight PACs
- ◇ Eight PCI-64/33 I/O buses for expansion slots, each 240 MB/s
- ◇ Attachments to CTI/Scalable Computing Architecture SCA crossbar interconnection, 3.8 GB/s
- ◇ SCSI/storage buses depend on the installed SCSI adapter, most likely either Fast-wide or Ultra2-wide

Memory

- ◇ SDRAM DIMMs, 88-bit or 80-bit
- ◇ Two to eight memory boards
- ◇ Each memory board has 16 slots: four 4-slot “quadrants”
- ◇ Memory is up to 256-way interleaved
- ◇ 1 GB minimum
- ◇ 32 GB maximum

Expansion slots

- ◇ 28 PCI 64-bit 33 MHz slots on eight PCI 64-bit channels

Storage

- ◇ 16 internal SCSI drives, exact type depending on installed SCSI adapter

3.52.2 Clustering

Multiple V-Classes can be connected together to form a single large system resulting in a “SCA”, a scalable Computing Architecture system. Up to two four V2500/V2600s can be clustered together to form a system with up to 128 processors, 128 GB of RAM, 112 PCI slots and 64 SCSI drives. Clustered V-Classes are ccNUMA computers and do not conform fully to the PA-RISC 2.0 specification.

Multiple systems are connected via two CTI rings: these links attach via the STACs to the eight memory controllers. The two rings are called X-ring and Y-ring. Each system attaches to one or two other V2500/V2600 cabinets and their respective crossbars with a node-to-node data rate of 3.8 GB/s. The links are implementation of the IEEE SCI standard taken over from Convex — Coherent Toroidal Interconnect or Convex Toroidal Interconnect. Each node’s main memory is globally accessible from other nodes on the CTI network, that is, local memory is globally shared. 32-512 MB of each system’s main memory is reserved for cache memory for the CTI network configured statically at boot time.

3.52.3 External ports

- ◇ SCSI depends on installed adapter, either Ultra or Fast wide
- ◇ Serial and Ethernet connections of the teststation/SSP

3.52.4 Operating systems

- ◇ HP-UX: 11.00 and 11i v1 (v1)

3.52.5 Benchmarks

System	SPEC95 rate int	SPEC95rate fp
V2500	16-CPU: 400232-CPU: 7481	
V2600	16-CPU: 516432-CPU: 9315	

Comparison to SPEC benchmark data from other Unix workstations and servers:

Table 3.182: Based on old SPEC95rate archives

System	Processor	SPEC92 fp	SPEC95 int	SPEC95 fp	SPEC95 rate int	SPEC95 rate fp
DG AViiON AV 20000	16-CPU Pentium Pro 200 MHz				1007	

DEC Al-phaServer 8400 5/300	12-CPU 21164 300 MHz		33 (8P)		767	919
Siemens RM600 720	24-CPU R4400 250 MHz				921	
HP 9000 D380	2-CPU PA-8000 180 MHz		12	17	210	221
HP 9000 K580	6-CPU PA-8200 240 MHz		17 (1P)	28 (1P)	902	849
HP 9000 T600	12-CPU PA-8000 180 MHz		12	15	1192	1151
Convex SPP1600	8-CPU PA-7200 120 MHz 16-CPU PA-7200 120 MHz 32-CPU PA-7200 120 MHz			290 541 996	383 744 1444	
Convex SPP20000	8-CPU PA-8000 180 MHz 16-CPU PA-8000 180 MHz			713 1307	935 1413	
HP Visualize C3600	1-CPU PA-8600 552 MHz		42	64	379	576

3.5.2.6 Dimensions

Height	Width	Depth	Weight
990mm	800mm	940mm	223kg

3.5.2.7 Documentation

Manuals

- ◇ Operator's Guide HP 9000 V2500 Server (PDF) Hewlett-Packard Company (December 1998, first edition, A5075-90005) **parisc linux**
- ◇ Installation Guide HP 9000 V2500 Server (PDF) Hewlett-Packard Company (December 1998, first edition, A5075-90001) **parisc linux**
- ◇ Diagnostics Guide HP V2500/V2600 Servers (PDF) Hewlett-Packard Company (December 1999, first edition, A5824-96002) **parisc linux**
- ◇ Upgrade Guide HP V2500/V2600 Servers (PDF) Hewlett-Packard Company (December 1999, first edition, A5824-96004) **parisc linux**

Articles

- ◇ Architecture Reference Guide V2500 Server (PDF) Hewlett-Packard Company (June 1999, first edition, A5074-90004) **parisc linux**
- ◇ HP Scalable Computing Architecture Randy Wright and Arun Kumar (October 2000/ revised January 2002: USENIX, Proceedings of the First WIESS Workshop)

3.53 HP zx2000

HP zx2000 were Itanium workstations from HP, released in the early 2000s. They are close to PA-RISC C8000 workstations and build around the same HP zx1 chipset. zx2000 workstations are built in a sleek tower case, also available as rack-mount.

Shortly after releasing the zx2000, HP dropped Itanium *workstations* altogether from its portfolio and soon had no modern HP-UX Unix workstations anymore. All remaining HP-UX and Itanium offerings were IA64 server systems, the *Integrity rx*.

HP zx6000 Itanium workstations were based on HP zx2000 but were dual-processor capable.

- ◇ HP zx2000 were introduced in 2002
 - 900 MHz, SCSI, Radeon 7000, Linux sold for \$5,554
 - 900 MHz, IDE, Radeon 7000, HP-UX MTOE sold for \$5,865
 - 900 MHz, SCSI, Fire GL4, HP-UX MTOE sold for \$8,340

3.53.1 System architecture

Processors

Table 3.184: All caches are on-die (L1, L2 and L3).

System	CPU	Speed	L1 and L2 cache	L3 cache
HP zx2000	Itanium 2 <i>McKinley</i> VLIW 64-bit	900 MHz	16/16 KB + 256 KB	1.5 MB
HP zx2000	Itanium 2 <i>Madison</i> VLIW 64-bit	1.4 GHz	16/16 KB + 256 KB	1.5 MB
HP zx2000	Itanium 2 <i>Madison</i> VLIW 64-bit	1.4 GHz	16/16 KB + 256 KB	1.5 MB
HP zx2000	Itanium 2 <i>Madison</i> VLIW 64-bit	1.5 GHz	16/16 KB + 256 KB	1.5 MB
HP zx2000	Itanium 2 <i>Deerfield</i> VLIW 64-bit	1.0 GHz	16/16 KB + 256 KB	1.5 MB

Chipset

- ◇ HP zx1 chipset, original HP Itanium design based on two main components: MIO memory and I/O controller and IOA I/O adapters.
- ◇ Plutozx1 MIO is the main chipset controller and connects processor bus, two memory buses and seven I/O channels. Contains memory and cache controllers.
- ◇ Four *Mercury*zx1 IOAs connect PCI-X slots and I/O devices to the zx1 MIO on six I/O channels (3.0 GB/s)
- ◇ Gigabit Ethernet, Intel 82540
- ◇ Two-channel Ultra160 SCSI controller (optional)
- ◇ Ultra ATA-100 IDE controller, PCI649
- ◇ Graphics possibly through separate AGP boards:
 - *Optional* ATI FireGL4 (HP-UX)
 - *Optional* ATI FireGL X1 (HP-UX)

- *Optional* ATI FireGL Z1 (HP-UX)
- *Optional* nVIDIA Quadro4 900 XGL (Linux)
- *Optional* nVIDIA Quadro4 980 XGL (Linux)
- *Optional* nVIDIA Quadro2 EX (Linux)
- *Optional* ATI Radeon 7000 AGP (HP-UX and Linux)
- Other cards might or might not work
- ◇ PDH controller
- ◇ Serial controller, DUART 16550A-compatible
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard management controller, BMC—IPMI interface

System buses

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s
- ◇ zx1 memory bus, 200 MHz, 4.25 GB/s
- ◇ Six zx1 I/O channels/buses, aggregate 3.0 GB/s I/O bandwidth
 1. AGP 4x graphics bus on two channels: 1.0 GB/s
 2. PCI-X 64/133 I/O slot on two channels: 1.0 GB/s
 3. Four PCI-X 64/66 I/O slots on one channel: 0.5 GB/s
 4. Gigabit Ethernet, IDE, USB and audio controllers on PCI 32/33 on one channel: 0.5 GB/s
- ◇ AGP 4x graphics bus on two I/O channels, 1.0 GB/s aggregate
- ◇ PCI-X 64/133 I/O bus on two I/O channels, 1.0 GB/s aggregate
- ◇ PCI-X 64/66 I/O bus on one I/O channel, 0.5 GB/s aggregate
- ◇ PCI 32/33 I/O bus for onboard devices on one I/O channel, 0.5 GB/s aggregate
- ◇ SCSI-3 Ultra160 (LVD) storage I/O bus (if optional controller is installed)
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Takes up to 2 GB modules
- ◇ Four slots
- ◇ 512 MB minimum (2×256 MB)
- ◇ 8 GB maximum (4×2 GB)
- ◇ 4.25 GB/s memory bandwidth

Expansion slots

- ◇ One PCI-X 64-bit/133 MHz slot, full-length
- ◇ Three PCI-X 64-bit/66 MHz slots, full-length
- ◇ One PCI-X 64-bit/66 MHz slot, half-length
- ◇ All PCI slots are 3.3 V
- ◇ One AGP Pro 4x 32-bit slot, 1.5 V

Storage

- ◇ Up to two internal 3.5" bays for either Ultra ATA-100 IDE or Ultra160 SCSI hard drives
- ◇ Two half-height 5.25" bays for externally accessible Ultra ATA-100 IDE or SCSI (LVD or SE) drives (DVD/CD)

3.53.2 External ports

- ◇ TP/RJ45 Gigabit Ethernet
- ◇ Four USB 2.0 ports (two in front, two in rear)
- ◇ Two serial RS232C DB9
- ◇ Four phone jacks (microphone, line-in and line-out) on 16-bit audio card
- ◇ Optional IEEE-1394 Firewire ports

3.53.3 Operating systems

- ◇ HP-UX for Itanium 11i v1.6 and 11i v2
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ OpenVMS (officially unsupported on this platform)
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ Windows Server 2008 Itanium-based Editions
- ◇ Windows Server 2003 Itanium-based Editions

3.53.4 Dimensions

System	Height	Width	Depth	Weight
Tower	502mm	268mm	512mm	25kg
Rack-mounted	4U	482mm	510mm	20kg

3.53.5 Benchmarks

System	Processor	SPEC2000int	SPEC2000fp	SPEC2000rate int	SPEC2000rate fp
zx2000	McKinley 900 MHz	668	1086		12.6

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.187: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
Sun Ultra 40	AMD Opteron 256 3.0GHz	1957	
AMD	Opteron 250 2.4GHz	1619	1652
HP zx6000	Madison 1.5 GHz	1315	2106
Intel	Pentium 4 520 2.8GHz	1290	
HP ProLiant BL40p	Intel Xeon 2.8GHz	1249	1081
AMD	Athlon XP 2.2GHz	1080	873
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
HP Visualize C3750	PA-RISC PA-8700+ 875 MHz 2.2MB	678	674
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610

3.53.6 Documentation

- ◇ HP Workstation zx2000 - Technical Reference Guide, 5969-3154, HP: April 2003
- ◇ HP workstation zx2000 - data sheet, 5981-1463EN, HP: July 2002 (URL gone)

3.54 HP zx6000

HP zx6000 are dual-processor Itanium workstations from HP, released in 2002. The zx6000 were based on the zx2000 workstation with an HP zx1 Itanium architecture, also used in the zx2000 and PA-RISC servers. zx6000 were designed for rack-mounting (2U) with rails, with the optional tower kit it could be converted to a standalone unit. Rack-mounted rx2600 are closely related.

HP zx6000 have higher I/O and memory bandwidth and three times as much memory as earlier HP zx2000 workstations. HP zx6000 with fast CPUs were probably the fastest HP-UX workstations ever by HP. Both Itanium and Unix workstations were dropped by HP soon after releasing zx2000 and zx6000.

- ◇ HP zx6000 were introduced in 2002
 - entry, 900 MHz, Linux sold for \$10,520
 - dual 900 MHz, Fire GL4, HP-UX TCOE sold for \$14,160
 - dual 1 GHz, Quadro 2 EX, Linux sold for \$20,070

3.54.1 System architecture

Processors

Table 3.188: All caches are on-die (L1, L2 and L3).

System	CPU	Speed	L1 and L2 cache	L3 cache
HP zx6000	1-2 Itanium 2 <i>McKinley</i> VLIW 64-bit	900 MHz	16/16 KB + 256 KB	1.5 MB
HP zx6000	1-2 Itanium 2 <i>McKinley</i> VLIW 64-bit	1.0 GHz	16/16 KB + 256 KB	3.0 MB
HP zx6000	1-2 Itanium 2 <i>Madison</i> VLIW 64-bit	1.3 GHz	16/16 KB + 256 KB	3.0 MB
HP zx6000	1-2 Itanium 2 <i>Madison</i> VLIW 64-bit	1.5 GHz	16/16 KB + 256 KB	6.0 MB

Chipset

- ◇ HP zx1 chipset, on original HP Itanium design based on two main components—MIO, the memory and I/O controller, and IOAs, I/O adapters.
- ◇ HP Plutozx1 MIO, main chipset controller and connects processor bus, two memory buses and seven I/O channels. Contains memory and cache controllers.
- ◇ Six *Mercury*zx1 IOAs connect PCI-X slots and I/O devices to the zx1 MIO on seven I/O channels (3.5 GB/s)
- ◇ Gigabit Ethernet, Broadcom 5701
- ◇ Two-channel Ultra320 SCSI controller, LSI 1030
- ◇ Ultra ATA-100 IDE controller, PCI649
- ◇ Graphics through separate AGP boards:
 - *Optional* ATI FireGL4 (HP-UX)
 - *Optional* ATI FireGL X1 (HP-UX)
 - *Optional* ATI FireGL Z1 (HP-UX)

- *Optional* nVIDIA Quadro4 900 XGL (Linux)
- *Optional* nVIDIA Quadro4 980 XGL (Linux)
- *Optional* nVIDIA Quadro2 EX (Linux)
- *Optional* ATI Radeon 7000 AGP (HP-UX and Linux)
- Other cards might or might not work
- ◇ PDH controller
- ◇ Serial controller, DUART 16550A-compatible
- ◇ FPGA controller for ACPI (2.0) and LPC
- ◇ Baseboard management controller, BMC — IPMI interface
- ◇ 10/100 Ethernet for management, Intel 82550

System buses

- ◇ Itanium 2/zx1 processor bus 6.4 GB/s
- ◇ Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s, aggregate 8.5 GB/s
- ◇ Seven zx1 I/O channels/buses, aggregate 3.5 GB/s
 1. AGP 4x graphics bus on two channels: 1.0 GB/s
 2. PCI-X 64/133 I/O slot on one channel: 0.5 GB/s
 3. PCI-X 64/133 I/O slot on one channel: 0.5 GB/s
 4. PCI-X 64/133 I/O slot on one channel: 0.5 GB/s
 5. Gigabit Ethernet and Ultra320 SCSI on PCI 64/66 on one channel: 0.5 GB/s
 6. IDE, USB, management LAN on PCI 32/33 on one channel: 0.5 GB/s
- ◇ Three PCI-X 64/133 I/O buses
- ◇ PCI-X 64/66 I/O bus, for SCSI/Gigabit Ethernet onboard
- ◇ PCI 32/33 I/O bus, for IDE/USB/management onboard devices
- ◇ Two SCSI-3 Ultra320 (LVD) storage I/O buses
- ◇ AGP 4x graphics bus
- ◇ UltraATA-100 IDE storage I/O bus

Memory

- ◇ PC2100 registered ECC DDR266 SDRAM DIMMs
- ◇ Takes up to 2 GB modules
- ◇ Twelve slots
- ◇ 512 MB minimum (2×256 MB)

- ◇ 24 GB maximum (12×2 GB)
- ◇ 8.5 GB/s memory bandwidth

Expansion slots

- ◇ Three PCI-X 64-bit/133 MHz slots, full-length
- ◇ All PCI slots are 3.3 V
- ◇ One AGP Pro 4x 32-bit slot, 1.5 V for graphics

Storage

- ◇ Three internal 3.5" bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug
- ◇ Slimline bay for optional IDE CD or DVD drive
- ◇ Drive 1 and 2 are on one SCSI channel, drive 3 and the external connector on the second

3.54.2 External ports

- ◇ Gigabit Ethernet, TP/RJ45
- ◇ 10/100 Ethernet, TP/RJ45 BT management network
- ◇ Ultra320 SCSI 68-pin
- ◇ 25-pin serial for management processor card, needs break-out cable for 3 serial ports
- ◇ Four USB 2.0 ports
- ◇ Two serial RS232C DB9
- ◇ 16-bit stereo audio (optional)

3.54.3 Operating systems

- ◇ HP-UX Itanium 11.6 and 11i v2
- ◇ Linux for Itanium
- ◇ FreeBSD/ia64
- ◇ Windows Server 2008 Itanium-based Editions
- ◇ Windows Server 2003 Itanium-based Editions
- ◇ Windows XP 64-Bit Edition Version 2003
- ◇ OpenVMS (officially unsupported on this platform)

3.54.4 Dimensions

System	Height	Width	Depth	Weight
Tower	494mm	295mm	675mm	25kg
Rack-mounted	2U	483mm	679mm	22kg

3.54.5 Benchmarks

System	Processor	SPEC2000int	SPEC2000fp	SPEC2000rate int	SPEC2000rate fp
zx6000	McKinley 900 MHz	669	1139	7.8 2-CPU: 15.4	13.22-CPU: 23.9
zx6000	McKinley 1.0 GHz	807	1422		16.5 2-CPU: 30
zx6000	Madison 1.5 GHz	1315	2106	15.2 2-CPU: 30.4	24.42-CPU: 42.4

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.191: Based on old SPEC2000 archives

System	Processor	SPEC2000int	SPEC2000fp
Sun Ultra 40	AMD Opteron 256 3.0GHz	1957	
AMD	Opteron 250 2.4GHz	1619	1652
Intel	Pentium 4 520 2.8GHz	1290	
HP ProLiant BL40p	Intel Xeon 2.8GHz	1249	1081
AMD	Athlon XP 2.2GHz	1080	873
HP c8000	PA-8800 1.0 GHz	1001 (est.)	
HP AlphaServer ES80	Alpha 21364 1GHz	689	975
HP Visualize C3750	PA-RISC PA-8700+ 875 MHz 2.2MB	678	674
HP zx2000	McKinley 900 MHz	668	1086
IBM POWER 275	IBM POWER4+ 1GHz	617	862
Sun Fire 280R	UltraSPARC III Cu 1GHz	511	688
DELL Power Edge 4400	Pentium III Xeon 1 GHz	437	302
IBM RS/6000 M80	IBM RS64 IV 750MHz	409	359
HP i2000	Itanium Merced 800MHz 4MB	365	610

Compared to the competition at the time, Itanium computers were exceptionally strong in floating-point use cases, beating other CPUs in FP with more than twice the clock. Integer and general workloads were much weaker in Itanium, only barely beating PA-RISC, but a Madison 1.5 GHz much higher rated Intel and AMD processors.

3.54.6 Documentation

- ◇ Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000 (PDF) Hewlett-Packard 2007, 5991-5988
- ◇ HP Workstation zx6000 - data sheet, 5981-7454EN, HP: June 2003 (PDF URL gone)
- ◇ HP workstation zx6000 - data sheet, 5981-1464EN, HP: July 2002 (PDF URL gone)

3.55 RDI PrecisionBook

RDI PrecisionBooks are portable PA-RISC workstations, released by RDI in 1998, shortly before the takeover by Tadpole. They were based on HP 9000 C132L workstations in a portable case and marketed as “first HP-UX laptops.”

PrecisionBooks were used for “engineering, software development, network management, financial modeling, military command operations, and intelligence gathering.”

As RDI PrecisionBooks were technically based on C132L/C160Ls, they supported the same PA-RISC operating systems and applications. A major addition by RDI to the system logic was an integrated Cardbus controller for which Tadpole supplied drivers for HP-UX.

RDI PrecisionBooks apparently did not enjoy large commercial success but Tadpole reused the laptop design for other RISC laptops of the 1990s, for example the UltraSPARC-based Tadpole UltraBook that was slightly more successful.

In addition to the PrecisionBook, only two other portable PA-RISC computers were produced – the military-focused SAIC Galaxy 1100, based on HP 9000 712, and the Japanese Hitachi 3050RX100C laptop, based on Hitachi custom design.

There were a few other RISC Laptops in the 1990s, with a wide variety of processor architectures such as SPARC, PowerPC and even Alpha.

- ◇ RDI PrecisionBook 132 12”, HP 9000 779, were introduced in 1998 for \$11,995
- ◇ RDI PrecisionBook 160 14”, HP 9000 779, were introduced in 1998 for \$14,995
- ◇ RDI PrecisionBook 180 14”, HP 9000 779, were introduced in 1998

3.55.1 System architecture

Processors

Table 3.192: The external L2 cache was optional but was supplied with most systems

System	CPU	Speed	L1 Cache	L2 Cache
PrecisionBook 132	PA-7300LC	132 MHz	64/64 KB on-chip	1 MB off-chip optional
PrecisionBook 160	PA-7300LC	160 MHz	64/64 KB on-chip	1 MB off-chip optional
PrecisionBook 180	PA-7300LC	180 MHz	64/64 KB on-chip	1 MB off-chip optional

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Phantom PseudoBC GSC+ port
- ◇ HP Dino GSC-to-PCI bridge

- ◇ HP Visualize-EG (*Graffiti*) graphics with 2MB frame buffer memory
- ◇ 1 MB flash memory
- ◇ Two Cirrus CL-PD6832 PCI-CardBus bridges
- ◇ CMD PCI0643 IDE/UDMA33 controller

Display

- ◇ Integrated display, option of 12.1" (0.24mm dot pitch) or 14.1" (0.28mm dot pitch) active matrix LCD (the 14-inch version were most popular)
- ◇ XGA resolution (1024×768), 16M colors, 60Hz refresh
- ◇ External monitor output supports VGA, SVGA, XGA, SXGA and 1600×1200 resolutions at refresh rates of 60, 72 and 75Hz
- ◇ At XGA resolution the LCD and external monitor can be used at the same time, with different resolutions on the external monitor the LCD blanks

Input

- ◇ PS/2-compatible, 97-key keyboard
- ◇ Three-button trackpad

Energy

- ◇ Lithium-Ion battery with 40Wh capacity, 450g, 0.5-1 hours battery time
- ◇ Recharge time of 2.5 hours when powered off
- ◇ Laptop draws about 70W continuous
- ◇ AC adapter provides 19V (DC) 3.68A, non-standard pinout

System buses

- ◇ GSC-2 general system-level I/O bus
- ◇ PCI-32/33 device I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus disk I/O
- ◇ PDH bus, peripheral interface connecting to flash memory, NVRAM and PSM bus
- ◇ PSM bus, provides connection to the power-supply module

Memory

- ◇ Two sockets for 32-512 MB (2×256)
- ◇ Proprietary ECC modules, 32-256 MB modules, 60ns, 144-bit wide

Expansion slots

- ◇ Two Cardbus slots, for Cardbus and PCMCIA expansion cards

Storage

- ◇ Two 2.5" IDE hard drives with SCSI converter or 2.5" SCSI drives
- ◇ Since 2.5-inch SCSI drives are uncommon RDI used regular IDE notebook drives with a special IDE-SCSI converter from ADTX)

3.55.2 External ports

- ◇ SCSI-2 50-pin single-ended
- ◇ Ethernet RJ45
- ◇ VGA 15-pin Dsub graphics connector
- ◇ Two PS/2 connectors for keyboard/mouse
- ◇ Audio (microphone, headphones, line-in)
- ◇ 15-pin connector for external floppy
- ◇ High-pin-count connector for docking station
- ◇ Connector for an special I/O breakout cable to connect:
 - Two serial RS232C DB9
 - Parallel DB25
 - AUI 10Mbit Ethernet

3.55.3 Operating systems

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11i v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

Not all devices or expansion options and modules are supported in Linux and the BSDs. OpenBSD fully supports the Cardbus controller and a range of different Cardbus and PCMCIA devices (Fast-Ethernet, WLAN etc.).

3.55.4 Benchmarks

Table 3.193: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
PrecisionBook 132	PA-7300LC 132MHz	6.49	6.54
PrecisionBook 160	PA-7300LC 160MHz	7.78	7.39
PrecisionBook 180	PA-7300LC 180MHz	9.22	9.43

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.194: Based on old SPEC95 archives

System	CPU	SPEC95 int	SPEC95 fp
Tadpole UltraBookIli	Sun UltraSPARC Ili 400MHz	17.9	20.6
Siemens SCENIC 1000	Intel Pentium II 333MHz	13.0	9.43
SGI O2	MIPS R10000 196MHz	10.1	8.77
Intel Alder	Intel Pentium Pro 200MHz	8.09	6.75
Sun Ultra 2 1170	Sun UltraSPARC 167MHz	6.34	9.33
DEC Alphastation 255	DEC Alpha 21064A 233MHz	4.27	5.09
IBM RS/6000 Notebook 860	PowerPC 603e 166MHz	3.94	2.71

3.55.5 Documentation

- ◇ PrecisionBook Hardware Reference Guide, 1997, RDI
- ◇ PrecisionBook Hardware User Guide, 1997, RDI
- ◇ RDI HP-UX 10.20 Installation Guide, 1997, RDI
- ◇ PrecisionBook Technical White paper, Issue 1.2 2000, Tadpole
- ◇ PrecisionBook Technical White Paper (Tadpole RDI: August 1999, link gone)
- ◇ ADTX SCSI-IDE converters information from Michael Shalayeff (link gone)
- ◇ Workstations go mobile, CNET Jan. 26, 1998
- ◇ HP Professional, March 1998 page 12, hparchive.org archive
- ◇ CIO Magazine May 1998 page 72, google books
- ◇ RISC Laptops Archive with more information on the many RISC laptops of the 1990s

3.56 SAIC Galaxy 1100

SAIC Galaxy 1100 are portable PA-RISC workstations based on the HP 9000/712 workstation in a ruggedized case released in 1994. Galaxy 1100 portables are very rare, originally built by SAIC in the 1990s for military and intelligence applications.

HP was part of the US Navy TAC-4 program in the 1990s in which HP supplied PA-RISC workstations to the Navy for measurement and control. For environments where standard workstations were not robust enough, HP contracted SAIC to produce a ruggedized MIL-SPEC portable workstation for the Navy: the SAIC Galaxy 1100 based on HP 9000 712.

As these systems were produced under a military contract and sometimes used in classified environment only few became available to civilian world. Only two other portable PA-RISC computers were sold – the RDI PrecisionBook, based on HP Visualize C132L, and the Japanese Hitachi 3050RX100C laptop; the SAIC Galaxy was not directly sold outside of military contracts and only later became available publically through resellers.

A long article on SAIC Galaxy 1100 and their VUE environment by Cameron Kaiser from 2023 expands on the background and historic usage of Galaxy.

There were a few other RISC Laptops in the 1990s, with a wide variety of processor architectures such as SPARC, PowerPC and even Alpha.

- ◇ SAIC Galaxy 1000, HP 9000 712, were introduced in 1994
- ◇ SAIC Galaxy 1100, HP 9000 712, were introduced in 1994

3.56.1 System architecture

Processors

System	CPU	Speed	L1 Cache
Galaxy 1000	PA-7100LC	60 MHz	1 KB on-chip and 64 KB off-chip
Galaxy 1100	PA-7100LC	80 MHz	1 KB on-chip and 256 KB off-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Artist graphics, 8-bit, 1 MB VRAM (could be extended to 2)
- ◇ *Integrated* Other I/O (serial, parallel, floppy)
- ◇ PCMCIA controller

Display

- ◇ 10.4" active matrix LCD

- ◇ XGA resolution, *i.e.*, 1024×768
- ◇ 256 colors (8-bit color depth)
- ◇ 60Hz refresh

Human Input

- ◇ PS/2-compatible, 84-key integrated QWERTY keyboard with 12 function keys
- ◇ Trackball and three-button pad

System buses

- ◇ GSC system level I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus

Memory

- ◇ 72-pin ECC SIMMs, same as on standard HP 9000 712
- ◇ (Original documentation describes proprietary memory modules)
- ◇ 8-32 MB modules
- ◇ Four sockets
- ◇ 16 MB (2×8) minimum, 128 MB (4×32) maximum
- ◇ Memory has to be installed in pairs, starting from slot 0

Expansion slots

SAIC developed several specialized I/O devices for the Galaxy that attached to GIO/TSIO expansion slots. Industry-standard PCMCIA slots were available as well through a SAIC-specific extension board.

- ◇ Two PCMCIA slots, for either two Type I/II or one Type III PCMCIA card
- ◇ Proprietary SAIC modules for the standard GIO/TSIO slots

Storage

- ◇ One 3.5" Fast-Narrow 50-pin SCSI-2 hard drive
- ◇ One 3.5" 1.44 MB Floppy drive

3.56.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Serial RS232C DB9 (up to 115200 baud)
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ VGA HD15
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Three phone jacks (microphone, headphones and line-in)

3.56.3 Operating systems

Since Galaxy 1100 are technically “normal” PA-RISC workstations they support standard PA-RISC operating systems and software.

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 v1 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9.07 (possibly also 9.05), pre-Y2K
- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

3.56.4 Benchmarks

Table 3.196: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
Galaxy 1000	HP PA-7100LC 60MHz	67.0	85.3	2.08	2.66
Galaxy 1100	HP PA-7100LC 80MHz	99	122	3.12	3.55

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.197: Based on old SPEC92 and SPEC95 archives

Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2	3.11	3.10
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2	4.04	2.35
SGI Indy	MIPS R4400SC 75MHz	88.1	96.6		

IBM RS/6000 Notebook 860	PowerPC 603e 166MHz			3.94	2.71
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		
Tadpole SPARCbook 3	Sun MicroSPARC 50MHz	26.4	21.0		

3.56.5 Dimensions

Height	Width	Depth	Weight
114mm	412mm	311mm	8kg

- ◇ Portable requirements: Navy TAC-4
- ◇ Shock: Federal Test Method Standard 101C, Method 5007.1 free-fall drop
- ◇ Airborne: MIL-STD-740-1, Grade C, Table 1

3.56.6 Documentation

- ◇ SAIC Galaxy 1100 product page, Old product page, Science Applications International Corporation (1996)
- ◇ RISCy BUSINESS presents the SAIC GALAXY 1100, Floodgap Systems, Cameron Kaiser (2020)
- ◇ SAIC Galaxy 1100: a pre-CDE VUE of the PA-RISC with a security clearance, Old VCR, January 2023
- ◇ RISC Laptops Archive with more information on the many RISC laptops of the 1990s
- ◇ HP/SAIC/HARRIS TEAM WINS \$672 MILLION U.S. NAVY TAC-4 CONTRACT, SAIC press release, Januar 1995

3.57 SAIC Talon

SAIC Talon are portable PA-RISC workstations based on HP 9000 712 workstations in a ruggedized case released in 1994. Talon portables are almost unknown today, originally built by SAIC in the 1990s for military and intelligence applications as part of the US Navy TAC-4 program.

HP supplied the US Navy in the 1990s in the TAC-4 program with PA-RISC workstations. For “severe” environments HP contracted SAIC to produce ruggedized MIL-SPEC workstations for the Navy: the SAIC Talon and Galaxy.

Both Talon and Galaxy were based on HP 9000 712 workstation design, with Talon seemingly even more ruggedized than Galaxy, painted in “Forest green, color 24052 per FED-STD-595.” Talon and Galaxy were produced under military contract and used in classified environments, so only few became available to civilian world. There is scant information available on SAIC Talon.

There were a few other RISC Laptops in the 1990s, with a wide variety of processor architectures such as SPARC, PowerPC and even Alpha.

- ◇ SAIC Talon, HP 9000 712, were possibly introduced in 1994

3.57.1 System architecture

Processors

System	CPU	Speed	LI Cache
Talon	PA-7100LC	60 MHz	1 KB on-chip and 64 KB off-chip

Chipset

- ◇ HP LASI integrated chipset
- ◇ *Integrated* NCR 53C710 8-bit single-ended SCSI-2
- ◇ *Integrated* Intel 82596CA 10 Mbit Ethernet controller
- ◇ *Integrated* HP Harmony CD/DAT quality 16-bit stereo audio
- ◇ HP Artist graphics, 8-bit, 1 MB VRAM (could be extended to 2)
- ◇ *Integrated* Other I/O (serial, parallel, floppy)
- ◇ PCMCIA controller, possibly from SAIC
- ◇ EISA controller, possibly HP Wax
- ◇ *Optional* EISA-VME bridge
- ◇ *Optional* Modem via PCMCIA

Display

- ◇ 10.4” active matrix LCD
- ◇ 1024×768 resolution

- ◇ “full-color”

Human Input

- ◇ 85-key integrated IBM-PC keyboard with 12 function keys
- ◇ Three-button “Force” pad

System buses

- ◇ GSC system level I/O bus
- ◇ SCSI-2 Fast-Narrow single-ended bus
- ◇ EISA additional expansion I/O bus
- ◇ *Optional* VME

Memory

- ◇ Possibly: 72-pin ECC SIMMs, same as on standard HP 9000 712
- ◇ 8-32 MB modules
- ◇ Four sockets
- ◇ 16 MB (2×8) minimum, 128 MB (4×32) maximum
- ◇ Memory has to be installed in pairs, starting from slot 0

Expansion slots

SAIC provided a 14.4k modem for the PCMCIA slot, which are labelled optional in documentation. It is unclear what happened to the standard GSIO/TSIO slots on stock 712 mainboards. It is also unclear how the EISA expansion was added to the system, and how the VME connects to it.

- ◇ *Optional* Two PCMCIA slots, for Type I/II or III
- ◇ EISA card slot
- ◇ *Optional* VME through EISA-to-VME extender

Storage

- ◇ One 3.5” Fast-Narrow 50-pin SCSI-2 hard drive
- ◇ One 3.5” 1.44 MB Floppy drive

3.57.2 External ports

- ◇ SCSI-2 50-pin Fast-Narrow single-ended
- ◇ Serial RS232C DB9 (up to 115200 baud)
- ◇ Parallel DB25
- ◇ Ethernet RJ45
- ◇ Ethernet AUI 15-pin
- ◇ VGA HD15
- ◇ Two PS/2 connectors for keyboard & mouse
- ◇ Three phone jacks (microphone, headphones and line-in)
- ◇ *Optional* Modem

3.57.3 Operating systems

Talons are possibly “normal” PA-RISC workstations and should support standard PA-RISC operating systems and software.

- ◇ HP-UX, the original HP Unix shipped with it
 - HP-UX 11.11 in 32-bit mode, TCOE and MTOE versions
 - HP-UX 11.00 in 32-bit mode
 - HP-UX 10.20 32-bit
 - HP-UX 10.00 and HP-UX 10.10, pre-Y2K
 - HP-UX 9.07 (possibly also 9.05), pre-Y2K
- ◇ NeXTSTEP, Mach-based Unix with beautiful GUI, PA-RISC in version 3.3
- ◇ PA-RISC Linux, main Linux port to PA-RISC, supported by HP in the 2000s
- ◇ OpenBSD, open-source Unix-like, ported to PA-RISC
- ◇ NetBSD, open-source Unix-like, ported to PA-RISC

3.57.4 Dimensions

Height	Width	Depth	Weight
190mm	508mm	406mm	18kg

Environmental requirements

- ◇ Portable requirements: Navy TAC-4
- ◇ Shock: three drops in transit case from height of 36”
- ◇ Airborne: operating 10,000 feet, MIL-STD-740-1, Grade C, Table 1
- ◇ Sand/Dust: Six hours blowing dust at 50Å C

- ◇ Rain: 1.8" rain per hour with 40mph wind for 40 minutes
- ◇ Salt Fog
- ◇ Fungus: "No growth"
- ◇ Immersion: "Closed transport configuration, 2 hours at depth of 1 meter in transit case"
- ◇ Solar Radiation: MIL-STD-810E
- ◇ Vibration: MIL-STD-167-1
- ◇ EMI: MIL-STD-461 surface ship and submarine

3.57.5 Benchmarks

Table 3.201: Based on old SPEC92 and SPEC95 archives

System	CPU	SPEC92 int	SPEC92 fp	SPEC95 int	SPEC95 fp
Talon	HP PA-7100LC 60MHz	67.0	85.3	2.08	2.66

Comparison to SPEC benchmark data from other contemporary Unix workstations:

Table 3.202: Based on old SPEC92 and SPEC95 archives

Sun SPARCstation 20	Sun SuperSPARC II 75MHz	125.8	121.2	3.11	3.10
Siemens PCE-5S	Intel Pentium 100MHz	96.2	81.2	4.04	2.35
SGI Indy	MIPS R4400SC 75MHz	88.1	96.6		
IBM RS/6000 Notebook 860	PowerPC 603e 166MHz			3.94	2.71
DEC AlphaStation 200	DEC Alpha 21064 100MHz	74.6	95.2	1.48	2.79
Sun SPARCstation 10	Sun SuperSPARC 40MHz	50.2	60.2	1.13	1.38
Digital DECstation 5000	MIPS R4000 50MHz	43.2	42.1		
Tadpole SPARCbook 3	Sun MicroSPARC 50MHz	26.4	21.0		

3.57.6 Documentation

- ◇ SAIC Talon product page, Science Applications International Corporation (1996)
- ◇ HP/SAIC/HARRIS TEAM WINS \$672 MILLION U.S. NAVY TAC-4 CONTRACT, SAIC press release, Januar 1995
- ◇ RISC Laptops Archive with more information on the many RISC laptops of the 1990s

3.58 Stratus Continuum

Thanks to Ti Kan (2004) for the input.

Stratus Technologies produced a line of “Ultra High Availability Fault Tolerant” PA-RISC servers, called Continuum, in the 1990s. Continuum were based on different PA-RISC processors and sold as Continuum 400, 600 and 1200 series between 1995 and 2004. These fault tolerant Stratus server feature a great deal of redundancy, with up to four CPUs to form one single logical processor.

Before PA-RISC, Stratus used different architectures – Stratus/32, XA400 and XA2000 from the 1980s used Motorola 68000s CPUs and Stratus XA/R from the early-1990s used Intel i860 processors, a RISC/VLIW design.

PA-RISC-powered Continuum were phased out by Stratus in the mid-2000s in favor of Intel-based systems, Xeon Pentium 4 ftServer V Series.

Table 3.203: Selected 1999 base prices

System	Processor	Year	Base price
Continuum 412	L1/P2 PA-7100 96MHz PA-RISC 32-bit	1996	\$66,000
Continuum 418	L1/P4 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$140,500
Continuum 428	L2/P8 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$240,500
Continuum 618	L1/P4 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$274,000
Continuum 628	L2/P8 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$424,000
Continuum 1218	L1/P4 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$499,000
Continuum 1228	L2/P8 PA-8000 180MHz PA-RISC 64-bit	1996-97	\$649,000

Prices are “only basic server configuration” from HP Professional in 1999.

3.58.1 Continuum 400

The Continuum 400 series has the same CPU/memory architecture as the 600/1200, but the I/O bus is different. Instead of a Golf bus, it has an X bus that connects each CPU/memory module to a pair of PCI bridge boards. All I/O connectivity is via PCI cards.

There are two PCI bays of 7 slots each, connected downstream from the PCI bridge boards. Each bay has a dual channel SCSI adapter on it as standard equipment. These are also cross-wired and dual-initiated much in the same way as the SCSI ports on the 600/1200 systems.

Continuum 400s were also typically shipped with a pair of Ethernet adapter cards. The PCI bridge boards also each contains a removable PCMCIA flash memory card. This is used as the boot device. FTX puts the bootloader as well as the UNIX kernel on there, whereas HP-UX only uses it for the bootloader.

The PCI bay doors control the power the the PCI slots. Once opened, all slots in that bay are powered off to facilitate removal and insertion of cards. The system continues to run on cards in the other bay. An interlock mechanism prevents both bay doors from being opened at the same time.

Two chassis versions were available, one a short form-factor AC-powered, the other a tall CO central office version with a choice of AC or DC power.

The Continuum 400 supported mainly Stratus-modified HP-UX as operating systems, with Stratus own FTX Unix only sold exceptionally.

3.58.2 Continuum 600 and 1200

The Continuum 600 and 1200 series are similar designs but with different chassis configuration. The 600 has six slots for the main Golf bus, and the rest of the space is filled with I/O card cages meant for secondary I/O boards. The 1200 has twelve slots for the main bus which occupies the entire width of the chassis. Secondary I/O boards go into a separate chassis.

Both models have space for two rows of cooling fans on the top, and two rows of disk drives on the bottom and also either a QIC or DAT tape drive or CDROM drive. The redundant power supplies with built-in UPS resides at the very bottom.

The main Golf bus is the main interconnect between the “big” boards:

- ◇ G7xx: CPU and memory boards
- ◇ K450: 4-channel HVD fast wide SCSI and Ethernet adapter
- ◇ K460: 4-channel HVD fast wide SCSI and Ethernet adapter
- ◇ K470: “carrier board” for PMC PCI-mezzanine daughter cards
- ◇ K600: Adapter to the secondary I/O card cages

On the 600 chassis, the six slots consists of two for the pair or CPU/memory boards, and four more slots for two pairs of “big” boards. On the 1200 chassis, there are slots for two pairs of CPU/memory boards and four pairs of big boards.

In addition the 600/1200 main chassis also has a pair of Console Controller cards which provides the RS232 console terminal and RSN modem connectivity. This controller also has a command mode that allows the operator to type commands on the console to reset the system, power down, power up, etc. It runs on “housekeeping power” that is independent of the rest of the system. The Console controller also contains some environmental monitoring circuitry that checks the chassis internal temperature and will increase the cooling fan speed if necessary.

The secondary I/O chassis can be used to plug in a wide array of I/O boards, all Stratus proprietary. These boards are also used on the XA/R line. FTX supported many of the communications boards like ISDN, serial, parallel, X.25, and all sorts of other comm boards. HP-UX did not support many of those, if any. VOS also supported disk and tape I/O through this.

Continuum 600 and 1200 were geared towards the VOS transactional operating system from Stratus, with FTX Unix offered only exceptionally.

3.58.3 Processors and architecture

Each logical processor is physically two pairs of actual CPUs, that means four physical CPU chips per single logical one. Each pair is located on a separate FRU. All processors run “lock-stepped,” they do exactly the same thing at the same time. Comparator logic between each two physical CPU pair monitors for discrepancies.

If any physical CPU glitches or does something different, the comparator logic will detect the error and take that pair of CPUs offline, while the system continues to run on the other pair. There is no “failover time.” On multi-processor boards, each FRU contains multiple pairs of the logical processor halves.

The memory is self-checking and ECC corrected. If an uncorrectable error occurs, the FRU in which the memory is located will also be taken offline.

The big I/O boards are also self-checking and contain a pair of everything. However, with the exception of the K600 they do not run lock-stepped to the twin FRU. For example on the K450/K460 boards, each of the SCSI host adapters is connected via the backplane into the same SCSI bus on the partner board, but each board's controller occupies a different SCSI target ID.

Only one controller is normally active, but when a failure occurs on the active board, all I/O is switched to the other controller. For the Ethernet ports on that board, they can be wired up to the same network or to different networks, and a software RNI redundant network interface layer provides transparent switching. All disks are mirrored.

3.58.4 System Table

Table 3.204: Stratus Continuum PA-RISC servers overview

System	CPU	Logical Physical	Cache per CPU	RAM max	Expansion max	Storage max	I/O max	OS
412	PA-7100 96 MHz	L1/P2	512 KB	2 GB	12 PCI	14 drives 4 CD-ROMs 4 tape	16 100Mbit 8 T1/E1 64 Async 64 RS232 32 X.21 32 V.35	HP-UX, FTX
415	PA-7100 96 MHz	L1/P2	2 MB	2 GB	12 PCI			HP-UX, FTX
418	PA-8000 180 MHz	L1/P4	2 MB	8 GB	12 PCI			HP-UX, FTX
419	PA-8500 360 MHz	L1/P4	1.5 MB	8 GB	12 PCI			HP-UX, FTX
422	PA-7100 96 MHz	L2/P4	512 KB	2 GB	12 PCI			HP-UX, FTX
425	PA-7100 96 MHz	L2/P4	2 MB	2 GB	12 PCI			HP-UX, FTX
428	PA-8000 180 MHz	L2/P8	2 MB	8 GB	12 PCI			HP-UX, FTX
429	PA-8500 360 MHz	L2/P8	1.5 MB	8 GB	12 PCI			HP-UX, FTX
439	PA-8600 480 MHz	L1/P4	1.5 MB	8 GB	12 PCI			HP-UX, FTX
449	PA-8600 480 MHz	L2/P8	1.5 MB	8 GB	12 PCI			HP-UX, FTX
610S	PA-7100 72 MHz	L1/P4	512 KB	128 MB	6 slots			VOS, FTX
610	PA-7100 72 MHz	L1/P4	512 KB	512 MB	6 slots			VOS, FTX
615S	PA-7100 96 MHz	L1/P4	2 MB	128 MB	6 slots			VOS, FTX
615	PA-7100 96 MHz	L1/P4	2 MB	1 GB	6 slots			VOS, FTX

616S	PA-8500 360 MHz	L1/P4	1.5 MB	0.5 GB	6 slots				VOS, FTX
616	PA-8500 360 MHz	L1/P4	1.5 MB	2 GB	6 PCI 2 Stratus 28 I/O	L47/P94 disks 4 tape	10 100Mbit 8 T1/E1 8 TR 4 FDDI 448 Async 112 RS232 28 X.21 56 V.35		VOS, FTX
618	PA-8000 180 MHz	L1/P4	2 MB	3 GB	6 slots				VOS, FTX
619	PA-8500 380 MHz	L1/P4	1.5 MB	4 GB	6 slots				VOS, FTX
620	PA-7100 72 MHz	L2/P8	512 KB	512 MB	6 slots				VOS, FTX
625	PA-7100 96 MHz	L2/P8	2 MB	2 GB	6 slots				VOS, FTX
628	PA-8000 180 MHz	L2/P8	2 MB	3 GB	6 slots				VOS, FTX
629	PA-8500 380 MHz	L2/P8	1.5 MB	4 GB	6 slots				VOS, FTX
651-2	PA-8600 480 MHz (552 MHz?)	L1/P4	1.5 MB	4 GB	6 PCI 2 Stratus 28 I/O	L47/P94 disks 4 tape	10 100Mbit 8 T1/E1 8 TR 4 FDDI 448 Async 112 RS232 28 X.21 56 V.35		VOS, FTX
652-2	PA-8600 480 MHz (552 MHz?)	L2/P8	1.5 MB	4 GB	6 PCI 2 Stratus 28 I/O				VOS, FTX
I210	PA-7100 72 MHz	L1/P4	512 KB	?	12 slots				VOS, FTX
I215	PA-7100 96 MHz	L1/P4	2 MB	?	12 slots				VOS, FTX
I218	PA-8000 180 MHz	L1/P4	2 MB	3 GB	12 slots				VOS, FTX

I219	PA-8500 380 MHz	L1/P4	1.5 MB	4 GB	12 slots			VOS, FTX
I220	PA-7100 72 MHz	L2/P8	512 KB	512 MB	12 slots			VOS, FTX
I225	PA-7100 96 MHz	L2/P8	2 MB	2 GB	12 slots			VOS, FTX
I228	PA-8000 180 MHz	L2/P8	2 MB	3 GB	12 slots			VOS, FTX
I229	PA-8500 380 MHz	L2/P8	1.5 MB	4 GB	12 slots			VOS, FTX
I245	PA-7100 96 MHz	L4/P16	2 MB	2 GB	12 slots			VOS, FTX
I251-2	PA-8600 480 MHz (552 MHz?)	L1/P4	1.5 MB	4 GB	18 PCI 6 Stratus 84 I/O	L95/P190 disks 4 tape	18 100Mbit 8 T1/E1 24 TR 8 FDDI 448 Async 112 RS232 84 X.21 168 V.35	VOS, FTX
I252-2	PA-8600 480 MHz (552 MHz?)	L2/P8	1.5 MB	4 GB	18 PCI 6 Stratus 84 I/O			VOS, FTX

- ◇ **Logical/Physical CPUs:** “L” and “P” denote *Logical* and *Physical* devices — logical CPUs are made up of two pairs of CPUs each (*i.e.*, 2×2)
- ◇ **Storage:** “L” and “P” denote *Logical* and *Physical* devices — logical disk drives are formed from physical devices via RAID sets
- ◇ **I/O:** Maximum number of I/O devices supported (not necessarily always configured with this number); notably the devices are also redundant

3.58.5 Operating systems

Stratus Technologies ported its custom operating systems to its fault tolerant Continuum PA-RISC servers in the 1990s: both Unix and transaction-oriented systems. Operating system support was split between Stratus Continuum 400 and the Continuum 600 and 1200 on the other hand.

- ◇ Stratus FTX, Stratus System V Unix (on Continuum 400)
- ◇ HP-UX 11.00, modified by Convex (on Continuum 400)
- ◇ Stratus VOS, Stratus transaction processing (on Continuum 600/1200)

FTX Unix

Stratus Continuum 400 were marketed with Stratus-modified HP-UX Unix 11.00 as main choice but also supported Stratus FTX Unix. FTX was System V Unix from Stratus and only sold on an exceptional basis.

FTX (Fault Tolerant Unix) was a System V Unix operating system from Stratus designed for high availability and reliability with fault-tolerance mechanisms. It was developed by Stratus for its own fault-tolerant computer systems.

There also was a cancelled effort to port the Stratus VOS operating system to the 400s. Continuum 400 servers running the Stratus-modified HP-UX 11.00 were fully binary compatible with stock HP-UX — programs compiled for “normal” HP-UX ran without changes on Continuum 400.

VOS

Stratus Continuum 600 and 1200 were sold primarily with Stratus VOS for transaction processing, with releases 13.0 (1995) to 14.7.2 (2005) on PA-RISC hardware. Also offered on the 600s and 1200s on exceptional basis was Stratus FTX, hardware support was limited though.

VOS was developed by Stratus as transaction-oriented operating system for its fault-tolerant servers. Stratus added a Unix implementation (System V) called Unix System Facilities (USF) to VOS and later added POSIX compliance as well.

3.58.6 Documentation

- ◇ HP-UX Continuum 400 Series (PA-7100) Technical Service Guide (no URL)
- ◇ The Stratus Continuum Family (URL gone)
- ◇ Stratus Continuum 400 Series Fault-Tolerant HP-UX Servers, Stratus Technologies 2003
- ◇ Stratus Continuum Products 600 and 1200, Stratus Technologies 2003
- ◇ Stratus Machine History (August 2017: Paul Green. Accessed March 2021)
- ◇ Stratus HP-UX Brochure, Stratus 2004
- ◇ Stratus VOS Operating System, Count on Stratus, Stratus 2004

Stratus Continuum Series - VOS, Stratus Virtual Operating system, Stratus 2003 SVOS Software Release Bulletins, Stratus 2004, FTP

- ◇ Continuum 600/1200 Series (PA-7100) Service Announcement, Stratus 1998
- ◇ Stratus Shifts High-End Servers From PA-RISC to Intel, Computer World 2004
- ◇ Stratus Continuum 600/1200 Series Systems, cabinet illustration and parts, Stratus customers service
- ◇ Servers in the Stratusphere, HP Professional June 1999

3.59 PA-RISC Third Party Systems

Not only HP sold PA-RISC computers in the golden decade of Unix RISC workstations in the 90s. Several third party vendors organized in the Precision RISC Organisation (PRO) sold rebadged HP 9000 computers in East Asia in the mid-1990s or developed custom PA-RISC platforms.

- ◇ Hitachi sold custom 3050RX and 3500 PA-RISC workstations and servers with HP CPUs and relabeled HP 9000 systems as OEM, the 9000V series. Hitachi also developed own PA-RISC processors, the PA/50 and HARP-1, used in some specific Hitachi computers.
- ◇ Mitsubishi marketed the original HP 9000 720, 730 and 750 in the early-1990s as MELCOM ME RISC and sold them in Japan.
- ◇ NEC was very active in PRO with the NX7000 and TX7 ranges of PA-RISC computers that were based off OEM rebranded D, K, L, S and T-Class.
- ◇ OKI offered a large range of HP 9000 PA-RISC servers and workstations, OEM rebranded as OKITAC 9000 series. In its semiconductor business, OKI also developed a custom PA-RISC processor, the OP32 for embedded devices.
- ◇ Samsung marketed rebadged HP 9000 715 workstations in Korea.

These computers were shipped with Unix operating systems, geared towards technical and scientific users. Vendors either licensed HP-UX Unix directly or slightly modified it like Hitachi with HI-UX/WE2 and HI-UX/MPP or Samsung with SS-UX (?). Documentation on these computers and software is almost nonexistent, few sources describe them at all, except some press releases.

3.59.1 Hitachi

Hitachi and HP had a “long-term” alliance since 1989 that included joint PA-RISC development, before HP opened up the PA-RISC alliance with the PRO consortium in the 1990s. Hitachi then built several lines of computers with PA-RISC processors as part of that consortium over the next years: custom workstations (3050RX) and servers (3500) for HI-UX/WE2, and rebadged HP 9000, sold in Japan as Hitachi 9000V with HP-UX, and the SR2 supercomputers with HI-UX/MPP.

Hitachi 3050RX workstations

Hitachi designed a range of custom PA-RISC workstations for the Japanese market in the 90s. These very rare systems were apparently marketed as “Hitachi Creative Station 3050RX Group” and ran HI-UX/WE2, the Hitachi HP-UX variant.

The 3050RX 200 was billed as one “the industry’s cheapest Unix workstations with a harddisk” at time of release in 1993.

System	Processor	Cache	RAM	Expansion
3050RX/100CLaptop	Hitachi PA/50L 33 MHz	8/4 KB	80 MB	10.4", 1024x768 TFT
3050RX/200low-cost	Hitachi PA/50M33 MHz	8/4 KB	144 MB	\$6.190
3050RX/220	PA-7100 50 MHz	64/64 KB	192 MB	none
3050RX/220	PA-7100LC 60 MHz	256 KB	?	?
3050RX/230	PA-7100 80 MHz	256/256 KB	192 MB	none
3050RX/235	PA-7100LC 80 MHz	512 KB	?	?

3050RX/255	PA-7300LC 132 MHz	64/64 KB L1(1 MB L2)	256 MB	Two slots
3050RX/310S	PA-7100 33/40 MHz	64/64 KB L1	272 MB	One slot
3050RX/320	PA-7100 50 MHz	64/64 KB L1	416 MB	Three slots
3050RX/320G	PA-7100 50 MHz	64/64 KB L1	192 MB	Three slots
3050RX/320S	PA-7100 50 MHz	64/64 KB L1	272 MB	One slot
3050RX/330	PA-7100 80 MHz	256/256 KB	416 MB	Three slots
3050RX/330G	PA-7100 80 MHz	256/256 KB	192 MB	Three slots
3050RX/330T	PA-7100 80 MHz	256/256 KB	192 MB	Three slots
3050RX/330	PA-7100 100 MHz	256/256 KB L1	416 MB	Three slots
3050RX/355E	PA-7300LC 132 MHz	64/64 KB L1(1 MB L2)	1.5 GB	Two slots one audio
3050RX/365	PA-7300LC 160 MHz	64/64 KB L1(1 MB L2)	1.5 GB	Two slots one audio
3050RX/430	PA-7100 80 MHz	256/256 KB L1	768 MB	Seven slots
3050RX/440	PA-7100 100 MHz	256/256 KB L1	768 MB	Seven slots
3050RX/535	PA-7100LC 80 MHz	512 KB L1	?	?

Hitachi 3500 servers

Hitachi also sold specially branded servers, the 3500, in 1993, which were equivalently rare as the 3500RX workstations and also ran HI-UX/WE2, Hitachi's HP-UX variant.

System	Processor	Cache	RAM	Expansion
3500/310	PA-7100 50 MHz	64/64 KB	416 MB	?
3500/410	PA-7100 50 MHz	64/64 KB	512 MB	?
3500/510	PA-7100 50 MHz	64/64 KB	512 MB	?
3500/520	PA-7100 50 MHz	256/256 KB	512 MB	?
3500/530	PA-7100 80 MHz	256/256 KB	512 MB	?
3500/540	PA-7100 100 MHz	256/256 KB	512 MB	?
3500/630	PA-7100 80 MHz	256/256 KB	1024 MB	?
3500/640	PA-7100 100 MHz	256/256 KB	1024 MB	?

Hitachi 9000V OEM systems

Hitachi also sold a line of original HP systems as OEM (probably only in Japan) — rebranded as “Hitachi 9000V series” which included the following systems from 1995 onwards:

System	Processor	HP equivalent
9000V V715/100XC, V715/100, V715/80, V715/64	PA-7100LC	HP 9000/715 (newer models)
9000V V715/100Tiny, V715/80Tiny	PA-7100LC	HP 9000/712 (probably)
9000V V735/125	PA-7150	HP 9000 735/125
9000V VE55, VE45, VE35, VE25	PA-7100LC	HP 9000/E-Class
9000V VQ200, VQ210	PA-7200	HP 9000/J200, HP 9000/J210
9000V VR100, VR200, VR400	PA-7200	HP 9000/K100, HP 9000/K200, HP 9000/K400
9000V VT500	I-12 PA-7100	HP 9000/T500 (T-Class)
9000V VT600	I-12 PA-8000	HP 9000/T600 (T-Class)
9000V VT800	I-16 PA-8000	might be based on HP S-Class

Hitachi Supercomputers

Hitachi developed and produced a line of 32-bit supercomputers based on its own PA-RISC chips utilizing a hyper (3-D) crossbar design. Both ran Hitachi HI-UX/MPP, an Unix with Mach 3.0 microkernel extensions.

System	CPU	Caches	RAM	Performance	Notes
SR200I	8-128 Hitachi HARP-I 90 MHz	8/16 KB L1 512/512 KB	4 GB	23 GFLOP	Distributed memory parallel system
SR220I	32-1024 Hitachi HARP-IE 150 MHz	8/16 KB L1 512/512 KB	256 GB	307 GFLOP	Distributed memory parallel system vector processing

3.59.2 Mitsubishi

Mitsubishi Electric of Japan sold OEM rebranded HP 9000 workstations in the early 1990s as “MELCOM ME RISC series” as part of the PRO consortium for PA-RISC OEMs. Apparently three models were sold, all based on the original HP 9000 workstations 720, 730 and 750 (– some sources also mention an 705 and 710 equivalent). The computers were marketed for graphical use cases with HP GRX and other high-end graphics adapters.

System	Processor	HP equivalent	Price
ME/R7200ME/S7200	PA-700050 MHz	HP 9000/720	\$23,453
ME/R7300ME/S7300	PA-700066 MHz	HP 9000/730	
ME/R7500ME/S7500	PA-700066 MHz	HP 9000/750	

Almost no information exists on Mitsubishi PA-RISC and MELCOM ME RISC apart from few press releases – these were probably not very widely sold.

3.59.3 NEC

NEC Electronics of Japan was also a Precision RISC Organization (PRO) member and actively sold PA-RISC computers marketed as TX7 in the mid-1990s mostly in Japan. TX7 and NX7000 were often rebadged HP 9000 computers sold by NEC as OEM, with the custom P590 designed by NEC to “fill the gap between D and K-Class”. NEC PA-RISC computers ran licensed HP-UX Unix.

System	Processor	HP equivalent	Price
NX7000/220 NX7000/420	1-4 PA-7200 160-180 MHz	HP 9000/K-Class	¥8,680,000 ¥12,160,000
NX7000/27 NX7000/37	1-2 PA-8000 180 MHz	HP 9000/D-Class	¥4,000,000 ¥4,600,000
NX7000/250 NX7000/260 NX7000/450 NX7000/460	1-4 PA-8000 160-180 MHz	HP 9000/K-Class	¥9,200,000 ¥10,600,000 ¥11,700,000 ¥13,200,000
NX7000/500	1-12 PA-7100 90 MHz	HP 9000/T500	
NX7000/520	1-14 PA-7150 120 MHz	HP 9000/T520	¥27,500,000

NX7000/L1000 NX7000/L2000 NX7000/L3000	1-2 PA-8500 1-4 PA-8500 1-4 PA-8600	HP 9000 L1000 HP 9000 L2000 HP 9000 L3000	Â€3,200,000 Â€4,300,000
NX7000/PS200	1-1024 PA-8000 160-180 MHz	Custom or S-Class?	Â€36,000,000
TX7/D280	PA-8000 180 MHz	HP 9000 D-Class	Â€4,700,000
TX7/K370	PA-8200 200 MHz	HP 9000 K-Class	Â€10,700,000
TX7/P590	1-8 PA-8000	Custom NEC	Â€17,600,000
TX7/V2200	4-16 PA-8200 200 MHz	HP 9000/V2200	Â€31,500,000

3.59.4 OKI

Similar to Mitsubishi in the early 1990s, Oki Electric Industry sold various PA-RISC workstations and servers from HP rebranded as OEM systems. These were integrated into the “OKITAC” brand of OKI and shipped from 1992 onward mostly in Japan, running stock HP-UX.

System	HP equivalent
OKITAC 9000/800 Series	HP 9000/800 Nova servers
OKITAC 9000 A Series	HP 9000/A180C
OKITAC 9000 B Series	HP Visualize B1000
OKITAC 9000 C Series	HP Visualize C3000
OKITAC 9000 D Series	HP 9000 D-Class
OKITAC 9000 J Series	HP Visualize J5000
OKITAC 9000 K Series	HP 9000 K-Class
OKITAC 9000 R Series	HP 9000 R380 and R390

OKI also developed a custom PA-RISC processor in the 1990s as member of the Precision RISC Organization (PRO) consortium. This OP32 processor was not used in its own workstations, but geared towards embedded devices.

3.59.5 Samsung

Samsung Electronics produced and sold HP 9000 workstations under licence from 1993 on as part of the Precision RISC Organization, PRO. Custom workstation systems were designed by the Samsung Workstation Division in San Jose, USA, running “SS-UX” operating system with “added I/O-features” to HP-UX Unix, which Samsung also licensed from HP.

System	Processor	HP equivalent	Price
SWS715	PA-710050 MHz	HP 9000 715	\$14,000
SWS715	PA-710033 MHz	HP 9000 715	\$4,000

Samsung intended to sell the SWS715 through indirect channels to non-HP partners, targeting “imaging and scientific visualisation”, probably limited to the Korean market. Press releases mention Samsung planning to develop its own PA-RISC processor, with integrated memory technology, and separately port or ship Microsoft Windows NT to its PA-RISC computers.

3.59.6 Documentation

Documentation on these computers and software is almost non-existent anymore, and few sources describe them at all, except some surviving press releases.

- ◇ IPSJ Computer Museum: 3050RX Hitachi Group/3500 Series, Information Processing Society of Japan (n.d. Accessed August 2008)
- ◇ The Hitachi SR2201 series, Overview of Recent Supercomputers, Aad van der Steen, October 2004
- ◇ The Hitachi SR2201 series, Overview of recent supercomputers, Aad van der Steen, NCF, September 1994 (PDF)
- ◇ HITACHI CLAIMS TO HAVE THE INDUSTRY'S CHEAPEST UNIX WORKSTATION, USING PRECISION ARCHITECTURE..., CBR Online Archive, 28 Oct 1993
- ◇ October 1993 PROgress Newsletter, USENET post, Google Archive, 11/01/1993
- ◇ SAMSUNG, WITH FIRST PA-RISC STATION, COMMITS TO NT, CBR Online Archive, 21 March 1993
- ◇ MITSUBISHI DEMONSTRATES AGREEMENT WITH H-P, CBR Online Archive, 22 May 1991
- ◇ Main Specifications and Features of the TX7 Scalable Server Series, NEC Press Release December 1997
- ◇ Release of New Low-End Models of the NX7000 Series That Realize Double the Price-Performance of Current Models, NEC Press Release September 1999
- ◇ Main specifications of NX7000/L1000 and L2000, NEC Press Release September 1999
- ◇ NEC INTRODUCES SCI/TECH SERVERS, PARTNERS WITH HP, HPC Wire, December 5, 1997
- ◇ NEC GETS EVEN FRIENDLIER WITH HP, CASTS DOUBT ON MIPS WORK, CBR Archive, December 7, 1997
- ◇ >NEC NX7000/500, Information Processing Society of Japan, n.d.
- ◇ Fujitsu to Enhance NX7000 Series with New Models and MPP Parallel Server Suitable for Building Large-Scale Decision Support Systems, NEC Press Release January 1996
- ◇ Release of three high-performance models of UNIX server NX7000 series, NEC Press Release March 1996
- ◇ Hitachi to Release High-end 9000V Series UNIX Server, Hitachi Press Release October 1997
- ◇ HP, HITACHI AND NEC TO BRING ENHANCED RESILIENCE FOR MISSION-CRITICAL APPLICATIONS TO ENTERPRISE COMPUTING, NEC Press Release October 1997
- ◇ Hitachi Released the VT800, the top model of the HITACHI 9000V series servers., Hitachi Press Release October 1997

3.60 HP Visualize P-Class NT Workstations

HP Visualize Personal Workstations were Intel-based computers for Windows NT, released in 1999. With P-Class, HP complemented its PA-RISC Visualize Unix workstations. Systems A5015A from P450 to P700C were entry-level HP NT workstations, followed by X-Class.

Based on Intel Pentium III processors up to two-way SMP capable and with Intel 440BX chipset, the P-Class started with P450, P500 and P600 using *Katmai* processors, updated later in P600C, P650C and P700C with *Coppermine* CPUs.

They were dedicated professional graphics workstations for 3D design, CAD and CAM on Windows NT, used for “professional digital content creation.”

Visualize P-Class shared almost nothing with the PA-RISC based Visualize brethren but the Visualize graphics adapters, which they use in modified + Versions on AGP. They also were shipped with 3rd-party graphics such as Elsa Gloria Synergy II and 3Dlabs Oxygen GVX-1.

The dark-grey mini-tower HP P-Class used was similar to PA-RISC HP Visualize B1000, C3000, C3600, C3700 workstations and apparently the same to lower-end HP Kayak PCs.

System	Number	Config	Introduced	Price
P450	A5015A	entry	1999	\$3,225
P500	A5015A	entry	1999	\$4,060
128 MB, fx2+	1999	\$4,060		
dual, 128 MB, fx4+	1999	\$9,630		
P600	A5015A	entry	1999	\$3,300
P600C	A5015A	entry	2000	\$2,600
P650C	A5015A	entry	2000	
P700C	A5015A	entry	2000	

There was a technically different P-Class A6034A released soon after, based on Pentium III and RCC chipset.

3.60.1 System architecture

Processors

System	CPU	Speed	L1 Cache	L2 Cache*
HP Visualize P450	1-2 Intel Pentium III	450 MHz	32 KB on-chip	512 KB back-side
HP Visualize P500	1-2 Intel Pentium III	500 MHz	32 KB on-chip	512 KB back-side
HP Visualize P550	1-2 Intel Pentium III	550 MHz	32 KB on-chip	512 KB back-side
HP Visualize P600	1-2 Intel Pentium III	600 MHz	32 KB on-chip	512 KB back-side
HP Visualize P600C	1-2 Intel Pentium III	600 MHz	32 KB on-chip	256 KB on-chip
HP Visualize P650C	1-2 Intel Pentium III	650 MHz	32 KB on-chip	256 KB on-chip
HP Visualize P700C	1-2 Intel Pentium III	700 MHz	32 KB on-chip	256 KB on-chip

P450 to P600 use Pentium III *Katmai* processors with 512 KB L2 cache on half-frequency back-side bus (BSB). P600C to P700C use Pentium III *Coppermine* with integrated 256 KB L2 on full-frequency.

CPUs are installed in SECC(2) cartridges in two Slot 1 slots. CPU frequencies are hard-coded but can

be selected with switches 3, 4 and 5. VRMs required might be 0950-2837 and/or 0950-3310.

Chipset

- ◇ Intel 440BX AGP chipset
 - Intel 82443BX Host Bridge/Controller *North Bridge*, connects CPU bus (GTL), memory bus (SDRAM), PCI and AGP buses
 - Intel PIIX4E (82371EB) *South Bridge*, connects PCI to ISA, USB and IDE
- ◇ (integrated) IDE controller PCI Bus master Ultra ATA/33 (in 82371EB)
- ◇ (integrated) USB controller (in 82371EB)
- ◇ NS87317, Ultra I/O, integrates parallel, serial, keyboard, mouse, floppy controllers and RTC
- ◇ Two ROM sockets for flash ROMs
- ◇ *Optional* PCI Ultra Wide SCSI controller
- ◇ Graphics through separate boards, usually shipped with:
 - *Optional* Visualize *fx* OpenGL 3D with 18 MB SGRAM and 16-32 MB SDRAM, dual PCI-AGP
 - *Optional* Visualize *fx2+*, *fx4+*, *fx6+* with 18 MB SGRAM, dual PCI-AGP
 - *Optional* ELSA GLoria Synergy with 8MB SGRAM
 - *Optional* ELSA Synergy II
 - *Optional* Oxygen GVX1
- ◇ Analog Devices AD1816 sound chip
- ◇ *Optional* Combo LAN/SCSI card with HP 10BT/100TX Ethernet (AMD PCNET) and Symbios SYM5C875JE Ultra Wide SCSI
- ◇ *Optional* Some P-Class apparently had SCSI on-board

System buses

- ◇ Intel 100 MHz Front-side bus (FSB), Processor-Local (GTL) bus, 64-bit with ECC
- ◇ Memory bus 100 MHz (SDRAM) CL2, 64-bit with ECC, 800 MB/s throughput
- ◇ PCI 33 MHz 3.3V bus
- ◇ AGP 66 MHz
- ◇ ISA bus
- ◇ IDE PIO mode 4 and Bus Master IDE

Memory

- ◇ 100 MHz SDRAM DIMMs non-buffered or registered ECC
- ◇ Four slots for 128/256 MB modules (documentation sometimes mentioned three)
- ◇ Non-buffered and registered ECC cannot be mixed
- ◇ 128 MB to 1 GB maximum registered ECC (documentation mentions 2 GB)
- ◇ 128 MB to 384 MB non-buffered (unclear)
- ◇ *Optional* Some P-Class had four, some had three memory slots

Expansion slots

- ◇ One AGP slot, 66 MHz
- ◇ Three PCI slots, 33 MHz
- ◇ One ISA slot
- ◇ One ISA or PCI slot
- ◇ I/O slot layout (from top to bottom):
 1. AGP
 2. PCI 32-bit, PCI 1
 3. PCI 32-bit, PCI 2
 4. PCI 32-bit, PCI 3
 5. PCI 32-bit or ISA 16-bit, PCI 4
 6. ISA 16-bit

Storage

- ◇ Hard drives either Ultra ATA/33 or Ultra Wide SCSI
- ◇ 3.5" Floppy drive
- ◇ Two internal trays for 3.5" drives
- ◇ Two external trays for 3.5" drives
- ◇ Three external trays for 5.25" drives, CDs etc.

3.60.2 External ports

- ◇ Two serial RS232C DB9
- ◇ VGA DB 15-pin
- ◇ Parallel DB25
- ◇ Two USB ports

- ◇ Two PS/2 ports for keyboard/mouse
- ◇ Two phone jacks for audio

3.60.3 Operating systems

- ◇ Windows NT, original support and drivers
- ◇ Windows 2000, original support and drivers
- ◇ Linux, original support and drivers
- ◇ many other PC operating systems

3.60.4 Dimensions

System	Height	Width	Depth	Weight
Desktop	415mm	211mm	420mm	11kg

There is an LCD panel on the front of the case which shows BIOS and configuration info and possible detected errors by the BIOS, enhanced by beeps. The LCD can also be used for diagnostics.

3.60.5 Benchmarks

No official SPECint or fp results could be found for HP Visualize P-Class, so the results are based on comparable Intel Pentium III and BX reference data.

Table 3.216: * - assumed results based on reference data

System	Processor	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp
HP Visualize P450*	Intel Pentium III 500 MHz	17.3*	12.7*	211*	177*
HP Visualize P500*	Intel Pentium III 500 MHz	20.7*	14.7*	231*	191*
HP Visualize P550*	Intel Pentium III 550 MHz	22.3*	15.1*		
HP Visualize P750C*	Intel Pentium III 750 MHz	35.7*	22.9*	325*	219*
HP Visualize B1000	PA-8500 300 MHz	23.9	39.3		
HP Visualize C3000	PA-8500 400 MHz	31.8	52.4	313	321
HP Visualize C3750	PA-8700+ 875 MHz			678	674

3.60.6 Documentation

Manuals

- ◇ HP VISUALIZE P-Class Personal Workstations (P450, P500, P550 and P600), HP 1999, 5968-4831E
- ◇ HP VISUALIZE P-Class Technical Specifications, HP website 1999
- ◇ HP VISUALIZE Personal Workstation P-Class Technical Reference, HP 1999, A5015-90021, VOGONS mirror
- ◇ hp workstation p-class summary, HP website , 2001

Articles

- ◇ HP DEBUTS PENTIUM III-BASED HP VISUALIZE P600 WORKSTATION, Computer Workstations, September 1999
- ◇ HP Intros HP Visualize Personal Workstations, HPC Wire, April 1999
- ◇ Reviews: HP Visualize P600C, Computer Graphics World, February 2000
- ◇ HP Intros HP Visualize Personal Workstations, HPC Wire, November 1999
- ◇ 1999 CATIA Version 5 Benchmark, CATIA Solutions Magazine, July/August 1999, FTP mirror
- ◇ An Overview of the VISUALIZE fx Graphics Accelerator Hardware, HP Journal 1998, Article 4
- ◇ VISUALIZE Workstation Graphics for Windows NT, HP Workstation Lab 1998
- ◇ HP VISUALIZE Workstation Family photo card, HP 1998
- ◇ Adding a Second CPU to the HP Kayak, VRM information also applicable to Visualize P-Class, Chris Winter, 2018

Drivers and BIOS

- ◇ hp workstation Windows NT 4.0 drivers for p class (“low”), HP website 2000
- ◇ HP Workstations Windows 2000 drivers, HP website 2000
- ◇ hp workstation HK.W1.02 BIOS for p/pL class, HP website 2001

3.6I HP Visualize X-Class NT Workstations

HP Visualize X-Class were Intel-based personal workstations for Windows NT, released in 1999. With the Pentium III-based X-Class, HP complemented its expensive PA-RISC workstations for entry-level technical design.

X-Class X500 to X550 (model A5014A) were high-performance HP NT workstations, above similar, but lower-tier Visualize P-Class.

Based on Intel Pentium III processors and up to two-way SMP capable with Intel 440GX chipset, X-Class used modern 32-bit *Xeon* CPUs in contrast to Katmai/Coppermine and BX P-Class.

HP Visualize X-Class were dedicated professional graphics workstations for 3D design, CAD and CAM on Windows NT, used for “professional digital content creation.”

Visualize X-Class shared almost nothing with the PA-RISC based Visualize brethren but the Visualize graphics adapters, which they use in modified + Versions on AGP. They also were shipped with 3rd-party graphics such as Elsa Gloria Synergy.

The dark-grey mini-tower HP X-Class used was similar to PA-RISC HP Visualize B1000, C3000, C3600, C3700 workstations and slightly different to P-Class.

- ◇ HP Visualize X500, A5014A, were introduced in 1999
- ◇ HP Visualize X500, A5014A, with dual-CPU, 512 MB RAM and Visualize fx6 cost \$12,326
- ◇ HP Visualize X550, A5014A, were introduced in 1999 for \$5,906

The later different Visualize x-class workstations were released soon after, based on Pentium III Xeon processors with RCC chipset, HP models A1280A and A1280B.

3.6I.1 System architecture

Processors

X500 and X550 use Pentium III *Xeon* processors with 512 KB or 1 MB L2 cache on full-frequency. CPUs are installed in SEC cartridges in two Slot 2 slots.

System	CPU	Speed	L1 Cache	L2 Cache*
X500	1-2 Intel Pentium III	500 MHz	32 KB on-chip	0.5-1.0 MB on-package
X550	1-2 Intel Pentium III	550 MHz	32 KB on-chip	512 KB back-side on-package

Chipset

- ◇ Intel 440GX AGP chipset
- ◇ Intel 82443GX Host Bridge *North Bridge*, connects CPU bus (FSB), memory bus (SDRAM), PCI and AGP buses
- ◇ Intel PIIX4E (82371EB) *South Bridge*, connects PCI to ISA, USB and IDE
 - (integrated) IDE controller PCI Bus master Ultra ATA/33
 - (integrated) USB controller
 - (integrated) DMA (82C37) and Interrupt (82C59) controllers

- (integrated) Power Management
- (integrated) SMBus interface
- ◇ NS87317, Ultra I/O, integrates parallel, serial, keyboard, mouse, floppy controllers and RTC
- ◇ Two ROM sockets for flash ROMs
- ◇ Adapter AIC 7880 PCI Ultra Wide SCSI controller
- ◇ Graphics through separate boards, usually shipped with:
 - *Optional* Visualize fx OpenGL 3D with 18 MB SGRAM and 16-32 MB SDRAM, dual PCI-AGP
 - *Optional* Visualize fx2+, fx4+, fx6+ with 18 MB SGRAM, dual PCI-AGP
 - *Optional* ELSA GLoria Synergy+ with 8 MB SGRAM
 - *Optional* ELSA Synergy II
 - *Optional* Oxygen GVX1
- ◇ Analog Devices AD1816 sound chip
- ◇ *Optional* Combo LAN/SCSI card with HP 10BT/100TX Ethernet (AMD PCNET) and Symbios SYM5C875JE Ultra Wide SCSI
- ◇ *Optional* HP FastRAID card for caching and RAID (133 MB/s)
- ◇ *Optional* Some X-Class apparently had SCSI on-board

System buses

- ◇ Intel 100 MHz Front-side bus (FSB), Processor-Local (AGTL+) bus, 64-bit with ECC, 800 MB/s data rate
- ◇ Memory bus 100 MHz (SDRAM) CL2, 64-bit with ECC, 800 MB/s data rate
- ◇ PCI 33 MHz 3.3V bus
- ◇ AGP 32-bit 66 MHz (2X), up to 568 MB/s data rate
- ◇ SCSI Ultra-wide storage bus, 16-bit, 40 MB/s
- ◇ ISA bus, 16-bit, 8.33 MHz, 16 MB/s
- ◇ IDE PIO mode 4 and Bus Master IDE

Memory

- ◇ 100 MHz SDRAM DIMMs either non-buffered or Registered ECC
- ◇ Four slots for 64/128/256 MB or 512 MB (Registered) modules
- ◇ Non-buffered or Registered ECC cannot be mixed
- ◇ 64 MB to 1 GB maximum (Non-Buffered)
- ◇ 64 MB to 2 GB supported (Registered ECC)

Expansion slots

- ◇ One AGP slot, 66 MHz
- ◇ Four PCI slots, 33 MHz
- ◇ One ISA or PCI slot
- ◇ I/O slot layout (from top to bottom):
 1. AGP
 2. PCI 32-bit, PCI 1
 3. PCI 32-bit, PCI 2
 4. PCI 32-bit, PCI 3 + HP RAIDport
 5. PCI 32-bit, PCI 4
 6. PCI 32-bit or ISA 16-bit, PCI 5

Storage

- ◇ Hard drives either Ultra ATA/33 or Ultra Wide SCSI
- ◇ 3.5" Floppy drive
- ◇ Two internal trays for 3.5" drives
- ◇ Two external trays for 3.5" drives
- ◇ Three external trays for 5.25" drives, CDs etc.

3.61.2 External ports

- ◇ Two serial RS232C DB9
- ◇ VGA DB 15-pin
- ◇ Parallel DB25
- ◇ Two USB ports
- ◇ Two PS/2 ports for keyboard/mouse
- ◇ Two phone jacks for audio

3.61.3 Operating systems

- ◇ Windows NT, original support and drivers
- ◇ Windows 2000, original support and drivers
- ◇ Linux, original support and drivers
- ◇ many other PC operating systems

3.61.4 Dimensions

System	Height	Width	Depth	Weight
Desktop	510mm	270mm	416mm	22kg

The LCD panel on front of the case shows BIOS and configuration info and errors by the BIOS, enhanced by beeps. The LCD can also be used for diagnostics.

3.61.5 Benchmarks

No official SPECint or fp results could be found for HP Visualize X-Class, so a similar Dell workstation 610 with GX chipset is taken as reference.

Table 3.219: * - assumed results based on reference data

System	Processor	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp
HP Visualize P500* (BX)	Intel Pentium III 500MHz	20.7*	14.7*	231*	191*
Dell Precision 610	Pentium III 500MHz	21.6*	15.5*		
Dell Precision 610	Pentium III 550MHz	24.2*	16.8*		
HP Visualize B1000	PA-8500 300MHz	23.9	39.3		
HP Visualize C3000	PA-8500 400MHz	31.8	52.4	313	321
HP Visualize C3750	PA-8700+ 875MHz			678	674

3.61.6 Documentation

Manuals

- ◇ HP VISUALIZE X-Class Personal Workstations (X500 and X550), HP 2000, A1280-90002
- ◇ HP VISUALIZE X-Class Personal Workstation, HP 1999, 5968-4832E
- ◇ HP VISUALIZE Personal Workstation X-Class Technical Reference, HP 1999, A5014-90020
- ◇ hp x-class overview & features, HP website 2001
- ◇ hp x-class workstation Data Sheet, HP 2001, 5980-3724ENUS

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- ◇ HP Intros HP Visualize Personal Workstations, HPC Wire, April 1999
- ◇ Reviews: HP Visualize P600C, Computer Graphics World, February 2000
- ◇ HP Intros HP Visualize Personal Workstations, HPC Wire, November 1999
- ◇ HP Announces Visualize X-Class Personal Workstation, HPC Wire, January 2000
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- ◇ An Overview of the VISUALIZE fx Graphics Accelerator Hardware, HP Journal 1998, Article 4
- ◇ VISUALIZE Workstation Graphics for Windows NT, HP Workstation Lab 1998
- ◇ HP VISUALIZE Workstation Family photo card, HP 1998, 5968-4840E

Drivers and BIOS

- ◇ hp workstation Windows NT 4.0 drivers for x class, HP website 2001
- ◇ HP Workstations Windows 2000 drivers, HP website 2000
- ◇ X-Class Windows 2000 drivers , HP website 2001
- ◇ hp workstation BIOS for Intel based systems , HP website 2001
- ◇ hp workstation ID.W2.02 BIOS for x/xL class, p/pL class, HP website 2001

3.62 HP Visualize x-class p-class Xeon

HP updated the Visualize Personal Workstations line in 2000 with new Intel-based models in the x-class and p-class. Models A1280 were new x-class, A6034 the new p-class – both identical besides maximum memory and some expansion configurations.

Based on Intel Pentium III Xeon Cascades processors, they were up to two-way SMP capable with rare RCC *ServerWorks* chipset and *Xeon* CPU models and updated earlier P-Class and X-Class workstations.

Visualize X-Class and P-Class *high* were NT-based workstations for Mechanical Design Automation (MDA) and Digital Content Creation (DCC) to complement more expensive HP PA-RISC Unix offerings.

Visualize X-Class shared almost nothing with PA-RISC-based HP Visualize workstations but modified version of Visualize graphics adapters on AGP Pro. They also were shipped with some 3rd-party graphics for 3D.

- ◇ HP Visualize p733, A6034A, were introduced in 1999
- ◇ HP Visualize x733, A1280, were introduced in 1999 for \$6,470
- ◇ HP Visualize x733, A1280A, with fx4, introduced in 2000 for \$7,470
- ◇ HP Visualize p800, A6034A, were introduced in 2000 for \$3,346
- ◇ HP Visualize x800, A1280B, with Elsa Synergy II, introduced in 2000 for \$4,246
- ◇ HP Visualize p866, A6034A, with Elsa Synergy II, introduced in 2000 for \$3,246
- ◇ HP Visualize x866, A1280B, with Elsa GLoria II, introduced in 2000 for \$5,906
- ◇ HP Visualize p1.0, A6034A, introduced in 2000 for \$3,846
- ◇ HP Visualize x1.0, A1280B, with Elsa Synergy II, introduced in 2000 for \$4,746
- ◇ HP Visualize X-Class A1280A were shipped with HP Visualize fx4+ and fx6+
- ◇ HP Visualize X-Class A1280B were shipped with HP Visualize fx5 and fx10 Graphics Cards; ELSA GLoria II and Synergy II
- ◇ HP Visualize X-Class A1280C: unclear
- ◇ HP Visualize P-Class A6034A were shipped with HP Visualize fx5 and fx10 Graphics Cards; ELSA GLoria II and Synergy II

3.62.1 System architecture

Processors

System	CPU	Speed	L1 Cache
HP Visualize x733HP Visualize p733	1-2 Intel Pentium IIIXeon <i>Cascades</i> ?	733 MHz	256 KB on-chip
HP Visualize x800HP Visualize p800	1-2 Intel Pentium IIIXeon <i>Cascades</i> ?	800 MHz	256 KB on-chip
HP Visualize x866HP Visualize p866	1-2 Intel Pentium IIIXeon <i>Cascades</i> ?	866 MHz	256 KB on-chip
HP Visualize x1.0 HP Visualize p1.0	1-2 Intel Pentium IIIXeon <i>Cascades</i> ?	1 GHz	256 KB on-chip

Chipset

Visualize x-class and p-class workstations use a *RCC* chipset, possibly ServerWorks III (HE?), after the company renamed itself.

- ◇ Reliance Computer *RCC* chipset, possibly ServerWorks *ServerSet III HE-SL*
- ◇ *RCC North Bridge*, with memory controller, connects CPU bus (FSB), memory bus (SDRAM), PCI and AGP buses
- ◇ *RCC I/O Bridge*, connects PCI to ISA, USB and IDE
 - (integrated) IDE controller PCI Bus master Ultra ATA/33
 - (integrated) USB controller
 - (integrated) DMA (82C37) and Interrupt (82C59) controllers
 - (integrated) Power Management
 - (integrated) SMBus interface
- ◇ NS87317, Ultra I/O, integrates parallel, serial, keyboard, mouse, floppy controllers and RTC
- ◇ Two ROM sockets for flash ROMs
- ◇ Intel 82559 10/100 Fast Ethernet controller.
- ◇ Graphics through separate boards, usually shipped with:
 - *Optional* Visualize *fx* OpenGL 3D with 18 MB SGRAM and 16-32 MB SDRAM, dual PCI-AGP
 - *Optional* Visualize *fx2+*, *fx4+*, *fx6+* with 18 MB SGRAM, dual PCI-AGP
 - *Optional* Visualize *fx5*, *fx10* up to 64 MB RAM, 6 (PA-RISC) geo engines, AGP
 - *Optional* ELSA GLoria II (“with hp visualize technology”)
 - *Optional* ELSA Synergy II with 32 MB SGRAM
 - *Optional* NVIDIA Quadro2 MXR
- ◇ CS4280 and CS4297 sound chips
- ◇ *Optional* Adaptec SCSI card for Ultra-wide LVD and SE SCSI

System buses

- ◇ Intel 133 MHz 2x Front-side bus (FSB), 64-bit with Parity, data rate
- ◇ Memory bus 133 MHz (SDRAM) CL2, 288/144-bit with ECC, 2 GB/s data rate
- ◇ PCI 33 MHz 3.3V bus
- ◇ PCI 66 MHz 5.0V bus
- ◇ AGP Pro 66 MHz 4X bus
- ◇ SCSI Ultra160 storage bus, 160 MB/s
- ◇ IDE PIO mode 4 and Bus Master IDE

Memory

- ◇ 133 MHz SDRAM 2-way interleaved
- ◇ X-Class (A1280): Eight slots for 64-512 MB SDRAM DIMMs
- ◇ P-Class (A6034): Four slots for 64-512 MB SDRAM DIMMs
- ◇ 64 MB to 2 GB (P-Class) or 4 GB (X-Class) supported

Expansion slots

- ◇ One AGP Pro slot, 66 MHz
 - Possibly on A1280B and A6034 Not supported: Visualize fx4, fx6, fx2+, fx4+, fx6+ (with plain AGP) will not work and might damage the board
 - A1280A was apparently shipped with fx2+ and fx4+ AGP Pro
- ◇ Three PCI slots, 32-bit 33 MHz, 5V
- ◇ Two PCI slots, 64-bit 66 MHz, 3.3V
- ◇ I/O slot layout (from top to bottom):
 1. AGP Pro
 2. PCI 32-bit, PCI 1
 3. PCI 32-bit, PCI 2
 4. PCI 32-bit, PCI 3
 5. PCI 64-bit, PCI 4
 6. PCI 64-bit, PCI 5

Storage

- ◇ Hard drives either Ultra ATA/33 or Ultra160 SCSI
- ◇ 3.5" Floppy drive
- ◇ Two internal trays for 3.5" drives
- ◇ Two external trays for 3.5" drives
- ◇ Three external trays for 5.25" drives, CDs etc.

3.62.2 External ports

- ◇ Two serial RS232C DB9
- ◇ VGA DB 15-pin
- ◇ Parallel DB25
- ◇ Two USB ports

- ◇ Two PS/2 ports for keyboard/mouse
- ◇ Four phone jacks for audio

3.62.3 Operating systems

- ◇ Windows NT, original support and drivers
- ◇ Windows 2000, original support and drivers
- ◇ Linux, original support and drivers
- ◇ many other PC operating systems

3.62.4 Dimensions

System	Height	Width	Depth	Weight
Desktop	483mm	208mm	473mm	15kg

There is an LCD panel on the front of the case which shows BIOS and configuration info and possible detected errors by the BIOS, enhanced by beeps. The LCD can also be used for diagnostics.

3.62.5 Benchmarks

No official SPECint or fp results could be found for newer HP Visualize x- and p-class systems, but some comparisons might be made with systems using a similar ServerWorks ServerSet III chipset, such as DELL Power Edge 4400.

Table 3.222: * - possible using ServerWorks ServerSet LE III, like the p/x-class
- data extrapolated for BX-based P-Class for comparison

System	Processor	SPEC95 int	SPEC95 fp	SPEC2000 int	SPEC2000 fp
DELL Power Edge 4400	Pentium III Xeon 1 GHz*			437	302
HP Visualize P750C	Pentium III 750 MHz	35.7	22.9	325	219
HP Visualize B1000	PA-8500 300 MHz	23.9	39.3		
HP Visualize C3000	PA-8500 400 MHz	31.8	52.4	313	321
HP Visualize C3750	PA-8700+ 875 MHz			678	674

HP PA-RISC were always good performers on FPU loads and pretty strong on a MHz-for-MHz comparison; granted on synthetic benchmarks.

3.62.6 Documentation

Manuals

- ◇ hp x-class workstation Data Sheet, HP 2001, 5980-3724ENUS
- ◇ hp visualize x-class workstations for Windows, HP 2000, 5980-1311E

- ◇ hp visualize x-class workstations for Windows, HP 2000, 5980-1311E
- ◇ HP VISUALIZE Personal Workstation Users Guide, HP 2000, A1280-90002
- ◇ Technical Reference HP Visualize A1280 X-Class and A6034 P-Class Personal Workstations, HP 2000, A1280-90016
- ◇ hp x-class overview & features, HP website 2001

Articles

- ◇ HP Announces Visualize X-Class Personal Workstation, HPC Wire, January 2000
- ◇ HP ANNOUNCES NEW PRODUCTS AND SERVICES, HPC Wire, July 2000
- ◇ HP Sets New Performance Standard With HP VISUALIZE X-Class Personal Workstation, HP Press release 1999

Drivers and BIOS

- ◇ hp workstation Windows NT 4.0 drivers for x class, HP website 2001
- ◇ HP Workstations Windows 2000 drivers, HP website 2000
- ◇ X-Class Windows 2000 drivers , HP website 2001
- ◇ hp workstation ID.W2.02 BIOS for x/xL class, p/pL class, HP website 2001
- ◇ Hp Visualize X Class (A 1280) & P Class (A 6034) Workstation Drivers & Documentation

3.63 PA-RISC Timeline from 1982

This page details the timeline and prices for HP 9000 PA-RISC computers, starting with the HP FOCUS predecessors of PA-RISC in the early 1980s. There are dedicated pages on the history of the HP 9000 PA-RISC Series as well as the PA-RISC Operating System history.

3.63.1 HP 9000 Computers

Below are the release years of PA-RISC processors and computer systems. The data is not complete, especially for entries from the 2000s and there are often discrepancies between announcements, release dates and actual shipped systems.

Table 3.223: PA-RISC hardware timeline

Year	CPU	Workstation	Server	Mainframe	Other
1982	FOCUS	520	530, 540		
1983					
1984			550		
1985					
1986	TS-1			840	
1987	NS-1		825	850	
1988			835		
1989	NS-2 PCX		808, 815 845 822, 832	860	
1990			842, 852	855, 870	
1991	PA-7000	720, 730, 750	865 F10, F20, F30 H20, H30, H40 I30, I40		
1992	PA-7100	705, 710 715/33, 50, 75 725, 735, 755	G50, H50, I50	890	742i, 745i 747i
1993			G60, G70 H60, H70 I60, I70	T500	
1994	PA-7100LC	712/60, 80 715/64, 80, 100 SAIC Galaxy 1100	E25, E35, E45	SPP1000	743i 748i
1995	PA-7200	712/100 715/100XC C100, C110 J200, J210	E55, K100 K200, K210 K400, K410	T520 SPP1200	
1996	PA-7300LC PA-8000	B132L, B160L C160L C160, C180 J280	D200, D300 D210, D310 D260, D360 D270, D370 K250, K260 K450, K460	SPP1600	744, 748

1997	PA-8200	B180L C200, C240 J282, J2240	D220, D320 D230, D330 D280, D380 K370, K570	T600 S-Class, X-Class SPP2000 V2200	
1998	PA-8500	RDI Precision- Book	A180 R380, R390 K380, K580	V2250, V2500	745
1999		C360, C3000 B1000 J5000, J7000	L1000, L2000 rp5430, rp5450 N4000	V2600	
2000	PA-8600	B2000, B2600 C3600 J5600, J6000	A400, A500 rp2400, rp2430 rp2450, rp2470 L1500, L3000 rp5400, rp5450	Superdome	
2001	PA-8700 <i>Merced</i>	C3650, C3700 J6700 <i>i2000</i>	rp5430, rp5470 rp7400, rp8400		
2002	<i>McKinley</i>	<i>zx2000, zx6000</i>	rp2405, rp5405 rp7405, rp7410		
2003	<i>Madison Deerfield</i>		rp8420 <i>rx2600</i> <i>rx5670</i>	Superdome sx1000	
2004	PA-8800 <i>Hondo</i>	c8000	rp3410, rp3440 rp4440 rp7420 <i>rx1600, rx1620</i> <i>rx2620, rx4640</i>		
2005	PA-8900		rp4410		
2006	<i>Montecito</i>			Superdome sx2000	
2007	<i>Montvale</i>		rp7440, rp8440 <i>rx2660</i>		
2008					
2009					
2010	<i>Tukwila</i>				
2011					
2012	<i>Poulson</i>				

3.63.2 Historic prices

Collection of historic prices of PA-RISC computers, around the date of introduction. These are indicative prices which have been collected over the years from a variety of sources, such as press releases, articles, journals. The data is not based on official or coherent sources and as such only indicative. There are probably contradictions and inaccuracies, but it is listed here to preserve some information from that time.

Table 3.224: PA-RISC computers entry dates and pricing

System	Released	Entry price
520	1982	\$30,000
530	1982	\$23,105
540	1982	\$24,115
550	1984	

705 Flounder	1992	\$8,990
710 Bushmaster	1992	\$12,490
712/60 Gecko	1994	\$4,000
712/80 King Gecko	1994	\$8,820
712/100 King Gecko	1995	\$15,100
715/33 Scorpio Jr.	1992	\$4,995
715/50 Scorpio	1992	\$11,895
715/64 Mirage Jr.	1994	\$10,000
715/75 Scorpio	1992	
715/80 Mirage	1994	\$13,000
715/100 Mirage Sr.	1994	\$19,000
715/100XC Turnip	1995	\$21,000
720 Cobra	1991	\$11,990
725/50 Spectra	1992	\$17,895
725/75 Spectra	1992	\$20,295
725/100 Electra	1994	
730 King Cobra	1991	\$19,990
735/99 Hardball	1992	\$37,395
735/125 Hardball	1992	
742i/50 Sidewinder	1992	\$8,000
743i/64 Anole-64	1994	\$4,355
743i/100 Anole-100	1994	\$10,355<
744/132L Anole-132L	1996	\$8,600
744/165L Anole-165L	1997	
745i/50 Pace	1992	\$13,390
745i/100 Fast Pace	1992	
745/132L	1998	\$9,999
745/165L	1998	
747i/50 Pace	1992	\$15,990
747i/100 Fast Pace	1992	
748i/64 Telepace	1994	\$13,910
748i/100 SuperPace	1994	\$19,910
748/132L	1996	\$12,000
748/165L	1996	
750 Coral	1991	\$43,190
755/99 Coral II	1992	\$58,995
755/125 Coral II	1992	
SAIC Galaxy 1100	1994	
RDI PrecisionBook 132	1998	\$11,995
RDI PrecisionBook 160	1998	\$14,995
RDI PrecisionBook 180	1998	
808	1989	\$16,000
815	1989	\$14,900
822 SilverFox Low	1989	\$19,950
825 Firefox	1987	\$42,500
825SRX Firefox	1987	\$69,500
832 SilverFox High	1989	\$30,000
835 TopGun	1988	\$45,000
840 Indigo	1986	\$113,500

842 SilverBullet Low	1990	\$85,000
845 ShoGun	1989	\$59,500
850 Cheetah	1987	\$220,500
852 SilverBullet High	1990	\$143,000
855 Jaguar	1990	\$340,500
860 Cougar	1989	\$291,000
865 Panther	1991	\$275,000
870/300 Panther	1990	\$440,000 (/300)\$530,000 (/400)
890 Emerald	1992	\$340,000
Apollo DN10000	1988	\$79,900-\$235,900
Apollo DSP10000	1988	\$69,900-\$225,900
A180	1998	
A180C	1998	\$16,000
A400	2000	\$4,600
A500	2000	\$9,200
B132L Merlin L2	1996	\$10,840
B160L Merlin L2	1996	\$16,480
B180L Merlin L2	1997	\$16,500
B1000	1999	\$9,900
B2000	2000	
B2600	2000	
C100 Raven T	1995	\$19,715
C110 Raven T	1995	\$25,715
C132L Raven L2	1996	
C160L Raven L2	1996	\$19,480
C160 Raven U	1996	\$24,000
C180 Raven U	1996	\$50,000
C200 Raven U+	1997	\$21,000
C240 Raven U+	1997	\$46,000
C360	1998	\$22,365
C3000	1999	\$13,800
C3600	2000	\$12,243
C3650	2001	\$12,504
C3700	2001	\$15,915
C3750	2001	
C8000	2004	\$9,312
D200 UltraLight	1996	
D210 UltraLight	1996	\$6,900
D220 UltraLight	1997	\$8,900
D230 UltraLight	1997	
D250 UltraLight	1996	
D260 UltraLight	1996	
D270 UltraLight	1996	\$22,260
D280 UltraLight	1997	\$25,450
D300 UltraLight	1996	
D310 UltraLight	1996	
D320 UltraLight	1997	
D330 UltraLight	1997	\$16,700
D350 UltraLight	1996	

D360 UltraLight	1996	
D370 UltraLight	1996	\$25,250
D380 UltraLight	1997	\$30,490
D390 UltraLight	1998	\$30,000
E25 (806) Wright Brothers	1994	\$6,000
E35 (816) Wright Brothers	1994	
E45 (826) Wright Brothers	1994	\$11,320
E55 (856) Wright Brothers	1995	
F10 (807) Old Nova	1991	\$12,895
F20 (807) Old Nova	1991	\$20,000
F30 (837) Old Nova	1991	
H20 (827) Old Nova	1991	
G30/H30 (847) Old Nova	1991	\$65,000
G40/H40 (867) Old Nova	1991	\$112,500
G50/H50 (887) New Nova	1992	
G60/H60 (887) New Nova	1993	
G70/H70 (887) New Nova	1993	
I30 (857) Old Nova	1991	\$95,000
I40 (877) Old Nova	1991	\$140,000
I50 (897) New Nova	1992	
I60 (897) New Nova	1993	
I70 (897) New Nova	1993	
i2000	2001	\$7,000
J200 Skyhawk	1995	\$27,655
J210 Skyhawk	1995	\$35,655
J210XC Light Hawk	1995	
J280 FireHawk	1996	\$38,520
J282 FireHawk	1997	
J2240 FireHawk+	1997	\$55,900
J5000	1999	\$13,118 (single) \$24,313 (dual)
J5600	2000	\$21,108 (dual)
J6000	2000	\$13,118 (single) \$22,575 (dual)
J6700	2001	\$26,454 (dual)
J6750	2001	
J7000	1999	
J7600	2000	
K100 Kittyhawk	1995	
K200 Kittyhawk	1995	
K210 Kittyhawk	1995	\$40,000
K220 Kittyhawk	1996	
K250 Mohawk	1996	\$52,200
K260 Mohawk	1996	\$77,200
K370 Bravehawk	1997	\$66,500
K380	1998	
K400 Kittyhawk	1995	
K410 Kittyhawk	1995	\$65,000
K420 Kittyhawk	1996	
K450 Mohawk	1996	
K460 Mohawk	1996	

K570 Bravehawk	1997	\$86,500
K580	1998	
L1000	2000	\$16,000
L1500	2000	
L2000	1999	\$21,500
L3000	2001	\$39,000
N4000	1999	\$48,000
R380	1998	\$17,350
R390	1998	
rp2400	2000	
rp2405	2002	\$4,795
rp2430	2000	
rp2450	2000	
rp2470	2000	
rp3410	2004	\$4,000
rp3440	2004	\$7,000
rp4410	2005	
rp4440	2004	\$21,000
rp5400	2000	\$16,000
rp5405	2002	\$29,026
rp5430	2000	\$39,000
rp5450	2000	\$21,500
rp5470	2001	
rp7400	2001	
rp7405	2002	\$50,595
rp7410	2002	\$92,250
rp7420	2004	
rp7440	2007	
rp8400	2001	\$124,000
rp8420	2003	
rp8440	2007	
rx1600	2004	\$3,000
rx1620	2004	\$4,000
rx2600	2003	\$7,300
rx2620	2004	
rx4610	2001	\$25,000
rx4640	2004	\$15,000
rx5670	2003	\$27,000
SPP1000/CD	1994	\$145,000
SPP1000/XA	1994	\$550,000
SPP1200/CD	1995	\$160,000
SPP1200/XA	1995	\$586,000
SPP1600	1996	
SPP2000 S-Class	1997	\$189,000
SPP2000 X-Class	1997	\$720,000 \$3M
Superdome	2000	“about \$400,000”
Superdome sx1000	2003	
Superdome sx2000	2006	
T500 TNT 100	1993	\$165,000 uni \$660,000 12-way

T520 TNT 120	1995	\$145,000 uni \$520,000 14-way
T600 Jade 180	1997	
V2200	1997	\$157,000
V2250	1998	
V2500	1998	
V2600	1999	
ZX2000	2002	\$5,554- \$8,340
ZX6000	2002	\$10,520- \$20,070
16600A	1997	\$24,240
16700A	1997	\$9,900
16701A	1997	\$5,000

Further reading

- ◇ HP-UX Support Matrix, Hewlett-Packard Development Company, July 2013

Chapter 4

PA-RISC Operating Systems

4.1 Overview

Many operating systems have been available for PA-RISC computers over the years: Unix was the majority with a few niche systems ported later. The PA-RISC platform was developed for Unix server and workstation duties, so HP shipped its own HP-UX Unix with it, starting in the 1980s.

Modern open source systems have been available for PA-RISC since the early 2000s, with ports of Linux, OpenBSD and NetBSD. These in turn were based on university research projects ported to PA-RISC, including Mach, OSF/1 and BSD. Other, more special systems were available for transactions, real-time and fault-tolerance.

4.1.1 Unix

The main operating system for PA-RISC is HP-UX, the native Unix for HP 9000.

- ◇ **HP-UX:** HP Unix developed by HP for HP PA-RISC computers, HP-UX 11i is the last version from the 2000s for 32-bit, 64-bit and Itanium 2 computers. Popular HP-UX 10.20 has broad 32-bit (and Y2K) support and there were many older HP-UX versions since the 1980s: HP-UX 1.0 to 7.0, HP-UX 8.0 and 9.0.
- ◇ **NeXTSTEP:** Commercial operating system for PA-RISC from NeXT, based on Mach Microkernel, Unix userland and modern GUI, supported PA-RISC in V3.3 in 1994.
- ◇ Several Games run on HP-UX, from iconic 3D to simulation and strategy.

4.1.2 Open Source

Several open source operating systems are available for PA-RISC, development started in the early 2000s with mostly stable support since then.

- ◇ **Linux:** PA-RISC support was included in mainstream Linux during the 2000s and shipped with Debian and Gentoo, now available as part of Debian-ports.
- ◇ **OpenBSD/hppa:** Open source BSD Unix-like operating system ported to HP PA-RISC computers focused on 32-bit workstations and some 64-bit in 32-bit mode.
- ◇ **NetBSD/hppa:** Open source Unix-like operating system, supports PA-RISC computers since around 2005, called NetBSD/hp700 earlier and based on OpenBSD.
- ◇ **QEMU:** The popular open source machine emulator supports PA-RISC since 7.1.0 for running HP-UX, BSD, NextSTEP and Linux on virtual hardware.

4.1.3 Research and Development

PA-RISC was used for many research projects in the late-1980s to mid-90s, many based on Mach—developed at HP, Open Group (OSF) and University of Utah:

- ◇ **MkLinux:** Research project from the mid-1990s by Open Group/OSF to port a Linux kernel onto a Mach microkernel, based on the MK-PA OSF/1.
- ◇ **HPBSD:** Original BSD Unix of the late-1980s, port from the University of Utah of 4.3BSD and later 4.4BSD to early 800s servers and 700s workstations.

- ◇ **Mach:** Several research ports of the Mach microkernel in the early 1990s, with HP Tut Mach 2.0 and the University of Utah with both Mach 3 and Mach 4 Lites.
- ◇ **OSF/1:** The third Unix flavor of the 90s, from the alliance of DEC, IBM, HP to compete with AT&T System V Unix: internal HP OSF/1 and OSF MK-PA OSF/1.
- ◇ **Chorus:** Early microkernel operating system, developed in France in the 1980s. Support PA-RISC in development releases in the early 1990s.

MkLinux and Mach 4/Lites were publically available, others required licenses for source code they contained. Linux and BSD ports made heavy use of their codebase.

4.1.4 Other commercial

There were a few specialized operating systems available for various PA-RISC computers in niche markets. This also includes a few porting attempts to PA-RISC.

- ◇ **MPE/iX:** Business real-time operating system for HP 3000 on PA-RISC. Not covered here – for more information see hpmuseum.net and Bob Green.
- ◇ **HP-RT:** Real-time operating system for HP 9000 740 VME instrumentation computers released from 1992 to 1997.
- ◇ **Convex SPP/UX:** Heavily modified Mach-based operating system for Convex and HP Exemplar SPP PA-RISC mainframes.
- ◇ **Stratus FTX**, a System V Unix, and **Stratos VOS**, a transaction-processing system, for fault-tolerant Stratus Continuum PA-RISC servers.
- ◇ **Clones and OEMs:** PA-RISC OEMs in Asia licensed HP-UX or developed their own, Hitachi with HI-UX/WE2 and HI-UX/MPP and Samsung with SS-UX (?).
- ◇ **Oddball** attempts like Windows NT on PA-RISC and Netware on PA-RISC in the 90s.

4.1.5 Support matrix

Table 4.1: PA-RISC OS support, ■ - full support, ◇ - partial support

OS	700	800	A	B	C	D	E	F-I	J	K	L	N	R	rp	rx	SD	T	V
HP-UX 1-7		■																
HP-UX 8	◇	■						■										
HP-UX 9	■	■			◇	◇	■	■	◇	◇							◇	
HP-UX 10.20	■		◇	◇	■	■	■	■	■	■			■				■	
HP-UX 11.00	◇		■	■	■	■	■	■	■	■	◇	◇	■				■	■
HP-UX 11i v1	◇		■	■	■	■			■	■	■	■	■	■		■	■	■
HP-UX 11i v2			◇								■	■		■	■	■		
HP-UX 11i v3												■		■	■	■		
Linux	■		■	■	■	■	◇		■	■	■		■	◇	◇	◇		
OpenBSD	■		◇	■	◇	◇			◇	◇								
NetBSD	■		◇	■	◇	◇	◇		◇	◇								
QEMU				◇	◇													
NeXTSTEP	◇																	
Mach 3		◇																

Mach 4	◇																	
MkLinux	◇				◇													
OSF/1	◇																	
MK-PA	■								◇									
HPBSD	■								◇									

4.2 HP-UX Unix on PA-RISC

4.2.1 Overview

HP-UX is the commercial Unix operating system from HP for PA-RISC workstations and servers. First developed by HP during the 1980s for early PA-RISC servers and predecessors, last HP-UX 11i from the 2000s runs on most PA-RISC 1.1 and 2.0 and Itanium 2 computers from HP.

HP-UX was standard Unix for HP 9000 computers in the Unix history of PA-RISC. Most PA-RISC computers were shipped with Unix and geared towards technical and business applications, like CAD, CAM, analysis and data processing, with some HP-UX games.

HP-UX started as server operating system with separate releases for PA-RISC workstations until the popular HP-UX 10.20 in 1996. With HP-UX 11.00, there were unified releases for servers and workstations. HP-UX 11 was the first 64-bit HP Unix with support for 64-bit PA-8x00 processors.

Early HP-UX releases up to 9.0 were strongly based on BSD Unix and close to HPBSD. From version 10, HP-UX became close to System V Unix (SVR4), a trend of the 1990s. Many earlier HP-UX Unix versions preceded the internet age with scant documentation left and are rather unknown today: from the first PA-RISC HP-UX 1.0 in 1986 to HP-UX 9 in 1992.

Table 4.2: PA-RISC OS support, ■ - full support, ◇ - partial support

OS	a.k.a.	Year	700	800	A	B	C	D	E	F-I	J	K	L	N	R	rp	rx	SD	T	V	zx/i
HP-UX 11.31	11i v3	2007												■		■	■	■			
HP-UX 11.23	11i v2	2003			◇								■	■		■	■	■			◇
HP-UX 11.20	11i v1.5	2001														■					■
HP-UX 11.11	11i	2000	◇		■	■	■	■			■	■	■	■	■	■		■	■	■	
HP-UX 11.00		1997	◇		■	■	■	■	■	■	■	■	◇	◇	■				■	■	
HP-UX 10.20	10.30	1996	■		◇	◇	■	■	■	■	■	■			■				■		
HP-UX 10.01	10.10	1995	■	■			◇		■	■	◇								◇		
HP-UX 9	.00-09	1992	■	■			◇	◇	■	■	◇	◇							◇		
HP-UX 8	.01-08	1991	◇	■						■											
HP-UX 7	7.03	1990		◇																	
HP-UX 3		1988		■																	
HP-UX 2		1987		◇																	
HP-UX 1		1986		◇																	

4.2.2 HP-UX 11i

HP-UX 11i is the last Unix from HP for its PA-RISC and Itanium computers, first released in 2000 and developed into multiple different streams and operating systems over the years. Versioning got slightly complex.

HP distinguished “operating environments” (OEs) with different functionalities: Minimal and Technical Computing Operating Environment (TCOE and MTOE) for workstations and Foundation, Enterprise and Mission Critical OEs (MCOE) for servers.

There were possibly more OEs not listed here. HP-UX 11i was available in at least the following versions - each with different OEs:

- ◇ 11i v3 (11.31): Itanium 2 servers and few 64-bit PA-RISC servers

- ◇ 11i v2 (11.23): 64-bit PA-RISC servers and Itanium 2 workstations and servers
- ◇ 11i v1.5/v1.6 (11.20/22): Itanium and Itanium 2 workstations
- ◇ 11i v1 (11.11): 32-bit and 64-bit PA-RISC workstations and servers.

HP-UX 11i was called 11.11 in the first version, before HP started another of its many rebrands of Unix products. Notable 11.11 was the last HP-UX version for many PA-RISC workstations, later support was limited to PA-RISC servers.

HP-UX 11i v3 (11.31)

HP-UX 11i v3 was released in 2007 and supported only 64-bit PA-RISC servers and Itanium 2 servers. Support for many other older servers was dropped, including some of (half-modern) rp server family.

Table 4.3: HP-UX 11i v3 (11.31) supported systems

Class	Computers
HP 9000 N-Class	N4000, N4000
HP Integrity rp	rp3410, rp3440, rp4410, rp4440, rp7400, rp7405, rp7410, rp7420, rp7440, rp8400, rp8420, rp8440
HP Integrity rx	rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
HP Superdome	Both PA-RISC and Itanium

HP-UX 11i v2 (11.23)

HP-UX 11i v2 was released in 2005 and supports 64-bit PA-RISC rp servers, Itanium 2 servers and workstations. Support for 32-bit PA-RISC 1.1 systems was dropped, along with most “lettered” 64-bit PA-RISC 2.0 workstations (B-Class, C-Class).

Table 4.4: HP-UX 11i v2 (11.23) supported systems

Class	Computers
HP 9000 A-Class	A400, A500
HP 9000 L-Class	L1000, L2000, L1500, L3000
HP 9000 N-Class	N4000, N4000
HP Integrity rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp4410, rp4440, rp5400, rp5450, rp5430, rp5470, rp7400, rp7405, rp7410 rp7420, rp7440, rp8400, rp8420, rp8440
HP Integrity rx	rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx4610 (not sure), rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
HP Superdome	Both PA-RISC and Itanium
HP Itanium zx	zx2000, zx6000 (v2 May 2005 might be last)

HP-UX 11i v1.5 (11.20) and v1.6 (11.22)

HP-UX 11i v1.5 and v1.6 are the first HP-UX versions for Itanium, released in 2001-2002 for early HP Itanium and Itanium 2 workstations and servers. The separate Itanium and PA-RISC support was later merged into unified 11i v2 HP-UX.

Table 4.5: HP-UX 11i v1.5 and v1.6 supported systems
List of supported systems might be incomplete.

Class	11i v1.5	11i v1.6
HP Itanium	i2000	i2000
HP Integrity rx	rx4610	rx2600, rx5670
HP Itanium zx		zx2000, zx6000
other	Probably many other Itanium systems supported	

The original HP Itanium i2000 workstations were apparently not supported in HP-UX versions newer than v1.6, thus had a short shelf-life of operating system support.

HP-UX 11i v1 (11.11)

The original HP-UX 11i release from 2000 supports most 64-bit PA-RISC systems and many older 32-bit servers and workstations. Some even older 32-bit PA-RISC systems were officially unsupported but could be made to work with some releases.

HP-UX 11.11, also called HP-UX 11i version 1, had different operating environments (OEs) for different PA-RISC computers which had specific support.

- ◇ Technical Computing Operating Environment (TCOE) for workstations
- ◇ Minimal Technical Operating Environment (MTOE) for workstations
- ◇ Mission Critical Operating Environment (MCOE) for servers
- ◇ Enterprise Operating Environment (EOE) for servers
- ◇ (Foundation) Operating Environment (OE) for servers
- ◇ all have the same Base OS Install common core

HP-UX 11i v1 was the last operating system for many PA-RISC workstations, which needed one of the two workstations versions TCOE or MTOE.

Table 4.6: HP-UX 11i 11.11 supported systems and OE, source: HP-UX 11i Release Notes

Class	Computers	HP-UX OE
HP 9000 700	712, some 715, some 725 (743i, 744, 745, 748i, 748)	TCOE, MTOE
Portables	RDI PrecisionBook, SAIC Galaxy 1100	TCOE, MTOE

HP Visualize	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600 C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3700, C3750, C8000 J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000	TCOE, MTOE
HP 9000 A-Class	A180, A180C, A400, A500	OE, EOE, MCOE
HP 9000 D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390	EOE, FOE, MCOE
HP 9000 K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580	OE, EOE, MCOE
HP 9000 L-Class	L1000, L2000, L1500, L3000	OE, EOE, MCOE
HP 9000 N-Class	N4000, N4000	OE, EOE, MCOE
HP 9000 R-Class	R380, R390	OE, EOE, MCOE
HP 9000 T-Class	T500, T520, T600	OE, EOE, MCOE
HP 9000 V-Class	V2200, V2250, V2500, V2600	OE, EOE, MCOE
HP Superdome	PA-RISC models	OE, EOE, MCOE
HP Integrity rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp4410, rp4440, rp5400, rp5450, rp5430, rp5470, rp7400, rp7405, rp7410, rp7420, rp7440, rp8400, rp8420, rp8440	OE, EOE, MCOE
<i>Not supported</i>	PA-7000/7100-based 705, 710, 715, 720, 730, 750, 725, 735, 755 PA-RISC 1.1 E-Class, Series 800 Nova Servers	

4.2.3 HP-UX 11.00

HP-UX 11.00 was the first 64-bit HP Unix, released in 1997, and ran on 32-bit and 64-bit PA-RISC computers. It supported most *lettered* servers and workstations plus some older HP 9000 700 and 800 systems. HP-UX 11.00 can run in either 64-bit or 32-bit mode. It had scant support for workstations in the original 1997 release developed by the HP Server division – later added with extensions to the OS.

Full 64-bit computing was defined by HP as a “64-bit CPU with 64-bit registers and data paths, 64-bit memory addressing, 64-bit Direct Memory Access, and a 64-bit kernel” required for “high-performance, resource-intensive applications, and applications such as databases and OLTP” that can use the scalability and memory addressing of 64-bit. HP-UX 11.00 was the first to support it on PA-RISC computers.

- ◇ Support for 64-bit computers in full 64-bit mode
- ◇ POSIX kernel threads, Message passing implementation (MPI), Performance optimized page size (POPS)
- ◇ Common internet file system (CIFS), Fibre channel for storage
- ◇ NFS v3.0, Java 2.0, Motif, X11R6 and CDE

HP-UX 11.00 supported many 64-bit workstations and most 32-bit PA-RISC workstations with at least

PA-7100LC CPUs. Support for HP 9000 servers was generally solid with only very old 1980s servers unsupported with not at least a PA-7000.

Table 4.7: HP-UX 11.00 supported systems with latest ACE and EP; * - unsure
source: HP-UX 11.00 Release Notes and ACE 9911 Release Notes

Class	Computers
HP 9000 700	712, some 715, some 725, 743i, 744, 745, 748i, 748
HP Visualize	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600 C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600 J200, J210, J280, J282, J2240, J5000, J5600, J6000, J7000
Portables	RDI PrecisionBook, SAIC Galaxy 1100
HP 9000 A-Class	A180, A180C, A400, A500
HP 9000 D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
HP 9000 E-Class	E25, E35, E45, E55
HP 9000 F/G/H/I	Series 800 Nova Servers (807-897)
HP 9000 K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
HP 9000 L-Class	L1000, L2000, L1500, L3000*
HP 9000 N-Class	N4000-36, N4000-44
HP 9000 R-Class	R380, R390
HP 9000 T-Class	T500, T520, T600
HP 9000 V-Class	V2200, V2250, V2500, V2600
HP Integrity rp	rp2400, rp2430, rp2450, rp2470, rp5400, rp5450, rp5430, rp5470*, rp7400, rp7410*
<i>Not supported</i>	PA-7000/7100-based 705, 710, 715, 720, 730, 750, 725, 735, 755 PA-RISC 1.0 early HP 9000 800 servers

In a similar vain to 32-bit HP-UX 10.20, there were Extensions Packs (EP) and Additional Core Enhancements (ACEs) that added support for hardware in HP-UX 11. Some 64-bit systems were only supported in 32-bit mode in original 11.00 from 1997, with 64-bit support added later.

- ◇ ACE 9911: Support added for full 3D graphics in 64-bit (?) and proper 2D and 3D graphics support for most Visualize adapters on workstations; (probably) B1000, B2000, C3000, C3600, J5000, J5600, J6000, J7000 workstations added; A-Class A400 and A500 servers added (or later); V2600 added (unsure); probably L1000/L2000 added
- ◇ EP 9905: Unsure what was added, probably N4000 servers and first support for “IA64 CEC” chipset – HP Stretch. Still no 3D workstations graphics supported.
- ◇ EP 9808: 64-bit support added for C160, C180, C200, C240, C360, J280, J282, J2240; V-Class
- ◇ Original 11.00 had some limitations: Graphics support in the original 11.00 release was severely limited. Many EISA adapters and older CRX-type graphics were *not* supported anymore in 11.00

or only in 32-bit versions

4.2.4 HP-UX 10

HP-UX 10 is the HP Unix operating system for 32-bit PA-RISC workstations and servers released by HP between 1995 and 1997. It had a short shelf-life due to fears of possible “Y2K bugs,” for which HP offered an upgrade path to HP-UX 11 and exchange CDs.

HP-UX 10 in its various guises supported almost all 32-bit HP 9000 700 series workstations, most lettered systems and most older HP 9000 800 servers. It was POSIX 1003.1 and 1003.2 and SVID3 compliant. HP-UX 10.01 was the last Unix to officially support older 1980s PA-RISC 1.0 computers.

HP-UX 10.20

HP-UX 10.20 was released in August 1996 as the HP Unix that supported almost all 32-bit PA-RISC workstations and servers. For HP-UX, 10.20 was pretty fast on supported machines with at least 64 MB RAM. It was discontinued by HP in 2002 and obsoleted in 2003 after shipping multiple releases.

- ◇ Support for 32-bit PA-7x00 processors and 64-bit PA-8x00 systems in 32-bit mode
- ◇ Large file size of up to 128 GB in HFS, JFS and LVM, Fibre Channel storage
- ◇ DHCP server and client
- ◇ Full X11R6, CDE graphical environment
- ◇ UNIX95 branded

Different HP-UX 10.20 releases were made for HP 9000 700 workstations and HP 9000 800 servers. Several extensions were shipped between 1997 and 1999 to add hardware support, most often through HP-UX Additional Core Enhancements (ACEs).

1. **HP 9000 Servers (10.20):** In July and August 1997, Hardware Extensions CDs were shipped to extend support for T600, K370, and K570 servers and improve fibre-channel (FC) support.
2. **HP 9000 Workstations (10.20):** Multiple Additional Core Enhancements (ACEs) were shipped to extend hardware support and add new features to 10.20:
 - ◇ ACE 9912: Add support for B2000, C3600, J5600, J6000, J7000, VISUALIZE-fxe, IDE CD drives, USB devices
 - ◇ ACE 9906: Add support for B1000, C3000, and J5000 workstations and USB; Euro, LVD SCSI, Super I/O
 - ◇ ACE 9806: Add support for C360 workstation, PCI Visualize-EG graphics, Visualize-fx hardware texture mapping, Y2K fixes
 - ◇ ACE 9804: Add support for J2240 workstations
 - ◇ ACE 9802: Add support for Visualize-EG 2D, fixes for Y2K compliance,
 - ◇ ACE 9707: Add support for OpenGL; B132L+, B180L, C200, C240 workstations, Ultra SCSI, 100 Base-T Ethernet, Visualize-FX
3. **HP 9000 Servers (10.30):** Released in 1997 with updates and enhancements to 10.20, HP-UX 10.30 focused on 800 Series servers. It added kernel (POSIX) threads, support for NFS version 3

(PV3), streams in TCP/IP, ASE, PPP and Y2K compliance. HP-UX 10.30 was “not intended” for workstations, discontinued in 1998 and obsoleted in 1999.

Generally, HP-UX 10.20 supported most 32-bit HP 9000 models. Hardware Enhancements bundles (HWE) were shipped with ACEs to support newer PA-8x00 based systems in 32-bit. Most HP graphics options, I/O devices and networking adapters integrated on HP 9000s were supported. Support for PA-RISC 1.0 and older servers was dropped.

Table 4.8: HP-UX 10.20 supported systems

Class	Computers
HP 9000 700	705, 710, 712, 715, 720, 730, 750, 725, 735, 755, 742i, 743i, 744, 745i, 745, 747i, 748i, 748
HP Visualize	C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, J200, J210, J280, J282, J2240, J5000, J5600, J6000, J7000
Portables	RDI PrecisionBook, SAIC Galaxy 1100
HP 9000 A-Class	A180, A180C
HP 9000 B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000
HP 9000 D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
HP 9000 E-Class	E25, E35, E45, E55
HP 9000 F/G/H/I	Series 800 Nova Servers (807-897)
HP 9000 K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
HP 9000 R-Class	R380, R390
HP 9000 T-Class	T500, T520, T600
HP Agilent	HP Agilent 16600A, 16700A, 16700B, 16702A, 16702B
<i>Not supported</i>	All PA-RISC 1.0 systems HP 9000 840, 822, 835, 850, 870, 890 and so on

HP-UX 10.10

HP-UX 10.10 was released in 1996 as feature-only release with few enhancements to HP-UX 10.00. It was discontinued by HP in 2000 and obsoleted in 2002.

New features and upgrades in HP-UX 10.10 included:

- ◇ CDE, the Common Desktop Environment GUI
- ◇ HP MC ServiceGuard
- ◇ HP Process Resource Manager
- ◇ Support for the HP Visualize graphics accelerators
- ◇ UNIX95 (SPEC 1170) branding

Supported hardware is unclear but probably the same as HP-UX 10.00. HP-UX 10.10 was the last stable OS release for several older Series 800 servers: 840S, 825S, 835S/SE, 845S/SE, 850S, 855S, 860S,

865S, 870S/x00, 822S, 832S, 842S, 852S, 890.

HP-UX 10.01

HP-UX 10.0 (or 10.01) was released in 1995, first as on-demand *New Business Release* (NBR) for new HP 9000 acquisitions and automatically shipped as *General Business Release* (GBR) for existing installations. There were different HP-UX 10 releases for workstations and server, discontinued in 2000 and obsoleted in 2003.

File system layout in HP-UX 10 was moved to a SVR4 (System V Release 4), which was “becoming a UNIX standard” in the 1990s. Software and licenses integrated into HP-UX included OSF Distributed Computing Environment (DCE), Streams and XTI over TCP/IP (“ARPA/9000”), NFS, NCS, X.11, Motif and HP VUE (Visual User Environment). HP-UX 10.0 was binary compatible from HP-UX 9.0.

New features and upgrades in HP-UX 10.0 included:

- ◇ Improvements to Symmetric Multi-Processor (SMP)
- ◇ Support for SMP in HP 9000 workstations
- ◇ Logical Volume Manager (LVM) software disk striping
- ◇ Journaled File System (JFS)
- ◇ Better I/O on 800 servers, Memory Mapped files and Dynamic Buffer Cache
- ◇ NFS version 4.2 and NFS booting support
- ◇ Focus on CD-ROM media for distributing HP-UX to move away from tapes (CD Now)

HP-UX 10.0 supported “all currently orderable HP 9000 Server and Workstation systems” and added support in the General Business Release for more systems.

Table 4.9: HP-UX 10.0 supported systems; * - in General Business Release

Class	Computers
HP 9000 700	705, 710*, 712, 715, 720, 730, 750*, 725, 735, 755, 742i, 743i, 745i, 747i, 748i
HP Visualize	C100, C110, J200, J210
HP 9000 800	Early HP 9000 800 servers* (PA-RISC 1.0)
HP 9000 E-Class	E25, E35, E45, E55
HP 9000 F/G/H/I	Series 800 Nova Servers (807-897)
HP 9000 K-Class	K-Class
HP 9000 T-Class	890, T500
<i>Not supported</i>	HP 9000 635, 645, 808 and 815, 825CHX, 825SRX, 834CH, 835SRX and so on

HP kept supporting HP-UX 9.0 in parallel to 10.0 due to the large installed HP-UX 9 userbase. When HP-UX 10.0 was released, HP supported new workstations and graphics in HP-UX 9.07 with a clear upgrade path. At HP-UX 10.01 discontinuance in 2000, HP recommended directly upgrading to 11.00

(and not 10.20).

HP-UX 10.0 was probably the last HP-UX to support early HP 9000 800 servers based on PA-RISC 1.0, though it is not totally clear which systems were supported.

4.2.5 HP-UX 9

HP-UX 9 was released between 1992 and 1994 and a popular and stable version of HP-UX for PA-RISC 1.0 and 1.1 32-bit 700 and 800 Series. There were different releases for workstations and servers, like in HP-UX 8 before: 700 Series workstations with odd release versions, 800 Series servers in even versions. HP-UX 9 included PA-7100 support, POSIX shell and graphical HP VUE 3.0 environment.

Last HP-UX 9 versions were discontinued in May 1998 and obsoleted, as HP-UX 9 was supposedly not “Y2K-ready” for the turn of the century. HP suggested an update to HP-UX 10.20 to ensure “proper system operation in the Year 2000”. HP-UX 9 was supposedly the last strongly BSD-based HP Unix before switching to System V in 10.x

Most HP-UX 9 and earlier versions were released prior to the “Web” -era of HP technical information so definite documentation is a bit hard to come by.

Table 4.10: HP-UX 9 supported systems, with some uncertainties

Class	Computers	Versions
HP 9000 700	705, 710, 715, 720, 730, 750, 725, 735, 755 (99), 742i, 745i, 747i	9.01, 9.03, 9.05, 9.07
HP 9000 700	712, 715, 735, 755 (125), 743i, 748i	9.05, 9.07
HP Visualize	C100, C110, J200, J210 [^]	9.07
HP 9000 800	Early HP 9000 800 servers (PA-RISC 1.0)	9.00, 9.02, 9.04, 9.06
HP 9000 E-Class	E25, E35, E45, E55	9.04?, 9.06
HP 9000 F/G/H/I	Series 800 Nova Servers (807-897)	9.00, 9.02, 9.04, 9.06
HP 9000 T-Class	890, T500 (unsure)	9.00, 9.02, 9.04, 9.06

HP-UX 9 for Workstations

HP-UX 9 was the second HP-UX release for PA-RISC workstations and supported most HP 9000 Series 700 workstations. The first HP-UX 9 version apparently supported PA-7000 705, 710 and 720, 730, 750. There were multiple HP-UX 9 minor versions:

HP-UX 9.01 was released in 1993 and added hardware support for PA-7100-based 725 and 735, 755 workstations and 742i, 745i and 747i VME boards Also supported were PA-RISC upgrades for Motorola 68000-based 425s and 425t, 1GB, 2GB and 525MB SCSI drives, CRX48Z graphics and JIS (Japanese) keyboards.

HP-UX 9.03 was released in 1993 for several newly released HP hardware, including PA-7100LC 712 workstation, floppy-disk support (SCSI?), device drivers for LASI chipset, and more. Software-wise, HP-UX 9.03 enhanced support for BOOTP and TFTP, “smart shutdown”, changes to SAM cluster configuration, and reduced the kernel and base OS footprint.

HP-UX 9.05 was released in 1993 and was primarily a hardware release that added support for 32-bit PA-7100LC 715 and 725 and PA-7150 735, 755 workstations. VME workstations 743i and 748i are also supported with 9.05. Additional support was added for HCRX graphics, 1GB half-height SCSI and 2GB SCSI drives.

HP-UX 9.07 was released in 1993 and added hardware support for the PA-7200 J200, J210 and possibly C100, C110 workstations and multi-buffered X11.

HP-UX 9.09 was released in 1994 and probably not widely shipped. It supposedly was a “B-level Security release” with very strict security controls (mandatory security). These B1 versions were separate products parallel to “other” HP-UX releases.

HP-UX 9 for Series 800

The separate product stream of HP-UX 9 for servers started with version 9.00 in 1992, which included support for new PA-7100 servers. For these HP-UX 9 server versions, only very scant information remains.

HP-UX 9.00 was released in July 1992 and added support for PA-7100 processors, a POSIX shell, VUE 3.0, fastlinks and ioscan(1) and model(1) commands plus the Logical Volume Manager (LVM) for disk management.

HP-UX 9.02 was released in 1993 and added hardware support.

HP-UX 9.04 was released in November 1993, discontinued by HP in 1997 and obsoleted at the end of 1998. It also added hardware support.

HP-UX 9.06 was supposedly released in 1994 but it is not clear if it was a released product or internal version (plan).

HP-UX 9.08 was released in 1994 and probably not widely shipped. It supposedly was a “B-level Security release” with very strict security controls (mandatory security). These B1 versions were separate products to “other” HP-UX 9 releases.

4.2.6 HP-UX 8

HP-UX 8 is HP’ Unix operating system for 32-bit PA-7000 and PA-7100 computers, released in 1991. The codebases for workstations and servers were different in HP-UX 8 with separate releases for workstations (odd version numbers) and servers (even versions).

HP-UX 8 was the first HP-UX to support SMP multiprocessing, in server versions starting with HP-UX 8.06.

Table 4.11: HP-UX 8 supported systems, with some uncertainties

Class	Computers	Versions
HP 9000 700	720, 730, 750	8.01, 8.05, 8.07
HP 9000 700	705, 710	8.07
HP 9000 800	Early HP 9000 800 servers (PA-RISC 1.0)	8.00, 8.02, 8.06
HP 9000 F/G/H/I	Series 800 Nova Servers (807-897)	8.02, 8.06

HP-UX 8 for Workstations

In 1991 and 1992, first HP 9000 700 workstations based on PA-RISC 1.1 PA-7000 CPUs were released. HP-UX 8 was the first HP-UX for these workstations.

HP-UX 8.01 was released in 1991 and “only sold to developers to create/test programs.” It supported the HP 9000 720, 730 and 750 workstations, with other hardware support unclear.

HP-UX 8.05 was released in July 1991, “a partial release, not considered complete and documented as interim at the time of shipments.” Supported systems again included the HP 9000 720, 730 and 750 workstation systems.

HP-UX 8.07 was released in January 1992 as final 8.0 release for workstations and supported the new HP 9000 705, 710 and 720, 730 and 750 systems. Hardware support was added for CRX, CRX-24, Dual-CRX, CD-ROM, 2.0GB drives, EISA cards (X.25, 802.5, FDDI), DDS tape drives. Software support was added for AAPI audio API

There might have been a “Trusted Systems” HP-UX 8.09 version with B1 security.

HP-UX 8 for Servers

HP-UX 8 supported many original PA-RISC server systems in the HP 9000 800 series.

HP-UX 8.00 was released in January 1991. Not much more information is findable these days other than it supporting some (most?) older HP 9000 800 servers.

HP-UX 8.02 was released in April 1992 and was rewritten to work on the new, lettered HP 9000 800 Nova servers – the F, G, H and I-Class (8x7).

HP-UX 8.06 was released in 1992 as HP-UX 8.0 with additional code to handle multiple processors in HP 9000 870 with up to four PCX processors.

HP-UX 8.04 and HP-UX 8.08 were released in 1991 and 1992 and were described as “security versions of 8.0 without additional hardware or software support.”

4.2.7 Older HP-UX

Unix and HP-UX were the standard operating systems when HP developed PA-RISC and the HP 9000 family. Many older HP-UX Unix versions were released in the 1980s for the many HP product families of the time.

As HP-UX in the 1980s preceded the internet age with digital documentation, not much information is left of these early versions.

Releases of early HP-UX were architecture-specific and versioning and numbering not very coherent: In 1988, HP-UX 3.0 for PA-RISC was released in parallel to HP-UX 6.0 for Motorola 68000. This confusing versioning was only mitigated in HP-UX 7.

HP-UX 7

HP-UX versions 7 were released from 1989 to 1990, mostly for Motorola 68000 systems. Apparently, HP-UX 7.03 supported PA-RISC systems in some way, probably the 800 Series servers. There is not much verifiable information on this though.

HP-UX 3

HP-UX 3.0 was released in 1988, in parallel to the 68000-specific HP-UX 6.0, it supported (apparently) at least HP 9000 825, 835 and 850. The 3.x versions of HP-UX were apparently PA-RISC-only releases for early 800/600 Series servers.

Sources from 1989 mention several “nasty bugs” in an HP-UX 3.01 release on the 850 server. It also supported an HP implementation of X11.

HP-UX 2

HP-UX 2, released in 1987, was either the first or second release for the PA-RISC Series 800 servers. It apparently supported the first HP 9000 840 and other early HP 9000 825, 835 and 850 servers. There were at least HP-UX 2.0 and HP-UX 2.1 releases for PA-RISC 1.0 systems, strongly BSD-influenced, that also supported “workstation” 825 and 835 with graphics hardware — when server 800s were marketed as 635SV and 645SV for a (confusing) time.

HP-UX 1

Some sources mention a HP-UX 1.0 as being the first HP-UX for PA-RISC HP 9000 840, released in 1986. This HP-UX was supposedly strongly BSD-based, in contrast to the AT&T HP-UX 1.0 for Series 500. Since versioning and naming was in flux during that time, maybe it was a pre-release of the product that became HP-UX 2.0, bundled with first 840 servers.

Other HP-UX

The really first HP-UX 1.0 was released in 1983 for the HP FOCUS and was supposedly very different to other HP-UX versions, based on an AT&T kernel. There was even another HP-UX 1.0 in 1984 for the HP Integral “PC” (on ROM) before 1.0 for PA-RISC in 1986.

HP-UX 5.0 was released in 1985 and supported Motorola-based Series 200 and 300 as well as FOCUS HP 9000 500, for which it was the last supported HP-UX (5.3). HP-UX for FOCUS 500 Series was the first commercial UNIX supporting multi-processor, multi-user systems in the early 1980s. SMP for PA-RISC was supported only much later in HP-UX.

HP-UX 6.0 from 1986 was for Motorola 68000, before unifying with PA-RISC in 7.0.

4.2.8 Documentation

Most of the documentation and references disappeared during the 2010s from the web. Much information has been gleaned from (slowly disappearing) USEnet postings from the 1980s and early 1990s in comp.sys.hp.hpux, especially for older versions of HP-UX. For a while now, archive.org has a growing list of HP-UX documentation.

Software

- ◇ Software Porting And Archive Centre for HP-UX, compiled software packages for HP-UX
- ◇ The Written Word FTP, 32-bit packages for HP-UX 11.00 (URL gone)

- ◇ The Written Word FTP, 32-bit packages for HP-UX 11.11 (URL gone)
- ◇ The Written Word FTP, 64-bit packages for HP-UX 11.23 (URL gone)
- ◇ HP Software Depot, HP website with HP-UX software packages

Manuals

- ◇ HP-UX 11i Version 1 Installation and Update Guide: HP Servers and Workstations Hewlett-Packard Company (June 2004, HP 5990-7279) **mirror**
- ◇ Installing HP-UX 11.0 and Updating HP-UX 10.x to 11.0: HP 9000 Computers Hewlett-Packard Company (November 1997, HP B2355-90153)
- ◇ Installing and Updating HP-UX 10.20, ACE and Hardware Extensions: HP 9000 Computers Hewlett-Packard Company (April 1998, B2355-90173) **bitsavers**
- ◇ Installing and Updating HP-UX 10.x HP 9000 Computers **bitsavers**

Websites

- ◇ HP-UX 11i versions and their lifecycle dates, support matrix, Hewlett-Packard (2009)
- ◇ HP-UX server support matrix (HP-UX 11.x support for servers) Hewlett-Packard Enterprise (2024)
- ◇ HP-UX update matrix (HP-UX 10.20 and 11.x support for workstations) Hewlett-Packard Development Company (2003: accessed March 2009)
- ◇ HP-UX version and server model support matrix (HP-UX 11 support for servers) Hewlett-Packard Company (2001: accessed April 2009)
- ◇ *Building a Bastion Host Using HP-UX 11*, Kevin Steves (April 2000: Hewlett-Packard)
- ◇ docs.hp.com - Technical documentation, good entry to HP-UX documentation
- ◇ hp-ux history, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ Support Matrix - HP-UX Workstations Processors, OS Versions and Graphics, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ HP-UX 11.11 and 11.23 Operating Environments, presentation HP World 2003

Release notes

- ◇ HP-UX 11i v3 Release Notes
- ◇ HP-UX 11i v2 Release Notes (from 2010. Original: docs.hp.com)
- ◇ HP-UX 11i v1.5 Release Notes (from docs.hp.com)
- ◇ Release Notes for HP-UX 11.0: HP 9000 Computers, Hewlett-Packard 1998
- ◇ hp-ux operating system releases, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ HP-UX 10.0 Overview, Hewlett-Packard Company (2002: mirror accessed January 2024)

- ◇ HP-UX 10.0 Supported Hardware and Software, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ HP-UX 10.30 and 10.20 Operating System Introduction Plan, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ HP-UX 10.20 Hardware Systems Supported, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ hp-ux 11.0 overview & features, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ Release Notes for HP-UX 11.0 Extension Pack, May 1999, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ Exploring HP-UX Releases and Media, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ Exploring HP-UX Releases and Media, Hewlett-Packard Company (1998: mirror accessed January 2024)

Other documents

- ◇ HP-UX FAQ (comp.sys.hp.hpux FAQ) Ian Springer (February 2008: accessed January 2024 on faqs.org)
- ◇ INFORMATION ON HP9000 SERVERS AND WORKSTATIONS Hewlett Packard Company (1997 (1999): accessed January 2009)
- ◇ HP Delivers 64-Bit HP-UX Operating System on HP VISUALIZE Workstations, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ Much information has been gleaned from many USEnet postings in comp.sys.hp.hpux, especially on the older versions, from between 1988 and 1998
- ◇ HP Developer Resource Document Library, Hewlett-Packard Company (1999: mirror accessed January 2024)
- ◇ ACE Software Archive, software.hp.com , Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ hp-ux 11.0 operating system, technical documentation , Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ 64-Bit Computing and the HP-UX 11.00 Operating Environment, HP Software, Hewlett-Packard Company (2000: mirror accessed January 2024)

Pictures Hewlett Packard, scans from product brochures, from hpmuseum.net and 100obit.it

4.3 NeXTSTEP on PA-RISC

4.3.1 Overview

NeXTSTEP is a Unix operating system based on Mach microkernel with an advanced GUI, developed in the 1980s and 90s by NeXT. NeXTSTEP supported PA-RISC computers in release 3.3 from 1994 in an effort to open up the operating system to other hardware platforms like HP PA-RISC, SPARC and Intel x86.

The PA-RISC version of NeXTSTEP 3.3 was developed on and specifically for the HP 9000 712 pizzabox workstation, a very fitting combination of the 1990s with a very nice user experience.

Introduced in 1989 by NeXT, NeXTSTEP featured development and user environments, an unique GUI and the Display Post Script (DPS) display system. The operating system core is a Mach microkernel, 4.3BSD compatible and runtime-extensible.

In its early years, NeXTSTEP only ran on NeXT “black hardware”, sophisticated and expensive custom NeXT designs based on Motorola 68000, the sleek NeXT cubes. In 1991 “white hardware,” Intel x86 PC, was supported in NeXTSTEP 3.1 to open up the operating platform.

Development continued and in 1994 NeXTSTEP 3.3 was released with support for different RISC platforms including Sun SPARC and HP PA-RISC. Support for PA-RISC in NeXTSTEP was only brief and limited to a select set of 32-bit HP 9000 workstations.

NeXTSTEP itself, while revolutionary in aspects, did not have long commercial success. However some of its ideas and technologies live on in Mac OS, after corporate M&A and consolidation in the tech sector.

4.3.2 Systems support

NeXTSTEP runs on some HP 9000 700 PA-RISC workstations of the 1990s with 32-bit processors like PA-7100 or PA-7100LC with ASP or LASI designs:

Class	Supported omputers
HP 9000 700	712, 715, 725, 735, 755
Portables	probably SAIC Galaxy 1100

NeXTSTEP ran very well on HP 9000 712 workstations and provided a unique operating system experience for the 1990s with Unix-like OS and a slick GUI on top. NeXT on PA-RISC was actually developed on 712 workstations.

HP 9000 735/125 were the fastest RISC workstations that ran NeXTSTEP in the 1990s.

4.3.3 Hardware support

NeXTSTEP 3.3 supports most standard hardware of supported PA-RISC workstations:

- ◇ Storage required between 400 MB for a user environment to 700 MB for complete developer environment
- ◇ 32 MB to 64 MB RAM required, with a maximum of 256 MB supported

- ◇ All onboard graphics and CRX and CRX-24 supported
- ◇ HCRX and HCRX-24 graphics supported after installation of NeXTSTEP 3.3 patches
- ◇ Onboard SCSI controllers for storage
- ◇ PS/2 keyboards only on 712 and 715/64, 80 and 100 workstations, no HIL
- ◇ HIL keyboards on all other systems
- ◇ **Unsupported** on 735/755 are FWD (Fast/Wide Differential) SCSI and FDDI

4.3.4 Documentation

Manuals

- ◇ NeXTstep 3.3 Network and System Administration Manual, NeXT Software Inc. 1994, mirrored at NeXTComputers.org, accessed December 2019
- ◇ NeXTstep 3.3 Developer Documentation Manuals, NeXT Software Inc. 1994, mirrored at NeXTComputers.org, accessed December 2019

Articles

- ◇ The NEXTSTEP/OpenStep FAQ, Bernhard Scholz 1996, mirrored at levez.com, accessed December 2019
- ◇ First NeXT RISCWorkstation: Our first look at NEXTSTEP on HP's low-cost pizza box, NeXTWORLD, April 1994
- ◇ NeXTstep on the HP 712 Part 1: Installation, Sophie Haskins, Pizza Box Computer, 2020
- ◇ <https://blog.pizzabox.computer/posts/hp712-nextstep-part-2/>, Sophie Haskins, Pizza Box Computer, 2020

Software

There used to be a large software archive available at the Peanuts.org FTP server. It went offline about 2004-2005, without a known mirror. Other than that there is not much software available, other than contemporary open source or shareware.

- ◇ NeXTSTEP Current Patch List (.pdf) Apple Computer 2006, mirrored at NeXTComputers.org, accessed 8 January 2009
- ◇ NeXTSTEP 3.3 “User” patch NS33RISCUserPatch3.tar and release notes NeXTSTEP 3.3 Patch 3 Overview (.pdf) Apple Computer 2006, mirrored at NeXTComputers.org, accessed 8 January 2009
- ◇ NeXTSTEP 3.3 “Developer” patch NS33DeveloperPatch2.tar

4.4 PA-RISC Linux

4.4.1 Overview

PA-RISC Linux runs on a broad range of 32-bit and 64-bit HP 9000 PA-RISC workstations and servers. The port was supported by HP and a few research initiatives for a while and is the most complete open source PA-RISC operating system, having been developed for now more than 25 years. Two major Linux distributions include PA-RISC in their releases and codebase: Debian and Gentoo.

In the late 1990s, PA-RISC was the last “big” RISC/Unix architecture without a proper Linux port. Early work by the Puffin Group in 1998 on the port of Linux to HP PA-RISC gained momentum after HP started helping with equipment and documentation in 1999. It quickly superseded the earlier Mach-based MkLinux. Because of HP’s assistance, supported machines at the time were newer than other ports like OpenBSD or Mach, such as HP 9000 A180, Visualize B180 and 64-bit PA-RISC 2.0.

Since the late 2000s, work on the PA-RISC Linux port became slower, similar to other open source operating systems on PA-RISC, but the tempo increased in 2014 again. Most PA-RISC Linux documentation and websites changed and moved in the 2020s.

4.4.2 Systems support

Most HP 9000 700 and B/C/J-Class workstations are supported with 32-bit and 64-bit PA-RISC processors. SMP multi-processing is supported, though not as smooth as other Linux platforms or HP-UX. Linux runs also on many HP 9000 PA-RISC server systems, although some proprietary I/O, CPU and memory are not supported.

Table 4.13: PA-RISC Linux supported systems

Class	Computers
HP 9000 700	705, 710, 712, 715, 720, 730, 750, 725, 735, 755
HP 9000 740 VME	742i, 743i, 744, 745i, 745, 747i, 748i, 748
HP 9000 A-Class	A180, A180CA400, A500
HP Visualize B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
HP Visualize C-Class	C100, C110, C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3700, C3750, C8000
HP 9000 D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
HP 9000 E-Class	E25, E35, E45, E55 (very limited)
HP Visualize J-Class	J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000, J7600
HP 9000 K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
HP 9000 L-Class	L1000, L2000, L3000
HP 9000 N-Class	N4000
HP 9000 R-Class	R380, R390
HP Integrity rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp5400, rp5450, rp5470, rp7400
Portables	RDI PrecisionBook, SAIC Galaxy 1100

Performance on Linux is not quite on par with original HP-UX — 50% was a rough estimate in the late-2000s. However the overhead of running a full-blown HP-UX probably consumes much of this

advantage, especially on older systems.

4.4.3 Hardware support

Most I/O subsystems are supported in PA-RISC Linux, including many common PC expansion options. Correct X11 graphical support is limited to a small set of HP adapters via the framebuffer device. As newer machines are more similar to standard Intel PCs, support is generally better but still lacking in some areas.

Distributions

The center of kernel and toolchain development is the official PA-RISC Linux project with source code, mailing lists, install instructions, an array of documentation and a hardware database. Two Linux distributions have included the PA-RISC port since the 2000s: Debian and Gentoo:

- ◇ Debian included PA-RISC Linux from 2002 until 2012 as Debian/hppa in various releases from 3.0 to 4.0. The Debian version of PA-RISC Linux is available in the Debian ports repositories where regular installation medias are made available as hppa in various releases
- ◇ Gentoo is the second Linux distribution that included a PA-RISC port.
- ◇ T2 System Development Environment includes Linux PA-RISC support.

4.4.4 Documentation

- ◇ PA-RISC Linux: HARDWARE SUPPORT PA-RISC Linux Porting Project (2024)
- ◇ PA-RISC LINUX FAQ PA-RISC Linux Porting Project (2024)
- ◇ ESIEE PA/Linux Detailed Hardware Support ESIEE The PA/Linux Team (2016)
- ◇ PA-RISC Linux hardware database, The PARISC-Linux Project (gone)
- ◇ PA-RISC Linux project page PA-RISC Linux Porting Project (2024)
- ◇ PA-RISC Linux Project History and Early Development, PA-RISC Linux Porting Project (October 2022)

Articles

- ◇ Linux on PA-RISC. One Martini Too Many (.pdf) Matthew Wilcox (July 2000: Paper for OLS2000)
- ◇ Debian-ports repositories, including PA-RISC port as hppa (Debian.org, accessed 2022)
- ◇ HP: OPEN SOURCE GROUP; PUFFIN DOES LINUX ON PA-RISC, Computergram International, February 23, 1999 (archived at CBR/Techmonitor)

4.5 NetBSD/hppa

4.5.1 Overview

NetBSD is a free, open source Unix-like operating system with support for 32-bit PA-RISC computers in NetBSD/hppa, a “Tier II” port.

The NetBSD port to PA-RISC focuses on 32-bit computers and 64-bit systems in 32-bit. It is largely based on Michael Shalayeff’s work on OpenBSD/hppa from 1999 to 2005 and some updated OpenBSD code later on. NetBSD supports PA-RISC since around 2005, called NetBSD/hp700 until the 7.0 release.

Similar to OpenBSD/hppa, it seems usage of and interest in NetBSD on PA-RISC has declined significantly since the 2000s. Even though NetBSD provides a modern Unix user experience, running PA-RISC might not be as smooth as before.

4.5.2 Systems support

NetBSD describes the following systems as supported (in the 9.2 release, as of 2021), unsure if all are completely supported and tested.

Table 4.14: OpenBSD/hppa supported systems* - in 32-bit mode

Class	Computers
HP 9000 700	705, 710, 712, 715, 720, 730, 750, 725, 735, 755
HP 9000 740 VME	742i, 743i, 744, 745i, 745, 747i, 748i, 748
HP 9000 A-Class	A180, A180C
HP Visualize B-Class	B132L, B160L, B132L+, B180L+, B1000*, B2000*, B2600*
HP Visualize C-Class	C100, C110, C132L, C160L, C160*, C180*, C200*, C240*, C360*, C3000*, C3600*, C3700*
HP 9000 D-Class	D200, D210, D220, D230, D300, D310, D320, D330
HP 9000 E-Class	E25, E35, E45, E55 (apparently, and with serial console only, without SCSI)
HP Visualize J-Class	J200, J210, J280*, J282*, J2240*, J5000*, J5600*, J6000*, J6700*, J6750*, J7000*, J7600*
HP 9000 K-Class	K100, K200, K210, K220, K400, K410, K420
Portables	RDI PrecisionBook, SAIC Galaxy 1100

4.5.3 Hardware support

Processors

Supported are 32-bit PA-RISC 1.0 PA-7000, PA-7100, PA-7100LC, PA-7200 and PA-7300LC processors. Also, some systems with 64-bit processors are supported in 32-bit mode: PA-8000, PA-8200, PA-8500, PA-8600 and PA-8700.

Buses and chipsets

Most PCI, GSC and Runway buses and onboard bus controllers are supported.

Networking

On-board Ethernet and Fast-Ethernet network interfaces are supported; the FDDI sliders on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel i8255x, Realtek 8120/8139, NE2000, SiS 900) could work.

Realtek RTL8150L USB-based Ethernet adapters are supported.

Storage

Storage I/O is supported via NCR 53C700 narrow, NCR 53C710 Fast-Narrow or NCR 53C875 Ultra-Wide SE SCSI controllers. On-board NCR 53C720 Fast-Wide HVD controllers are not supported.

GSC/HSC and PCI expansion cards with one of the 53C710 or 53C8xx (siop) SCSI chipsets, Adaptec 2940 (ahc) PCI and various Qlogic ISP PCI SCSI adapters should also work, however not necessarily for booting.

Graphics

SGC graphics (framebuffer).

It seems with NetBSD 11.0 in 2024, more graphics drivers were added: PCI Visualize EG card, HCRX video cards and an X.Org (X11) driver for Visualize EG.

Human I/O

Human I/O is supported via PS/2 and HIL.

Misc

Several PCI USB adapters from VIA and ALi have been tested and are known to work; they support USB mass-storage and Ethernet devices. The onboard Harmony audio system is supported.

4.5.4 Documentation

Manuals

- ◇ INSTALL Installation procedure for NetBSD/hppa, release 10.0, NetBSD (2024)

Websites

- ◇ NetBSD/hppa official port page, NetBSD (November 2024)

Software

- ◇ NetBSD/hppa 10.0 (November 2024) cdn.netbsd.org

4.6 OpenBSD/hppa

4.6.1 Overview

OpenBSD is an open source BSD Unix-like operating system, that was ported to HP PA-RISC computers in 32-bit during the 2000s. OpenBSD/hppa supports most on-board components and HP expansion options in supported systems, with significant support for generic/third-party devices and newer open source software.

OpenBSD provides a rather modern Unix userland on PA-RISC. However, OpenBSD/hppa development slowed down around 2008-2009, as did other open-source PA-RISC systems. It seems interest in and usage of OpenBSD/hppa port has declined in the community since the 2010s. PA-RISC Linux might be more stable.

NetBSD/hppa is heavily based on OpenBSD/hppa.

4.6.2 Systems support

Table 4.15: OpenBSD/hppa supported systems* - in 32-bit mode

Class	Computers
HP 9000 700	705, 710, 712, 715, 720, 730, 750, 725, 735, 755
HP 9000 740 VME	742i, 743i, 744, 745i, 745, 747i, 748i, 748
HP 9000 A-Class	A180, A180C
HP Visualize B-Class	B132L, B160L, B132L+, B180L+, B1000*, B2000*, B2600*
HP Visualize C-Class	C100, C110, C132L, C160L, C160*, C180*, C200*, C240*, C360*, C3000*, C3600*, C3700*
HP 9000 D-Class	D220, D230, D320, D330
HP Visualize J-Class	J200, J210, J280*, J282*, J2240*, J5000*, J5600*, J6000*, J6700*, J6750*, J7000*, J7600*
HP 9000 K-Class	K100, K200, K210, K220, K400, K410, K420
Portables	RDI PrecisionBook, SAIC Galaxy 1100

Unsupported are PA-RISC 1.0 systems and older HP 9000/800 servers like Nova, E-Class and older systems. In doubt are some newer 64-bit server systems with **rp** designations due to their chipsets and I/O systems.

As of 2024, OpenBSD/hppa does not properly boot on QEMU PA-RISC emulator. Installation works but booting the installed system crashes.

4.6.3 Hardware support

Processors

Supported are 32-bit PA-RISC 1.1 processors: PA-7000, PA-7100, PA-7100LC, PA-7200 and PA-7300LC. Some 64-bit PA-RISC processors are supported in 32-bit mode: PA-8000, PA-8200, PA-8500, PA-8600 and PA-8700.

Up to 2 GB of memory is supported.

Buses and chipsets

All PCI, GSC and Runway buses and onboard bus controllers such as ASP, LASI, Dino/Cujo, U2/Uturn, Astro and Elroy on the listed systems are supported. Additionally, Yenta-compatible PCI-Cardbus bridges are supported, as for instance found on the RDI Precisionbook.

ISA, EISA and HP-PB, VME buses and controllers are not supported.

Networking

On-board Ethernet and Fast-Ethernet network interfaces on the above machines are supported, FDDI on the 735/755 are not supported.

Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet chipset, like Intel i82596, DEC 21142/43 *Tulip*, Intel EtherExpress PRO/10 and PRO/100 series, Intel Gigabit chipsets, in various incarnations for the PCI bus, NE2000-compatible, 3Com 3c9xx EtherLink XL, should also work.

PCMCIA and to a lesser extent Cardbus devices are supported in a compatible PCI-Cardbus bridges, including various WLAN and Ethernet cards.

Storage

Storage is supported on NCR 53C700 Narrow, NCR 53C710 Fast-Narrow, NCR 53C720 Fast-Wide HVD/differential or the NCR 53C875 Ultra-Wide SE SCSI controllers.

GSC/HSC and PCI expansion cards with 53C7x0 or 53C8xx SCSI chipsets and Adaptec 2940 PCI SCSI adapters should also work, though are not necessarily bootable.

Various newer PCI SCSI controllers based on Adaptec AHA and LSI Fusion-MPT chipsets are also supported, though not bootable.

Graphics

All on-board graphics adapters are supported for text-mode via STI routines, similar to PC VGA BIOS. Additionally, Artist graphics, CRX, CRX-24, HCRX-8, HCRX-24, Visualize-EG and Visualize-FX (FX2, FX4 and FX6) graphics expansion boards on GSC and PCI are supported.

X11 graphics capabilities are apparently working, in some way, since April 2015.

Human I/O and multimedia

Input/output is supported via PS/2 or HIL on-board interfaces, though not all HIL devices are supported.

Various USB devices are supported, including networking adapters and I/O devices attached to expansion USB controllers, PCMCIA/PCI.

“Harmony” 16-bit audio, found on many PA-RISC workstations, is supported.

4.6.4 Documentation

Websites

- ◇ OpenBSD/hppa official page, OpenBSD (October 2023)
- ◇ Discontinued OpenBSD/hppa64 official page, OpenBSD (2019. Accessed 2020)

Software

There might be newer OpenBSD/hppa versions than listed below.

- ◇ OpenBSD/hppa 7.4 release (October 2023) ftp.openbsd.org
- ◇ OpenBSD/hppa snapshots ftp.openbsd.org
- ◇ Packages for add-on software see OpenBSD: Getting Packages
- ◇ Software is available through the OpenBSD Ports tree, a framework for open source software.

Manuals

- ◇ INSTALL.hppa (snapshot) installation instructions, OpenBSD (2020)
- ◇ INSTALL.hppa (7.4 release) installation instructions, OpenBSD (2023)

Other documents

- ◇ Michael Shalayeff: OpenBSD on PA-RISC talk NYCBUG (2007: NYCBUG 2005 talk. Accessed January 2009)

4.7 Mach on PA-RISC

4.7.1 Overview

Several ports of Mach microkernel operating systems to PA-RISC were developed between the 1980s and 1990s. Mach on PA-RISC was developed mainly at the University of Utah and in HP research projects but was also commercialized in products like SPP/UX and NeXTSTEP.

The University of Utah was a center of PA-RISC operating system research in the 1990s, Mach was ported in Utah to PA-RISC with Mach 3 in 1991 and Mach 4 in 1994, both of which were developed in parallel to the more conservative HPBSD port.

Mach was commercialized for workstations eventually with NeXTSTEP on PA-RISC in 1994 and later Mac OS X, itself based on Mach and influences from NeXTSTEP. SPP-UX, the Unix variant for Convex Exemplar scalable computers was based on Mach. Interest in Mach died down after the 1990s and ports were succeeded by open source projects in the early 2000s, which borrowed from their code and documentation.

4.7.2 Mach 3

The Mach 3 port to PA-RISC was called Mach 3/UX, developed by Bob Wheeler of the University of Utah around 1991. It was one of the first various Mach microkernel ports to PA-RISC. This port was supposed to accomplish what the previous, HP-internal HP Tut project aimed for — a proper port of Mach to PA-RISC. The sole target system was the HP 9000/835 server.

Ported was the Mach 3 microkernel with a proof-of-concept AT&T Unix System V kernel (personality) running as user-level server, with the Unix part originally done by CMU. Mach 3/UX never got very far, but code wound up later in Mach 4/Lites and probably MK-PA from OSF. There were no public releases known.

There was apparently another, separate University of Utah research project for OSF/1 on PA-RISC with a Mach 3.0 microkernel and OSF/1 1.0.4 server used for threading research.

4.7.3 Mach 4/Lites

The University of Utah ported the original Mach microkernel with a 4.4BSD-Lites server on top, released as **Mach 4/Lites**. It was based on the work of the Mach 3/UX project and developed and first released in 1994. It took the Mach microkernel with a Unix “server” on top — in this case Lites for 4.4BSD Unix.

The Unix which runs on top of the Mach kernel is Lites, an 4.4BSD-lite Berkeley Unix operating system personality provided by the Lites server/emulator. Lites is a user-mode, single-task implementation of BSD Unix which runs on top of a Mach micro-kernel, developed at Helsinki University of Technology (HUT) in Finland.

Mach 4/Lites was the mid-1990s public and freely available offspring of earlier, closed efforts of OSF/1 from the Open Group and HPBSD from the University of Utah. It was never a fully functional operating system and more of a coding and research project, meant to open source Mach and PA-RISC developments.

Supported hardware

Mach 4/Lites supported PA-RISC 1.1 HP 9000/700 workstations from the early to mid-1990s. In addition, there are several other PA-RISC-related device drivers, kernel components and utilities and a fairly complete 4.4BSD-lite user environment.

- ◇ HP 9000 705, 710, 720, 730, 750 based on PA-7000 processors
- ◇ HP 9000 715, 725, 735, 755 based on PA-7100 processors
- ◇ HP 9000 712 (with serious issues) and 715 based on PA-7100LC processors
- ◇ Devices: Internal single-ended and fast-wide different SCSI drives and tapes, RS232 serial, builtin Ethernet, GRX and CRX graphics, Artist on 712/715 (probably), HIL and PS/2 keyboard/mouse
- ◇ Unsupported: FDDI networking, EISA expansion cards and devices, parallel ports, audio, tele-share port on 712, floppy drives and all other hardware

Releases

Mach 4/Lites was released in Alpha status with freely distributable source, binaries, and boot images. This was for a complete Mach kernel that includes some of Utah's operating system research, the Lites BSD-based single-server, include directories and libraries, and a complete GNU toolchain for the ELF object format.

The following "releases" were available as source from FTP mirrors.

- ◇ **Mach 4/Lites (alpha)**: Support for few PA-RISC 1.1 workstations (1994)
- ◇ **Mach 4/Lites (snapshot2)**: Fixes for HP-UX compatibility for Netscape 1.2, with some late break-age in newer systems (1995)
- ◇ **Mach 4/Lites (snapshot3)**: probably released but not sure (1995)

Source of Mach 4/Lites were used extensively in newer BSD operating systems such as OpenBSD/hppa during their early development. The entire Mach 4/Lites system was self-built on Mach 4/Lites. Sources and binary releases are still available at mirrors, although performance and stability can be lacking.

4.7.4 SPP-UX

The Exemplar Operating System, SPP-UX, was a scalable Unix based on Mach developed by Convex for its SPP1000 and SPP2000 mainframe computers with up to 128 or 512 processors. SPP-UX implemented a distributed architecture that was supposed to look like (emulate) HP-UX for developers but was very different below the userland. It probably was released between 1993 and 1999?

The SPP-UX kernel and architecture was based on a Mach 3.0 distributed microkernel and was taken over by HP during the acquisition of Convex and its Exemplar SPP computers. Each hypernode of the SPP computers ran an independent instance of the Mach microkernel. There were three (four) main layers for SPP-UX:

1. **Distributed kernel**: Based on an enhanced Mach 3.0 microkernel, supposedly OSF 1/AD Mach from OSF R1, that was targeted for coupled SMP systems to support highly parallel applications; message-passing paradigm for NUMA computers

2. **HP-UX compatibility:** Second operating system layer compatible to HP-UX, to enable running HP-UX applications on SPP-UX, supposedly emulated HP-UX APIs and ABIs; management of distributed resources, processors, simultaneous users, process scheduler; supported parallel jobs as well as multiprocessing of single-thread
3. **Extensions and features:** Central management, open systems and standards like POSIX, specialized programming and development environment
4. Lastly, the **applications:** Possible were “HP Series 700” (stock HP-UX), “C Series” and “MPP” applications

SPP/UX supported the following hardware:

- ◇ Convex SPP1000, SPP1200, SPP1600
- ◇ HP Convex SPP2000, SPP2200, S-Class, X-Class

4.7.5 HP Tut (Mach 2)

HP Tut was an internal HP Laboratories research project in 1988-89 to port early HP-UX Unix onto a Mach microkernel, which apparently never succeeded far with that effort. It moved on to merging parts of Mach 2.0 microkernel under a HP-UX 2.0 userland (server) to get something close to resembling Mach on PA-RISC. HP Tut was the basis for various other porting efforts and PA-RISC Mach research projects.

Very few information is left on HP Tut, with some machine-dependent sources apparently having been used by the Chorus port to PA-RISC.

4.7.6 Chorus

Chorus was an early micro-kernel operating system, started as research project by the French research institute INRIA. It was commercialized in the 1980s by a spinoff, Chorus Systems. Chorus was ported to a few RISC architectures and used parts of System V Unix userland. Apparently, it was used by Unisys for a while in the 1990s, before Chorus was bought by Sun.

A development port to PA-RISC was done between 1990 and 1991 at the Oregon Graduate Institute (OGI) for the HP 9000 834 system, based on Chorus v3.3/MiX v3.2. The port was supported by HP and Chorus and done by two PhD students with some help.

For the PA-RISC port at OGI, “none of the team members had performed an operating system port before, neither did they have any experience working with the PA-RISC or Chorus.” Later on, an attempt to port Chorus/MiX V.3.2 (v3.4 nucleus) to an HP 9000 720 workstation was made at OGI, the 720 being a popular target for OS/Unix porting efforts at that time.

Hardware support

Hardware support and functionality of Chorus on PA-RISC was limited, with apparently no network interfaces or disk devices supported and console I/O depending on PDC and IODC routines. Code from various earlier projects was used, including from HP-UX 2.0 and HP Tut, Mach 2.0.

Releases

Chorus on PA-RISC was never released publically, since it used HP source code from HP Tut (Mach) and HP-UX and the USL.

The following “releases” were available as source from FTP mirrors.

- ◇ **CHORUS v3.3**: Support for HP 9000 834 (1991)
- ◇ **Chorus/MiX V.3.2**: Support for HP 9000 720 (1994?)

4.7.7 Documentation

- ◇ The Utah PA-RISC Code Snapshot Original webpage of the project. Mike Hibler (2002: University of Utah)
- ◇ <ftp://flux.cs.utah.edu/flux/mach/ALPHA/> (HTTPS mirror) contains the snapshots sets for a complete systems, University of Utah (1994-2002) **lip6.fr**
- ◇ Installation on HP 700s Utah PA-RISC Code Snapshot installation instructions. Mike Hibler (University of Utah.)
- ◇ Frequently Asked Questions about the Utah PA-RISC Code Snapshot Mike Hibler (September 1995: University of Utah)
- ◇ HPE Spectrum, comp.arch, Bob English, Oct 17, 1990
- ◇ Exemplar Operating System (SPP-UX), Hewlett-Packard Company (1997: mirror accessed January 2024)
- ◇ Convex Datasheet: Exemplar Operating System (SPP-UX), CONVEX Computer Corporation (1995: mirror accessed January 2024)
- ◇ Lites - The 4.4 BSD Lite Server, Helsinki University of Technology (1997, Johannes Helander)
- ◇ Lites - The 4.4 BSD Lite Server, 1994 OSDI BOF (1994, Johannes Helander)
- ◇ Porting Chorus to the PA-RISC: Project Overview Porting Chorus to the PA-RISC: Project Overview, 1992 Oregon Graduate Institute of Science & Technology (1994, J. Walpole, J. Inouye et al.) **pdxscholar**
- ◇ Porting Chorus to the PA-RISC: Overall Evaluation, 1992 Oregon Graduate Institute of Science & Technology (1994, J. Walpole, J. Inouye et al.) **pdxscholar**
- ◇ comp.os.chorus Frequently Asked Questions (FAQ), 1998, FAQs.org **pdxscholar**
- ◇ Chorus Ports: comp.os.chorus, Jon Inouye Nov 29, 1994, **google groups**
- ◇ PA-Chorus, Oregon Graduate Institute (OGI) (1999 archive)
- ◇ *Modularity and Interfaces in Micro-Kernel Design and Implementation: A Case Study of Chorus on the HP PA-RISC*, Proceedings of the USENIX Workshop on Micro-Kernels and Other Kernel Architectures 1992

4.8 MkLinux on PA-RISC

4.8.1 Overview

MkLinux was a 1990s project led by Apple and Open Group Research Institute to port Linux hosted on top of a Mach microkernel (pmk1.1) for Apple PowerPC computers. It was used extensively in the 1990s on computers like PowerBooks. An Open Group research project ported MkLinux later to PA-RISC, supported by HP, first released in 1997.

MkLinux was the first free operating system that really worked on PA-RISC hardware, in contrast to the various Mach ports, which suffered from unfinished development and a lot of bugs on PA-RISC. MkLinux on PA-RISC built on the previous OSF/1 MK-PA, improved the underlying OSF PA-RISC/Mach kernel from MK-PA with Linux 2.0 kernel and included X11R6 patches, the GNU ELF compiler and debugger and complete /usr and /var directories.

MkLinux on PA-RISC system was rather slow, did not support shared libraries, software support was rather rudimentary and at the time of development PA-RISC workstations were not largely available to private end-users. However, MkLinux was the first real option for hobbyists with second-hand PA-RISC computers in the 1990s.

Together with Mach 4/Lites, MkLinux inspired the later, more modern PA-RISC open source ports of Linux and OpenBSD/hppa in the late 1990s, which still exist today.

Systems support

MkLinux supported PA-RISC 1.1 32-bit HP 9000 workstation computers:

- ◇ HP 9000 705, 710, 720, 730, 750 based on PA-7000 processors
- ◇ HP 9000 715, 725, 735, 755 based on PA-7100 processors
- ◇ 715/33 not supported
- ◇ HP 9000 712, 715, 725/100 based on PA-7100LC processors
- ◇ HP 9000 C100, C110 based on PA-7200 processors

Hardware support

MkLinux supported most on-board hardware but no expansion or third-party devices.

- ◇ SCSI internal single-ended, internal fast-wide-differential, GSC based fast-wide-differential, and EISA fast-differential drives and DAT tapes
- ◇ Builtin Ethernet
- ◇ GRX, CRX and Artist graphics
- ◇ HIL and PS/2
- ◇ Audio
- ◇ RS232 serial
- ◇ ASP and LASI chipsets

Releases

MkLinux was released in snapshot status with freely distributable source, binaries, and boot images. It was available from the “OSF Mall” but could be downloaded freely from FTP in 1997. This was a more or less complete MkLinux distribution with pmk1.1 Mach kernel, MkLinux server, sources, root partition, /usr and /var content and X11R6.

The following “releases” were available as source from the Open Group (OSF) and FTP servers.

- ◇ **MkLinux for HP PA-RISC (first release):** Support for few PA-RISC 1.1 workstations (1997)

The Open Group Research Institute (OSF RI) ended its involvement into MkLinux not later than 1998.

4.8.2 Documentation

Most sources and mirrors disappeared during the last years, as ownership of the website, resources and code transitioned a few times.

- ◇ MkLinux - Linux on the OSF Microkernel, The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ MkLinux for HP PA-RISC, The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ Release Notes for MkLinux on HP PA-RISC Descriptions on MkLinux and extensive installation instructions. The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ ftp.mklinux.org/pub/hppa/, MkLinux sets at ftp.mklinux.org, The Open Group (1997, archived by CIRR 1999, current mirror SUNET.se accessed 2024)
- ◇ Software Mall - MkLinux Snapshot for HP PA-RISC, OSF (1998)
- ◇ A brief comparison of HP-UX and MkLinux on PA-RISC, Open Group (1997)
- ◇ Performance Improvements on the HP Precision Architecture, Open Group RI (1995?)

4.9 OSF/1 on PA-RISC

4.9.1 Overview

OSF/1 was the third flavor of the Unix operating system after System V and BSD. It was developed by a consortium of DEC, IBM and HP under the auspices of OSF, the Open Software Foundation. OSF/1 Unix used Mach microkernel, developed at Carnegie Mellon University (CMU), in a commercial setting. There were several experimental ports of OSF/1 to PA-RISC from HP, OSF and university groups.

HP used PA-RISC computers early for in-house operating system research including early Mach research and a HP OSF/1 port of Mach 2.0 to PA-RISC. Both saw limited distribution and use. In the 1990s OSF, the Open Group alliance ported OSF/1 Unix to PA-RISC (MK-PA) and used parts of this for the later Mach MkLinux port.

4.9.2 HP OSF/1

Around 1990, an internal HP project ported early 1.0 OSF/1 to PA-RISC, the alternative Unix operating system from an alliance of Unix vendors. HP supported the OSF/1 undertaking early on and planned a transition of its Unix offering towards OSF/1 when microkernel Mach operating systems were en vogue in the 1990s.

HP OSF/1 was developed by ex-Apollo staff after Apollo was bought by HP, with Mach 2.0 macrokernel on early HP 9000/700 workstations. The result was a fairly complete OSF/1 operating system with proper hardware support and usable desktop environment with Motif and other OSF/1 applications.

Releases

HP OSF/1 on PA-RISC was never distributed widely and sold commercially only for a short time before being withdrawn. It was apparently used a lot at the University of Utah, but HP decided against betting on it commercially, “[f]inding fault with at least OSF 1.0’s memory management, [HP] has distributed only limited quantities of what it considers a technical release.”

Hardware support

HP OSF/1 apparently supported the following HP 9000 PA-RISC workstations:

- ◇ HP 9000 720, 730 based on PA-7000 processors

4.9.3 Open Group MK-PA

The OSF Open Group Research Institute ported microkernel OSF/1 to PA-RISC in the mid-1990s as research project. Called MK-PA, the OSF port focused on 32-bit HP 9000/700 workstations and servers. Development was supported by HP OSSD (Open Source Software Development?) in several parts of the kernel and subsystems.

Performance was supposedly similar in HP-UX and MK-PA at the time with some advantages at higher loads for MK-PA OSF: “MK-PA is comparable to that of HP-UX for loads up to 200 simulated users and better for heavy loads.”

HP-UX compatibility (HPUX-CM) with HP-UX 9.05 was provided in MK-PA 7.1, compatibility with HP-UX 10 in MK-PA 7.2. For this, Open Group had to make the OSF/1 filesystem HP-UX compatible, extend OSF/1 to support HP-UX system calls and replace the HP-UX kernel with microkernel and HP-UX server. With this, MK7.2 could boot on a HP-UX filesystem with HP-UX binaries like HP-VUE. HP-UX X11 applications like FrameMaker, Mosaic could run on MK-PA.

Releases

OSF MK-PA was never released widely and required obtaining an OSF/1 source license from Open Group, which few institutions had.

- ◇ **MK6.0-PA** in 1994: Performance improvements from MK6, short-circuit RPC, HP-UX compatibility
- ◇ **MK6.3-PA** in 1995: PA-RISC merged in mainline, better performance, robustness and HP-UX compatibility, some RT support, X support
- ◇ **MK7-PA** in 1996: More RT functionality, FDDI and IP multicast, Dynamic Buffer Cache
- ◇ **MK7.2-PA** in 1996: Myrinet, Distributed systems (DIPC, XMM, KKT), real-time functionality, high-precision clock, HP-UX 10.0 compatibility

OSF MK 7.2 ran on both Intel x86 and HP PA-RISC and featured OSF/1 1.3.1 commands and libraries. Parts of MK-PA wound up later in free Mach 4/Lites and MkLinux. There were no known public releases of MK-PA since then.

Hardware support

MK-PA supported PA-RISC 1.1 hardware in HP 9000 workstations with strong HP-UX compatibility. Support for PA-RISC 1.0 was dropped from the original Mach 3/UX code base. MK-PA supported the following HP 9000 computers and hardware:

- ◇ HP 9000 710, 720, 730 based on PA-7000 processors
- ◇ HP 9000 715, 725, 735, 755 based on PA-7100 processors
- ◇ HP 9000 712, 715, 725/100 based on PA-7100LC processors
- ◇ HP 9000 J200, J210[XC], based on PA-7200 processors
- ◇ Most onboard I/O devices
- ◇ Interphase FDDI board, EISA Ethernet boards, HP Labs GSC bus Myrinet board
- ◇ Additionally DIPC and CORDS

Usage

OSF MK-PA on PA-RISC was mostly used by research institutions in the mid-1990s and was never distributed widely as commercial operating system.

Research usage included defense-related ARPA projects, where the US Navy (NSWC) used OSF MK7.2 for “real-time analysis and display of radar tracking data,” seemingly with TAC-4 support. PA-RISC computers with MK7.2-PA ran “Radar Track Data Servers” to which Pentium and SPARC systems were connected via Myrinet, processing up to “4800 radar tracks/second.”

4.9.4 Documentation

- ◇ MK-PA: An HP-UX compatible microkernel based Operating System, The Open Group (1998)
- ◇ An HP-UX compatible microkernel based Operating System, OSF RI Grenoble (1997)
- ◇ MK-PA Project Update, James Loveluck (1996: The Open Group)
- ◇ OSF MK 7.2, OSF RI (1997: , accessed February 2018)
- ◇ MK6-PA Performance Results, Open Group RI (1998)
- ◇ HPUX-CM: an HP-UX Compatibility Module for the HP-PA OSF/1 Server, OSF RI (1997)
- ◇ HEWLETT-PACKARD PUTS OSF/1 ON HOLD AS IT MERGES DOMAIN WITH HP-UX, Computer Business Review, March 22, 1992

4.10 Chorus on PA-RISC

4.10.1 Overview

Chorus was an early micro-kernel operating system, started as research project by the French research institute INRIA. It was commercialized in the 1980s by a spinoff, Chorus Systems. Chorus was ported to a few RISC architectures and used parts of System V Unix userland. Apparently, it was used by Unisys for a while in the 1990s, before Chorus was bought by Sun.

A development port to PA-RISC was done between 1990 and 1991 at the Oregon Graduate Institute (OGI) for the HP 9000 834 system, based on Chorus v3.3/MiX v3.2. The port was supported by HP and Chorus and done by two PhD students with some help.

For the PA-RISC port at OGI, “none of the team members had performed an operating system port before, neither did they have any experience working with the PA-RISC or Chorus.” Later on, an attempt to port Chorus/MiX V.3.2 (v3.4 nucleus) to an HP 9000 720 workstation was made at OGI, the 720 being a popular target for OS/Unix porting efforts at that time.

4.10.2 Systems support

Two PA-RISC computers were supported by Chorus on PA-RISC

- ◇ HP 9000 834 server, NS-1 PA-RISC 1.0, in Chorus v3.3
- ◇ HP 9000 720 workstation, PA-7000 PA-RISC 1.1, in Chorus/MiX V.3.2

4.10.3 Hardware support

Hardware support and functionality of Chorus on PA-RISC was limited, with apparently no network interfaces or disk devices supported and console I/O depending on PDC and IODC routines. Code from various earlier projects was used, including from HP-UX 2.0 and HP Tut, Mach 2.0.

4.10.4 Releases

Chorus on PA-RISC was never released publically, since it used HP source code from HP Tut (Mach) and HP-UX and the USL.

The following “releases” were available as source from FTP mirrors.

- ◇ CHORUS v3.3: Support for HP 9000 834 (1991)
- ◇ Chorus/MiX V.3.2: Support for HP 9000 720 (1994?)

4.10.5 Documentation

- ◇ Porting Chorus to the PA-RISC: Project Overview Porting Chorus to the PA-RISC: Project Overview, 1992 Oregon Graduate Institute of Science & Technology (1994, J. Walpole, J. Inouye et al.) [pdxscholar](#)
- ◇ Porting Chorus to the PA-RISC: Overall Evaluation, 1992 Oregon Graduate Institute of Science & Technology (1994, J. Walpole, J. Inouye et al.) [pdxscholar](#)

- ◇ [comp.os.chorus Frequently Asked Questions \(FAQ\)](#), 1998, [FAQS.org](#) [pdxscholar](#)
- ◇ [Chorus Ports: comp.os.chorus](#), Jon Inouye Nov 29, 1994, [google groups](#)
- ◇ [PA-Chorus](#), Oregon Graduate Institute (OGI) (1999 archive)
- ◇ *Modularity and Interfaces in Micro-Kernel Design and Implementation: A Case Study of Chorus on the HP PA-RISC*, Proceedings of the USENIX Workshop on Micro-Kernels and Other Kernel Architectures 1992

4.11 Windows NT and NetWare PA-RISC

4.11.1 Overview

Parallel to the well-known Unix and Mach operating systems for PA-RISC, some rather odd operating system ports were attempted over time. Forgotten since, HP and PA-RISC were part of several corporate development projects for commercial operating systems in the 1990s: Windows NT was ported by HP to PA-RISC as a demonstration and NetWare on PA-RISC had a serious product roadmap planned.

And there was also an abortive HP-UX port to Intel i386.

4.11.2 Windows NT

There were development efforts in the mid-1990s to port Microsoft Windows NT to PA-RISC. HP wanted to hedge its bets in the workstation market and especially the anticipated NT workstation market, which threatened Unix workstations.

Several magazine sources and USEnet posts around 1993 point to HP pursuing a PA-RISC port to NT, modified the PA-RISC architecture for bi-endianess PA-7100LC processors and even conducted a “back-room” presentation at the '94 Comdex conference of a (modified HP 712?) PA-7100LC workstation running Windows NT. Mentions of NT on PA-RISC continued in 1994 with some customer interest and the HP 9000 712 workstations were mentioned before release as possibly supporting Windows NT, next to Unix. No further indications in the press appeared after 1995.

Sources at HP (from the Unix division no less) spoke of “dim prospects” for NT on PA-RISC in October 1994 and it (NT) being a “dead-end architecture” in 1996. The final nail was the missing application landscape for PA-RISC on NT, as many applications would have to be ported or recompiled. Consensus at HP at the time seemed to favor the anticipated move to the post-RISC era with VLIW EPIC/Itanium – which did support Windows NT next to HP-UX, with Windows 2000 and XP follow-ons too.

Windows NT apparently “ran” on the following HP 9000 PA-RISC computers:

- ◇ HP 9000 712 based on PA-7100LC processors

4.11.3 NetWare

In the early 1990s, a two-year effort to port the NetWare operating system to PA-RISC was planned by HP and Novell. It was led by Novell as part of its “aggressive into the UNIX industry” with first product shipments targeted for 1992-93. The PA-RISC port was “more mortar for Novell’s brick wall.”

Novell dominated the network operation system market at the time and had agreements with other RISC vendors to port their architectures.

Development of PA-RISC was part of Processor-Independent NetWare (PIN) of NetWare 4.1. Support was planned for different computer architectures besides x86 like Alpha, Sun, MIPS and PowerPC.

The porting effort at NetWare for PIN and HP for the PA-RISC part took longer than planned (“got bogged down”), and HP finally pulled out in 1994 after Novell was unable to deliver Processor-Independent NetWare (PIN) on schedule.

PA-RISC NetWare was the supposed to be released in summer of 1994, until HP cancelled its plans to sell PIN on HP 9000 computers after the porting delays. HP decided to satisfy the “niche” for NetWare

in its product lineup with Intel-based NetServer computers supplemented by Portable NetWare on HP-UX, NetWare 4.1 Services and Novell Directory Service (NDS) ports to HP-UX.

The delay of PIN and cancellation of PA-RISC were a major disappointment when PA-RISC was “one of [the] prime choices” for NetWare.

NetWare apparently supported the following HP 9000 PA-RISC computers:

- ◇ unknown

4.11.4 HP-UX on Intel x86

Apparently, HP conducted a prototype port of HP-UX to x86 hardware when the future of HP-UX and the Itanium platform were in doubt during the early 2010s. PA-RISC was long gone then and HP had a team working in secret (“skunkworks”) to port HP-UX to x86 away from Itanium.

Some documents were made public through lawsuits; Oracle described HP efforts on repositioning itself and its server and Unix division in the early 2010s. HP apparently mulled buying parts of Sun and Solaris to consolidate its Unix position. Solaris was the Unix leader at the time in the US and HP-UX “everywhere else”, even though on a “death march due to inevitable Itanium trajectory.”

Parts of the conversation in these documents mention a successful boot of HP-UX on x86 in December of 2009, with porting efforts projected to cost “100M+” between 2010 and 2016. The plan was for mission-critical x86 systems (ProLiant DL980 and Superdome with x86) and first releases projected in 2011 (developer) and 2012 (Superdome and Linux ABI).

4.11.5 Documentation

- ◇ Novell und HP arbeiten an einem gemeinsamen RISC-Server, Computerwoche 20.12.1991
- ◇ HP lays out next-generation chip plans, Computerworld 1993-12-20: Volume 27 Issue 51
- ◇ HP edges toward NT support, Computerworld December 13, 1993: Volume 27 Issue 50, front and page 12
- ◇ NetWare hits setback in RISC-y move, Computerworld, Jul 11, 1994, Volume 28 Issue 28, page 121
- ◇ Decide already, Computerworld, Oct 3, 1994, Volume 28 Issue 40, page 134
- ◇ Novell’s NetWare for PA-RISC, Unix World February 1992, Volume IX, Number 2, page 16
- ◇ Processor Independent NetWare to run on HP, Sun and DEC RISC, InfoWorld 4 Oct 1993
- ◇ HP backs away from Novell PIN plans, redirects strategy to Intel NetServer, PC Week July 4, 1994
- ◇ When the Power Macintosh ran NetWare, Old VCR December 23, 2023
- ◇ HP started then spiked HP-UX on x86 project, The Register 23 May 2012

4.12 HP-RT Real-time

4.12.1 Overview

HP-RT was a real-time operating system from HP for its HP 9000 740 VME instrumentation computers, released from 1993 to 1997 in six versions from 1.0 to 3.0. It was sold as part of the “HP-RT Developer’s Kit” that included the 743rt and high performance 744rt VME computers.

HP-RT is derived from the real-time operating system LynxOS and was built as real-time operating system from scratch with native POSIX API and Unix features like “protected address spaces, multi-processing, and standard GUI.” Real-time scheduling is part of the kernel with response times under 200 μ s, later improved to sub-100 μ s for uses such as “hospital system tied to a heart monitor, or a missile tracking system.”

For programming, HP-RT supported dynamic shared libraries, ANSI C, Softbench (5.2), FORTRAN, ADA, C++ and PA-RISC assembly. From HP-RT 3.0, GUI-based debugging environment (DDert) and Event Logging library (ELOG) were included. POSIX 1003.1, 1003.1b and POSIX 1003.4a draft 4 were supported.

On the software side, HP-RT supported fast file system, X and Motif clients, X11 SERVERrt, STREAM-Srt (SVR 3.2), NFS, and others.

Software development required the *HP-RT Development Environment*, 740rt VME machines, like the 742rt, but also a dedicated HP 9000 700 host machine with HP-UX for compiling and linking. The software was then downloaded to the rt VME system.

HP 74x VME products were discontinued in 2002 as “customers have migrated to new solutions and platforms more rapidly than anticipated” with end of support between 2003 and 2007. This EOL included HP-RT as there were no follow-on HP PA-RISC products.

Systems support

HP-RT supported HP 9000 740 Series VME computers with rt suffix that were almost identical to their non-rt products.

System	Processor	Speed	HP-RT versions
HP 9000 742rt	PA-7100	50 MHz	HP-RT 1.0 to 3.0
HP 9000 743rt	PA-7100LC	64 MHz	HP-RT 2.0 to 3.0
V743rt Agilent	PA-7100LC	100 MHz	HP-RT 2.1 to 3.0
HP 9000 744rt	PA-7300LC	132-165 MHz	HP-RT 3.0

Hardware support

HP-RT supported most of the on-board hardware and only few expansion boards and devices. Some of the hardware and I/O was first supported in the last HP-RT version 3.01.

- ◇ HP SCSI single-ended (SE) and some fast-wide differential (FWD) SCSI
- ◇ RS-232-C serial and parallel
- ◇ Ethernet

- ◇ PC Card (PCMCIA) type II and flashdisks
- ◇ VME controller for VMEbus devices
- ◇ HCRX-8 and HCRX-24 GSC and Visualize-EG

4.12.2 Releases

There were six released versions of HP-RT from 1.0 to 3.01 plus several minor patch releases like 2.11 that were not shipped to all customers. A pause in releases was between 2.1 (1995) and 3.0 (1997) when support had to be developed for HP-UX 9 and HP-UX 10 in the HP-RT developers kit.

From inception, HP-RT was compliant with POSIX 1003.1 (operating system programming interfaces) and POSIX 1003.4 and 4a drafts (real time extensions and threads).

HP-RT is split into two parts: The HP-RT kernel with low-level I/O drivers, a 10ms interrupt clock, access to hardware timers (1µs) and standard OS functions such as scheduling, multitasking, memory management, IPC and kernel services. The second part: HP-RT services contain optional higher-level functions such as NFS, TCP/IP, debuggers.

The HP-RT developers kits cost \$9,995 at time of release. It seems HP-RT development and releasing was a bit in flux throughout the short(ish) timespan of commercial support and HP-RT ended soon after 744rt workstations and HP-UX 10.20 EOL.

HP-RT 3.0

HP-RT 3.00 was released as the last major version in January 1997. It added support for the PA-7300LC-based VME workstations 744rt/132L (no graphics yet) and updated the HP-RT operating system core significantly.

- ◇ POSIX.1b
- ◇ Dynamic shared libraries
- ◇ DDErt debugging and ELOG event logging
- ◇ Fast file system and NFS client caching
- ◇ Cron support
- ◇ Support for 40Mb flashdisk in PCMCIA

HP-RT 3.01 was the last version of HP-RT from October 1997 and added mostly hardware support, including for the 744rt/165L

- ◇ Visualize-EG graphics adapter
- ◇ SCSI fast-wide differential (FWD) support for A4268A adapter
- ◇ CD and SCSI floppy
- ◇ X11R6 Server
- ◇ Support for HP-UX 10.30
- ◇ PMC (PCI mezzanine) bridge board and expansion kit

HP-RT 2.0

The second HP-RT major release 2.0 was introduced in August 1994 and added support for HP 9000 743rt based on PA-7100LC processors. Besides hardware, HP-RT 2.0 added some features:

- ◇ FORTRAN (“not thread safe”)
- ◇ STREAMSrt (whatever that was)
- ◇ Further performance improvements
- ◇ More “alignment with HP-UX”
- ◇ BOOTP for network booting

HP-RT 2.1 was released in October 1995 and added more features and support for the (Agilent) V743rt VXI workstations with 32-bit PA-7100LC processors. The 743rt (and 742rt?) workstations were still supported.

- ◇ X11 SERVERrt graphical
- ◇ SNMPrt agent
- ◇ PCMCIA adapter support
- ◇ C++ (thread safe)
- ◇ “Generic driver”
- ◇ Debugging improvements

HP-RT 2.2 was released in June 1996 with several functional enhancements:

- ◇ HCRX-8 and HCRX-24 GSC graphics adapters
- ◇ Administration tool ADMrt
- ◇ Compatibility with HP-UX 10.10

There might have been a HP-RT 2.21 that already supported 744rt/132L, the GSC second slot expansion kit and external SCSI drives and DDS tapes.

HP-RT 1.0

The first HP-RT version 1.0 was released in January 1993, it supported the 742rt VME-based workstation on PA-7100 processors.

Features of HP-RT 1.0 were:

- ◇ POSIX.1 support and draft POSIX.4 and .4a support
- ◇ TCP/IP networking
- ◇ Network file system NFS
- ◇ X and Motif, X-terminal support
- ◇ C/ANSI C and C++ (“not thread safe”)

HP-RT 1.1 was released in July 1993 and extended some HP-RT features:

- ◇ Performance enhancements of HP-RT (“system tuning”)

- ◇ OTSrt (whatever that was)

4.12.3 Documentation

Almost all information on HP-RT has been gone from the internet for years.

Product features

- ◇ HP-RT Overview, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ hp-rt overview & features, Hewlett-Packard Company (2002: mirror accessed January 2024)
- ◇ HP-RT Roadmap of Key Features, Hewlett-Packard Company (n.d.: mirror accessed January 2024)
- ◇ The HP-RT Real-Time Operating System (.pdf) Kevin D. Morgan (August 1993: Hewlett Packard Journal. Accessed Januar 2024)
- ◇ HP-RT Datasheet, *Deterministic response time you can count on!*, Hewlett-Packard Company (2000: mirror accessed 2024)

Websites

- ◇ HP VME product availability and support, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ HP-RT Release Model, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP VME frequently asked questions, Hewlett-Packard Company (2001: mirror accessed January 2024)
- ◇ HP UPGRADES RT REAL-TIME SYSTEM, CBR Online Archive, March 19, 1997;
- ◇ Support Life Letter for HP-RT, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP Real-Time Computer Automates Pharmaceutical Production, Hewlett-Packard Company (2000: mirror accessed 2024)
- ◇ HP's real-time computing beats high-imaging speed, Hewlett-Packard Company (2000: mirror accessed 2024)

Manuals

- ◇ HP-RT Quick Reference HP-RT Manuals, Hewlett-Packard Company (2000, B5487-90009: mirror accessed 2024)
- ◇ VME Backplane Networking Administration Guide HP-RT Manuals, Hewlett-Packard Company (2000, B5489-90001: mirror accessed 2024)
- ◇ HP-RT Symbolic Debugger Users Guide HP-RT Manuals, Hewlett-Packard Company (2000, B5487-90004: mirror accessed 2024)
- ◇ Using STREAMS in the HP-RT Environment HP-RT Manuals, Hewlett-Packard Company (2000, B5491-90001: mirror accessed 2024)

- ◇ X11 SERVER rt Installation and Configuration Guide HP-RT Manuals, Hewlett-Packard Company (2000, B5493-90001: mirror accessed 2024)
- ◇ HP-RT Reference Volume 1 HP-RT Manuals, Hewlett-Packard Company (2000, B5487-90005: mirror accessed 2024)
- ◇ HP-RT Reference Volume 3 HP-RT Manuals, Hewlett-Packard Company (2000, B5487-90007: mirror accessed 2024)

4.13 PA-RISC Emulation QEMU

4.13.1 Overview

QEMU is an open source computer emulation and virtualization software, first released in 2003 by Fabrice Bellard. It supports many different computer systems and includes support for many RISC architectures besides x86. PA-RISC emulation has been included in QEMU since 2018.

QEMU emulates a complete computer in software without the need for specific virtualization hardware. With QEMU, a full HP Visualize B160L and C3700 workstation can be emulated to run PA-RISC operating systems like HP-UX Unix and compatible applications.

4.13.2 Systems support

QEMU supports emulating two types of PA-RISC workstations, both 32-bit and 64-bit, with necessary devices and I/O.

- ◇ HP Visualize B160L workstation with 32-bit PA-7300LC processor
- ◇ HP Visualize C3700 workstation with 64-bit PA-8700 processor (from QEMU 8.2, but still unstable)

4.13.3 Hardware support

Most of the major onboard hardware of the currently two workstations is supported by QEMU with some drivers and specific devices still missing.

Processors

Supported are 32-bit PA-RISC 1.1 PA-7300LC processors and 64-bit PA-RISC PA-8700 processors. Although both emulated machines are in reality single-CPU, QEMU allows both to emulate up to 16 virtual processors running in parallel.

QEMU currently allows to configure up to 3840 MB of memory. 32-bit PA-RISC operating systems will only allow 3584 MB. Supporting more memory for 64-bit operating systems is planned for the future.

Buses and chipsets

Onboard PCI, GSC and Runway buses and bus bridges are supported. Some HP chipsets are supported: LASI (partially), Dino, U2/Uturn, Astro and Elroy.

Other chipsets (ASP, Cell, zxt) and buses (ISA, EISA, VME) are not supported.

Networking

Most physical PA-RISC machines shipped with a DEC 21142/43 *Tulip* network card, which is supported by QEMU. Other PCI network cards like RealTek RTL8129/8139 Fast-Ethernet or Intel Gigabit Ethernet (e1000) can be emulated if the operating system (HP-UX or Linux) support it.

Unsupported are all other types of HP network interface like the 10MB Ethernet (82596DX and i82C596CA on ASP and LAS), FDDI on the 735/755 and others.

Storage

Storage is supported on LSI NCR 53C95A Ultra-Wide controllers.

Currently unsupported are earlier SIOP NCR 53C700 and NCR 53C710 devices for Narrow-SCSI integrated into LASI or on older HP 9000 workstations.

Graphics

Text-mode (STI) and graphics (X11) are supported on Artist graphics adapter. No other adapters are supported. X11 graphics for CDE are working.

Human I/O and multimedia

Input/output is supported via PS/2 interfaces. USB is only partially supported.

“Harmony” 16-bit audio, found on many PA-RISC workstations, is not supported.

4.13.4 OS support

Some of the major PA-RISC operating systems and releases work under QEMU emulation of HP B160L and C3700 PA-RISC workstations.

- ◇ HP-UX Unix from HP
- ◇ Linux on PA-RISC
- ◇ NetBSD/hppa from version 8.0
- ◇ Partially: MkLinux

QEMU emulates PDC (the “BIOS”), I/O routines and hardware so the emulation appears as a complete system to the operating system. OpenPA tested a few operating systems in late 2024.

4.13.5 Releases

The following QEMU versions have been available for PA-RISC.

- ◇ QEMU 9.2.0 (December 2024): Stable version for 32-bit and 64-bit PA-RISC
- ◇ QEMU 8.2 (September 2023): Support for 64-bit C3700
- ◇ QEMU 7.1.0 (August 2022): Added many PA-RISC enhancements to QEMU
- ◇ QEMU 2.12 (2018): First release to support PA-RISC (Helge Deller, Richard Henderson)

QEMU is available as source and included as binary in various operating systems package managers for installing third party software:

- ◇ Debian: Included in APT, `apt-get install qemu-system`

- ◇ Source: For compiling QEMU by tarballs or from git
- ◇ MacOS with brew: `brew install qemu`
- ◇ Fedora (dnf), Gentoo (emerge), RHEL (yum), SUSE (zypper)
- ◇ Windows binaries (Win32 and 64-bit, MSYS2)

4.13.6 Configuration

Example of QEMU with PA-RISC configuration, running HP-UX on a HP Visualize B160L workstation. This assumes QEMU has been installed in version 9.2.0.

Starting QEMU

Start QEMU with a minimal configuration and HP-UX boot CD-ROM ISOs:

```
# qemu-system-hppa -drive file=hdd.img -serial mon:stdio \
-cdrom iso/hpux.iso -boot menu=on -boot order=d -m 256 -machine B160L -smp cpus=1
```

This will start up QEMU to the PDC “BIOS” (SeaBIOS emulation of PDC):

```
SeaBIOS PA-RISC 32-bit Firmware Version 17 (QEMU 9.2.0)
```

```
Duplex Console IO Dependent Code (IODC) revision 17
```

```
-----
(c) Copyright 2017-2024 Helge Deller and SeaBIOS developers.
-----
```

Processor	Speed	State	Coprocessor State	Cache Size
0	250 MHz	Active	Functional	0 KB

```
Emulated machine:   HP B160L (32-bit PA1.1), 32-bit PDC, OS32
Available memory:   256 MB
Good memory required: 16 MB
```

```
Primary boot path:  FWSCSI.0.0
Alternate boot path: FWSCSI.2.0
Console path:       SERIAL_1.9600.8.none
Keyboard path:      SERIAL_1.9600.8.none
```

Available boot devices:

```
FWSCSI.0.0 : lsi 00:00.0 0:0 Drive QEMU QEMU HARDDISK 2.5+
FWSCSI.2.0 : DVD/CD [lsi 00:00.0 2:0 Drive QEMU QEMU CD-ROM 2.5+]
```

```
----- Main Menu -----
```

Command	Description
B0ot [PRI ALT <path>]	Boot from specified path

HElp [<menu> <command>]	Display help for menu or command
RESET	Restart the system
EXIT	Exit QEMU emulation

Main Menu: Enter command >

From the PDC, we proceed to the HP-UX installer:

```
Main Menu: Enter command > BOOT ALTERNATE
Interact with IPL (Y, N, or Cancel)?> N
```

To later boot the installed HP-UX on the drive image, remove `-boot order=d` and boot the primary drive in PDC (FWSCSI.0.0):

```
Main Menu: Enter command > BOOT PRIMARY
```

Settings

Some of most important basic settings, as used above in *Starting QEMU* for installing operating systems.

Drives

`-drive file=hdd.img` sets the first SCSI harddrive in QEMU to an HD image, which can be created by `# qemu-img create hdd.img 2G`

`-cdrom iso/hpux.iso` sets the SCSI CD-ROM to an ISO image for booting

Hardware

`-m 256` sets the main memory RAM to 256 MB

`-machine B160L` configures a HP Visualize B160L workstation

`-smp cpus=1` sets a single CPU

Boot and console

`-boot order=d` sets first boot order to the CD

`-boot menu=on` asks for the PDC boot menu

`-serial mon:stdio` standard I/O and monitor to console

`-serial telnet:0.0.0.0:8001,server,nowait -monitor stdio -nographic` for serial console redirected to local telnet

Tested operating systems

The following systems have been tested with QEMU version 9.2.0 as of late 2024:

- ◇ HP-UX 10.20 from May 2000 boots and installs, X11 and CDE work fine on B160L with 512 MB RAM and 2 GB disk
- ◇ HP-UX 11.00 from June 2002 and March 2004 boots and installs, X11 is spotty using 2 GB RAM and 4 GB disk
- ◇ HP-UX 10.20 from December 1999 boots and installs

- ◇ HP-UX 11.11 (11i) from December 2004 boot hangs on B160L and crashes on C3700 hangs while detecting I/O devices
- ◇ HP-UX 9.07 or 9.05: boot ISOs but no progress after that possibly missing QEMU drivers
- ◇ OpenBSD/hppa 7.6 boots install176.iso, installs but crashes on reboot of HD
- ◇ NeXTSTEP 3.3 boots but the installer crashes with 128 MB memory; possibly missing QEMU drivers
- ◇ Using a C3700 as emulated machine was spotty

These are admittedly quick test results and problems might be configuration issues or actual bugs and limitations in QEMU drivers. More information might be found on official QEMU pages but OpenPA will pursue more tests.

4.13.7 Documentation

- ◇ QEMU for PA-RISC overview, Linux kernel.org (August 2024)
- ◇ Download QEMU, QEMU (2024)
- ◇ SeaBIOS PDC (BIOS) on PA-RISC, Helge Deller github (2024)
- ◇ Dellerweb QEMU, Helge Deller, n.d.
- ◇ QEMU on PA-RISC, Helge Deller github (2024)
- ◇ QEMU Features/HPPA, QEMU Wiki, 2020

4.14 HP-UX Games and Software

4.14.1 Overview

While HP-UX was mostly used for engineering and design applications during the PA-RISC heydays, several games were ported to and played on HP-UX Unix in the 1990s.

This included many iconic 3D games from the early 1990s, compiled with OpenGL but also some other, semi-commercial ports of well-known games and the big universe of Unix and X11 freeware games.

Most games were ported HP-UX 10.20 from the late 1990s, with some newer ports targeting HP-UX 11.00 or HP-UX 11.11. Long dormant, some ports were rediscovered or adapter in the 2010s and 2020s again.

4.14.2 Collections

Many freeware games collections were available for Unix and often could be compiled on various versions of HP-UX.

- ◇ Unix Guru Universe: Games Software, source files from *asteriods* to *xtrek*
- ◇ HP-UX Porting Center: Games (Arcade) includes many X11 games as binaries
- ◇ HP-UX Porting Center: Games (Board) for strategy and traditional board games
- ◇ HP-UX Porting Center: Games (Networking) for games played over networks

Note some of these ports and packages are two decades old, so might need tweaking to run on “newer” HP-UX versions.

4.14.3 Commercial

The roster of commercial games and their ports included various well-known titles from the 1990s, with many games known to be working or having worked on HP-UX.

Doom

- ◇ Doom from id Software, the first-person shooter game from 1993, runs also on several Unix platforms and Linux since an unofficial port in 1994.
- ◇ An HP-UX version is available through Doom It Yourself from the early 2000s, based on id LinuxDoom sources. HP-UX needs some modifications (2020).
- ◇ Doom was apparently installed as easteregg on HP Agilent 16700 logic analyzers

Quake

- ◇ It seems Quake and Quake2 were ported to Unix and HP-UX specifically, but few documentation and resources exist
- ◇ CQ3A, a Quake3 renderer for CAVE apparently supports HP-UX
- ◇ An attempt was made to port Quake3 to newer HP-UX but the status is unclear

Simcity

There are two Simcity version for Unix– one is original DUX port and the second is Micropolis, a re-release for the OPLC program.

- ◇ Simcity, the multiplayer interactive strategy game, was ported by DUX in the early 1990s to Unix systems and distributed pretty widely as demo software in the Unix community
- ◇ Simcity has been recently liberated with some modifications and fixes
- ◇ It is known to be running on HP-UX 9, possibly also later versions HP-UX 10 and 11, it runs on X11 (Motif and Tcl) and can be played over the network with multiple players
- ◇ SimCity source was re-released as *Micropolis* during the OLPC (One Laptop Per Child) program
- ◇ Micropolis for Vintage Unix uses Simcity parts and is a fork of Linux Micropolis for X11.
- ◇ Micropolis supports newer HP-UX versions for HP 64-bit computers: 11i v1 (PA-RISC) and HP-UX 11i v3 (Itanium)

Civilization

There never was an official *Civilization* port, but an open source game inspired by it has been developed since the 1990s.

- ◇ Freeciv is a free and open turn-based strategy game, inspired by Civilization concepts. Internet and LAN multiplayer are supported plus many languages and platforms. Gameplay is in X11.
- ◇ Freeciv apparently supports HP-UX (and other Unix systems) in its source code, but no pre-compiled package repositories are known (sources).
- ◇ Freeciv was started in the mid-90s by students, after trying the Python/Tcl-based OpenCiv.

ACM flight simulator

- ◇ ACM Flight Simulator, a graphical flight simulator for jet aircraft, on X11
- ◇ ACM has been developed since the 1990s for Windows and Unix (last version 5.0)
- ◇ Packages of ACM are available for HP-UX, versions 11.11 (PA-RISC) to 11.31 (Itanium)
- ◇ ACM runs on X11, supports network play for up to eight clients, and simulates jet aircraft

Dominion

- ◇ Dominions: Priests Prophets & Pretenders, a turn-based fantasy game available for many Unices, runs on HP-UX in some older versions
- ◇ For HP 9000 an old HP-UX port is available

Maelstrom

- ◇ Maelstrom is a 2D space shooter originally developed for Macintosh MacOS in the 1990s
- ◇ Maelstrom gameplay is based on old Atari games – Asteroids and Blasteroids of the 1980s
- ◇ After Maelstrom was open sourced, it was later ported to Linux as Maelstrom 3.0. This Linux source also runs on various HP-UX versions
- ◇ Maelstrom HP-UX 11 on PA-RISC is available at OS archive

Battalion

- ◇ battalion, an arcade game developed in 1994 on Silicon Graphics for OpenGL runs on many operating systems
- ◇ Originally developed on Unix (IRIX), it has been ported to other Unices, various Windows versions and even iPhones
- ◇ battalion uses OpenGL graphics and had been adapted to use CAVE virtual reality environment
- ◇ For HP 9000, a newer (2024) HP-UX port is available at osarchive

Unclear status

- ◇ PEX Drive, was a demo from HP Graphics Labs to showcase the HP PEX library
- ◇ ClassiCube, an open replication of Minecraft Classic, for which a port to HP-UX is in progress
- ◇ OpenTTD, an open source simulation game similar to Transport Tycoon, runs on Linux and Unix systems. An HP-UX port might be possible.

4.14.4 Software

Will be extended in due time.

4.14.5 Documentation

- ◇ Reddit HP 16700 and Doom

4.15 PA-RISC Operating Systems History

4.15.1 Overview

Many operating systems and platforms were developed for PA-RISC computers since its inception in 1986. PA-RISC was designed as Unix platform but used in many more commercial, research and later open source systems.

PA-RISC Unix history started in 1986 with early commercial HP Unix — HP-UX for PA-RISC, which is still (somewhat) shipped today. Several other Unix commercial products from HP and other PA-RISC vendors were developed over the years.

Often used for research and development, PA-RISC was part of many academic projects, often based on Mach and BSD kernels and Unix-like operating systems. PA-RISC Open Source is based on these research projects, with the Linux and OpenBSD and then NetBSD port building on their codebases.

4.15.2 Unix: HP-UX and others

Unix was the standard operating system choice for PA-RISC computer and the main target for PA-RISC while developing it. HP 9000 were dedicated Unix servers and then workstations. Most operating systems for PA-RISC were either Unix implementations or variants of it.

HP developed and ported HP-UX, its commercial Unix offering, to PA-RISC very early on. Closely based on BSD Unix, HP-UX later on moved towards System V. Many of the Asian HP PA-RISC OEMs and clones also used HP-UX variants or own Unix implementations.

Another commercial, Unix-like operating system was NeXTSTEP, ported to PA-RISC during the 1990s, in parallel to other developmental ports of various commercial systems.

The plethora of research projects of the 1990s also used Mach microkernel and Unix-like systems, as did the 2000s open source (OSS) projects.

HP-UX on PA-RISC

The story of HP-UX Unix began before PA-RISC with versions for the early HP 9000 lineup — the HP FOCUS systems. From the late 1980s on, HP-UX was available on the first PA-RISC server computers (800s), with HP-UX 1.0 or 2.0 the first release on PA-RISC in 1986 or 1987.

Many updates soon followed, even though versioning was a bit complicated during that sparsely documented time. In the 1980s, another HP-UX was released with 3.0, followed by HP-UX 7.0 in 1990. The first HP Unix release for both 800 Series servers and the new 700 Series workstation was HP-UX 8.0, followed by 9.0 from the early 1990s, still strongly BSD-based. Releases were still not unified for 700 and 800 computers, with different minor releases specific to both.

The new HP-UX 10 was released a few years later in 1995, delayed for a year due to technical bugs. It was followed in quick succession by HP-UX 10.10 (mostly ignored), 10.20 and 10.30. Due to feared Y2K issues in earlier versions, HP made HP-UX 10.20 available free of charge for HP 9000 owners for a while. A server-only 10.30 released followed in 1997, as were many Additional Core Enhancements (ACEs), that added workstation hardware support to HP-UX 10.20.

The modernized HP-UX 11.0 was released soon after, starting in 1997, with a “true 64-bit kernel” with full 64-bit support for 64-bit computers but still support for many 32-bit PA-RISC systems. There was

supposedly scant support for workstations in the original 11.00 release that was developed by the HP Server division – to be added later with the EP and ACE in 1998 and 1999.

The focus of HP-UX shifted with 11i to the newer “lettered” (A-Class, B-Class) and rp/rx 64-bit and Itanium servers. HP started developing the HP-UX kernel to support PA-RISC and Itanium already beginning in 1997, and apparently together with NEC and Hitachi, old PA-RISC co-conspirators. HP-UX 11i v2 from 2003 then integrated PA-RISC and Itanium into a single operating system stream while HP-UX was focused more and more on specialized server roles – and stopped supporting most “older” PA-RISC workstations and 32-bit servers too.

In the late 2000s, HP ported HP-UX in an internal project to Intel x86 as a hedge during the architecture and operating systems consolidation of that decade. Porting target was a HP development system with 16 Intel CPUs on four mainboards. Development was stopped soon after, as HP committed to HP-UX on IA64 and Windows.

NeXTSTEP on PA-RISC

NeXTSTEP on PA-RISC was a commercial operating system based on Mach and BSD, with an Unix userland and modern GUI. Introduced in 1989, NeXTSTEP originally supported custom NeXT computers (“black” hardware, based on Motorola 68000) in the first few releases and pioneered many modern computer technologies such as the first web browser, UI concepts and an appstore.

NeXTSTEP releases 1.0/0.9 to 3.0 in 1992 only supported black NeXT hardware, with NeXTSTEP 3.1, support for “white” Intel i386 hardware was added to broaden the supported user base. For NeXTSTEP 3.3 the decision was made to support new RISC architectures: PA-RISC and SPARC.

NeXTSTEP was ported to PA-RISC with version 3.3, released in 1994. NeXTSTEP/hppa was developed specifically for the HP 9000 712 pizzabox workstation, support by HP engineers who worked on the NeXTSTEP kernel. Applications were supported through “fat” binaries, which supported multiple architectures on NeXTSTEP. Support for PA-RISC in NeXTSTEP was only brief and limited to a select set of 32-bit HP 9000 workstations in version 3.3, which was removed in the follow-on OPENSTEP 4.0.

NeXT and NeXTSTEP, while revolutionary in aspects, did not have much commercial success. OPENSTEP was supported until the late 1990s, which also included development of OPENSTEP APIs for Windows (NT), and a later acquisition by Apple. NeXTSTEP ideas and technologies lived on in Apple MacOS.

For the 1990s, NeXTSTEP on HP 9000 712 workstations was a rather unique and modern operating system experience compared to other Unix and RISC systems.

Other Unix

There were a few other notable operating systems ported to PA-RISC. HP’s own MPE business mainframe operating system was ported from the HP 3000 CISC platform to PA-RISC with MPE/XL and MPE/iX, with several releases from 1988 to 2002.

Several third-party Unix operating systems for PA-RISC mainframes were developed by companies for their own computers. This includes Convex SPP/UX, a heavily modified Mach-based operating system familiar to HP-UX for Exemplar SPP mainframes. Fault-tolerant Continuum servers from Stratus were also shipped with Unix, Stratus FTX, a System V Unix, or Stratos VOS, a transaction-processing oriented system.

In the mid-1990s, as part of the Precision RISC Organisation PA-RISC consortium, some Asian PA-RISC OEMs started selling their own PA-RISC computers. These either made use of licensed HP-UX versions or their own custom developed operating systems— like Hitachi with HI-UX/WE2 and HI-UX/MPP or Samsung with SS-UX.

Even other commercial

Besides well known commercial systems and research projects, some interesting operating systems were ported to PA-RISC. Forgotten since, Windows NT and NetWare were ported to PA-RISC in the 1990s as development projects.

Another PA-RISC operating system by HP was HP-RT, a real-time operating system geared towards instrumentation use cases on HP 9000 740 series VME workstations that had a short-ish lifespan between 1993 and 1997, when “customers have migrated to new solutions and platforms more rapidly than anticipated.”

4.15.3 Open Source: Linux and BSD

Open source operating systems on PA-RISC became popular through the mid-1990s Mach research ports, which laid the groundwork for more modern and complete open source systems. Mainstream Linux and OpenBSD both started around 1998 to port their respective systems to PA-RISC, and made use of Mach 4 for PA-RISC sources.

HP soon supported the PA-RISC Linux port and made documentation public. Linux on PA-RISC was integrated into the mainline 2.3 kernel in the early 2000s, followed by stable OpenBSD releases. PA-RISC Linux shipped in official Linux distributions, but has been scaled back slightly during the 2010s to be an Debian Port.

Linux on PA-RISC

A native Linux port to PA-RISC was started in 1999 and gained momentum when HP started helping with equipment and documentation in 1999. The main Linux port quickly superseded the earlier Mach-based MkLinux. Because of HP's assistance, the machines targeted at that time were newer than what other ports supported, like the A180, B180 and 64-bit PA 2.0 systems.

PA-RISC support was included in the mainstream kernel, and shipped with Debian and Gentoo distributions as official ports. During the 2010s however, support declined and development was scaled back, resulting in the eventual removal of PA-RISC from official distributions. PA-RISC Linux still has the broadest support for systems and hardware from the current open source efforts.

Development

In the late 1990s, PA-RISC was the last “big” RISC/Unix architecture without a proper Linux port, besides the limited Mach-based MkLinux. This had multiple reasons— PA-RISC systems were not widely used in academia but had a stronger market share in the technical and industrial world, from which they did no escape for a longer time than others. HP only reluctantly released technical documentation on their systems to the public in those times, which limited interest in and progress of development efforts.

Slow progress was made in 1999 with the initial start of the original Linux kernel on PA-RISC, as there was growing interest in these machines when more made their way into the second-hand market, and finally more documentation was released.

The Puffin Group

Early work on PA-RISC Linux started in 1999 with the help of The Puffin Group, which later employed several kernel and toolchain developers. Development was at first directed towards 32-bit systems; later on, with the help of HP, more modern machines were made available to developers, resulting in better hardware and 64-bit support.

Puffin Group developed much of the initial PA-RISC compiler and tool chain work.

HP support

In late 1999, HP started supporting and sponsoring PA-RISC Linux and the Puffin Group, in parallel to its Itanium (ia64) Linux undertakings. Earlier ports like Mach and MkLinux did not support newer 64-bit PA-RISC 2.0 computers, and had limited support for only SOM, not ELF binaries.

HP supported the port with developers, code, opening up PA-RISC documentation and sponsoring actual HP 9000 computers. Several important parts of the Linux kernel PA-RISC support were written by HP employees in the project. HP's support activities were channeled through the new Open Source Solutions Operation unit.

HP distributed HP 9000 PA-RISC computers to developer groups – there were at least HP 9000 A180 and A400 servers used for development. Most PA-RISC work was integrated around 2001 into Linux 2.3 with the majority committed into Linux 2.4, which booted. Stable support depended on solid PA-RISC support in gcc compiler and toolchain, which was added in gcc 2.95.

PA-RISC Linux sponsoring and organizational affiliations changed multiple times after that. HP and developer involvement fluctuated since then, but the port reached a stable state in the late 2000s and Linux distributions like Debian started to pick PA-RISC into their ports tree.

ESIEE

Contributed by Thibaut Varene

The PA-RISC Linux port effort started at the French network of graduate schools ESIEE (École Supérieure d'Ingénieurs en Électrotechnique et Électronique) in December 1999, with Thierry Simonnet, who was then managing the General IT Resources Service at ESIEE getting involved in the early stages of the port. In 2000, Simonnet decided to get students involved and started a case study as part of their school curriculum. The study was conducted in parallel by HP Labs, who sponsored the effort of the school, being a long time partner. This enabled the students to acquire skills, the study was completed in 2001 and presented at Linux Expo in Paris and at the Debian 1 Conference in Bordeaux, France.

With its increasing success, the initial case study spawned into a larger project that was open to students on their free time or as part of their classes, and more joined what was to be called the PATeam. From 2001 to the end of 2003, the team has been very active, doing PA-RISC development in the Linux kernel with writing drivers and improving overall stability. In 2004 and thereafter, ESIEE gradually reduced its support for the project.

OpenBSD and NetBSD on hppa

Work on an OpenBSD port to PA-RISC, OpenBSD/hppa, was started by the late Michael Shalayeff around 1999 in NYC. It was based on information and code from previous Mach porting efforts Lites/HPPA and MkLinux.

The first more or less complete OpenBSD/hppa release was version 3.5, albeit still with limitations many unsupported machines and I/O devices. PA-RISC has since been supported in OpenBSD on most 32-bit workstation, some 64-bit workstations and some servers. An OpenBSD/hppa64 port to support PA-RISC 2.0 computers running in 64-bit mode was started in 2007, but was discontinued after 2016.

NetBSD/hppa another free, open source Unix-like operating system, supports PA-RISC computers since 2005, called NetBSD/hp700 until the 7.0 release, as a “Tier II” port. The port focuses on 32-bit PA-RISC 1.1 computers and 64-bit PA-RISC 2.0 systems in 32-bit. The current effort is largely based on Michael Shalayeff’s work on the OpenBSD/hppa kernel from 2004 to 2005 and updated OpenBSD code later on.

4.15.4 Research: Mach and OSF

As soon as PA-RISC was released in the late 1980s, academic and industrial research projects started operating systems ports to PA-RISC. Several other operating systems have been ported to the PA-RISC platform over the time between the late 1980s and late 1990s. Most of them only reached development state and have long been unmaintained. Documentation is rare, some of it only in archives.

HPBSD on HPPA

The premier PA-RISC research system was HPBSD from the University of Utah, a port of 4.3BSD and later 4.4BSD to early HP 9000 800 servers and 700 workstations. HPBSD was born on 68k-based systems in 1987 when Mike Hibler started a port of 4.3BSD to HP 9000/320 and 350 workstations at the University of Utah. Major development lasted until about 1991 with the final addition of Motorola 68040 support.

In 1989, Jeff Forys started work on a HP 9000/800 port based on the hybrid HP-UX/Mach kernel called **HP Tut** done as an experiment at HP Labs. By 1990, HPBSD was running on an 9000/835 and later that year solidly on PA-RISC. For a short period of time in 1989-90, Mt Xinu also worked on the PA-RISC port and produced the first usable part of it, the boot loader, late in 1989. HPBSD used this boot loader.

In 1990 another Mach project was spun off of HPBSD—the Mach 3/UX single server port for the 9000/835 sponsored by HP and primarily done by Bob Wheeler. Starting in May 1991, Leigh Stoller ported HPBSD to the HP 9000/720 workstation, after which support for PA-RISC 1.0 and the 9000/800 platform was dropped.

The last major development to HPBSD was the addition of the 4.4BSD kernel filesystem and networking code and the 4.4BSD ANSI-compliant C library. Jeff Forys started this in 1992 and by 1993 all of the University of Utah HPBSD machines had been converted. This version was known as HPBSD 2.0. Since this merge included the NFS implementation done by Rick Macklem, all Sun-encumbered code could be eliminated.

In April 1993, a semi-formal release of HPBSD 2.0 was made to the 2-3 sites which had the necessary agreements with HP that were necessary to obtain HPBSD PA-RISC. After that, active development of HPBSD had pretty much stopped. As of Summer 1999, there were less than ten HPBSD machines

left. The last efforts were HP-UX compatibility 10.20 for the JDK and a 3Com EISA 100 Mbit ethernet driver.

Taken from the original Utah webpage, modified, with permission from Mike Hibler

Mach Microkernel on PA-RISC

Several ports of the Mach microkernel were undertaken during the early 1990s, with HP Tut using Mach 2.0 and the University of Utah trying Mach 3 and Mach 4. Porting efforts for OSF/1, the alliance Unix operating system from DEC, IBM, HP and others to compete with AT&T and Sun's System V Unix, started around 1990.

The first Mach 3 port to PA-RISC was Mach 3/UX from the University of Utah around 1991, one of the first various Mach microkernel ports to PA-RISC. This project targeted a proper port of Mach to PA-RISC on HP 9000/835 servers, where the HP-internal HP Tut somehow failed. Mach 3/UX never got very far, but code wound up later in Mach 4/Lites and probably MK-PA from OSF.

The University of Utah Flux Research Group ported the original Mach microkernel with a 4.4BSD-Lites server around 1994 to the PA-RISC architecture, based on the work of the Mach 3/UX project, and called it Mach 4/Lites. There was not much support provided and few enhancements made over the years, and it was quickly discontinued in favor of other projects both at Utah University and elsewhere, for example the MkLinux port. The project was seen from the beginning not as a complete operating system but rather as a snapshot for developers.

The operating system kernel is based on a Mach kernel, derived from CMU's (Carnegie Mellon University) MK83 release, and is loosely referred to as Mach 4. It contains some initial work done at Utah as part of the ARPA-funded *Fast and Flexible Mach Systems* work. In particular it contains a prototype implementation of migrating threads and a basic framework for signature-based remote procedure calls, a fundamental component of the presentation/interface work. None of these features is used either by the Lites server or within the kernel itself.

Also included is additional code never integrated into Mach 4, that was part of Utah's earlier Mach 3/UX and HPBSD ports or HP OSF/1. The former includes bus configuration and rudimentary device drivers for the CIO bus based workstations and servers as well as a remote kernel/task debugging facility developed by Convex. The latter includes some basic EISA support and alternative LAN drivers.

Taken from the original Utah webpage, modified, with permission from Mike Hibler

OSF/1 Unix on PA-RISC

HP itself ported OSF/1 to PA-RISC, which was never widely available commercially. This port was superseded in the mid-1990s by the OSF RI Open Group Research Institute with several releases of MK-PA. All of the Mach ports were never really used widely as production systems, but formed the basis for other research projects and later the BSD and Linux ports.

The OSF Open Group Research Institute ported OSF/1 to PA-RISC in the mid-1990s as research project, focusing on 32-bit HP 9000/700 workstations and servers. Porting was supported by HP in some way. Research releases were MK6.0-PA in 1994, MK6.3-PA in July 1995 and MK7-PA and MK7.2-PA in 1996. OSF MK-PA was never released widely, but used for research purposes, including ARPA projects (including radar tracking). Obtaining MK-PA from OSF RI required an OSF/1 source license.

MK-PA as research project wanted to demonstrate PA-RISC as OSF RI reference platform, performance parity between HP-UX and MK based systems, HP-UX binary compatibility, high-speed networking

capability.

The version of Mach 3 used by the OSF porting effort contained several of the Mach 4 enhancements of the University of Utah and probably used parts of the Mach 3/UX PA-RISC codebase. Parts of the MK-PA port itself were then used as base of the OSF port of Linux onto OSF Mach, MkLinux, which in turn was the base of several other PA-RISC porting efforts in the 2000s.

MkLinux on PA-RISC

Early Linux support on PA-RISC built upon the MkLinux research project from the mid-1990s by the Open Group/OSF, that ported a Linux kernel onto a Mach microkernel, which in turn built on the previous MK-PA OSF/1 port to PA-RISC.

MkLinux was a 1990s project led by Apple and Open Group Research Institute to port Linux hosted on top of a Mach microkernel (pmk1.1) to run an Apple PowerPC computers like PowerBooks. A research project between Open Group and OSF ported that system later to PA-RISC computers, supported by HP, with first PA-RISC development releases were in 1997.

MkLinux was the first free operating system that truly worked on PA-RISC hardware, in contrast to the various Mach ports, which suffered from unfinished development and a lot of bugs on PA-RISC. MkLinux on PA-RISC built on the previous OSF/1 MK-PA port and integrated parts from the PA-RISC kernel sources from the Utah University, including Mach 3/UX and Mach 4/Lites. MkLinux improved the underlying OSF PA-RISC/Mach kernel from MK-PA put a Linux 2.0 kernel as server personality on top, replacing BSD/Lites from the previous efforts. Included were X11R6 patches, the GNU ELF compiler and debugger and complete /usr and /var directories.

Other Microkernel on PA-RISC

An internal HP research project was **HP Tut** from around 1988-89 to port HP-UX onto a Mach microkernel. The project apparently never succeeded far and moved on to merging parts of Mach 2.0 under HP-UX 2.0 to get something close to resembling Mach on PA-RISC. HP Tut was the basis for various other porting efforts and PA-RISC research projects within and outside of HP.

Another micro-kernel operating system was Chorus by INRIA with a development port to PA-RISC done in 1990-1991 at the Oregon Graduate Institute (OGI) for PA-RISC 1.0 HP 9000/834 servers ("workstations"). This port was based on Chorus v3.3/MiX v3.2. Hardware support and functionality was limited, with apparently no network interfaces or disk devices supported and console I/O depending on PDC and IODC routines.

Code from various earlier projects was used, including from HP-UX 2.0 and HP Tut, HP-UX on 2.0 Mach. A later project ported Chorus v3.4 to the 9000/720 workstation a popular target for OS/Unix porting efforts at that time.

4.15.5 Timeline

Table 4.17: PA-RISC operating systems, ■ - full support, ◇ - partial

Year	HP-UX	Linux	OpenBSD	NetBSD	HPBSD	Mach 3	Mach 4	OSF/1	MkLinux	NeXT
Type	Unix	Open Source			Research					Unix
1986	◇									
1987	◇									
1988	◇									
1988	◇									
1989	■ ■				■					
1990	◇				■			◇		
1991	■				◇	◇		◇		
1992	■				◇					
1993	◇				■					
1994	◇						◇	■		■
1995	■						◇	■		
1996	■ ■						■	■		
1997	■ ■								◇	
1998	◇	◇							◇	
1999	◇	◇	◇							
2000	■ ■	◇	◇							
2001	■	◇	◇							
2002	■	■	◇							
2003	◇	◇	■							
2004	◇	◇	■ ■	◇						
2005	■	■ ■	■ ■	■						
2006	◇	◇	■ ■	■						
2007	■	■ ■	■ ■	■						
2008	◇	■	■ ■							
2009	◇	■	■ ■	■						
2010	◇		■ ■	■						
2011	◇	◇	■ ■							
2012	◇	◇	■ ■	■ ■						
2013	◇	◇	■ ■	■						
2014	◇	◇	■ ■							
2015	◇	◇	■ ■	■						
2016	◇	◇	■ ■							
2017	◇	◇	■ ■	■						
2018	◇	◇	■ ■	■ ■						
2019	◇	◇	■ ■	■						
2020	◇	◇	■ ■	■ ■						
2021	◇	◇	■ ■	■						
2022	◇	◇	■ ■	■						
2023	◇	◇	■ ■	■						
2024	◇	◇	■ ■	■						

4.15.6 Further reading

- ◇ For more technical information see the PA-RISC Operating Systems page, with details on release timelines and introduction dates on the PA-RISC Timeline.
- ◇ PA-RISC Linux Project History, PA-RISC Linux Wiki, OLD NEWS, 2024
- ◇ HPBSD: Utah's 4.3bsd port for HP9000 series machines Original homepage of the HPBSD project. Mike Hibler (July 1999: University of Utah)
- ◇ The Utah PA-RISC Code Snapshot Original webpage of the project. Mike Hibler (2002: University of Utah)
- ◇ MK-PA: An HP-UX compatible microkernel based Operating System, The Open Group (1998)
- ◇ MK-PA Project Update, James Loveluck (1996: The Open Group)
- ◇ OSF MK 7.2, OSF RI (1997: , accessed February 2018)
- ◇ HEWLETT-PACKARD PUTS OSF/1 ON HOLD AS IT MERGES DOMAIN WITH HP-UX, Computer Business Review, March 22, 1992
- ◇ MkLinux - Linux on the OSF Microkernel, The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ MkLinux for HP PA-RISC, The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ Release Notes for MkLinux on HP PA-RISC Descriptions on MkLinux and extensive installation instructions. The Open Group (1997, archived by CIRR 1999, current mirror MkLinux.org accessed 2022)
- ◇ Sun and NeXT throw open the doors to industry-standard object-oriented computing and Technical Implications, NeXTWORLD 1993 February (nextcomputers.org 2023)

Chapter 5

Appendix

5.1 Print History

Table 5.1: OpenPA print releases changes

Release	Files changed	Lines added	removed	modified
3.0				
2.9				
2.8	92	1336	1113	1456
2.7	48	96	360	1244
2.6	90	210	1753	9378
2.5	91	2048	1936	7636
2.4	70	818	1668	2422
2.3	52	1141	269	1306
2.2	69	1080	917	1975
2.1	18	315	29	170
2.0	56	2262	183	2377
1.2	-	-	-	-
1.1	14	157	406	775
1.0	-	-	-	-

Changes in the current Edition 3.0 since the last edition (2024):

- ◇ PA-RISC Architecture and Precision
- ◇ HP Visualize Intel-based Workstations
- ◇ HP Visualize 3D accelerators
- ◇ HP Visualize for Intel graphics
- ◇ Unix games for HP-UX
- ◇ ATI and nVIDIA graphics for PA-RISC and Itanium
- ◇ Research operating systems for PA-RISC
- ◇ More HP-RT content
- ◇ PA-RISC performance and SPECtable
- ◇ SAIC Talon portable computer
- ◇ QEMU PA-RISC emulation

Changes in the Edition 2.9 since the last edition (2022):

- ◇ PA-RISC Research Operating Systems detailed out
- ◇ Revised PA-RISC timeline, introduction dates
- ◇ More systems descriptions and better text
- ◇ New article on Apollo and PRISM
- ◇ New article on PA-RISC history
- ◇ New content on PRO and PA-RISC in Japan

- ◇ New article on OpenPA and Internet sources
- ◇ New article on Oddball operating systems (NT, Netware)
- ◇ New article on HP-RT
- ◇ Much more content on HP-UX
- ◇ Many corrections (again thanks!)

Changes in Edition 2.8 since the last edition (2020):

- ◇ Many revisions and corrections (thanks!)
- ◇ Text and language in all chapters
- ◇ TeX backend update

Changes in Edition 2.7 since the last edition (2018):

- ◇ HP 9000 and PA-RISC Computers Story article added
- ◇ OpenPA.net turned twenty in 2019
- ◇ Many updates to PA-RISC computers articles
- ◇ HP 9000 520 FOCUS article updated
- ◇ HP 9000 743/744 VME article update and extended for VXI boards
- ◇ PA-RISC in US Navy DTC and TAC information added
- ◇ Many revisions and corrections (thanks!)
- ◇ HP Agilent 16600 and 16700 PA-RISC logic analyzers article added

Changes in Edition 2.6 since the last edition (2016):

- ◇ HP 9000 and PA-RISC history article
- ◇ Operating system reference table
- ◇ Major housecleaning of almost all articles
- ◇ Separate PA-RISC chipsets pages
- ◇ Extended chipset and system architecture information

Changes in Edition 2.5 since Edition 2.4:

- ◇ (2.5.1) BSD operating system support updated (OpenBSD and NetBSD)
- ◇ PA-RISC System Architecture section integrated into the Chipset section, with multiple PA-RISC platform designs from the early 1980s to mid-2000s
- ◇ PA-RISC hardware and operating systems timeline added
- ◇ PA-RISC entry dates and prices added
- ◇ Many dead links to official documentation and resources removed (404)
- ◇ Wording and spelling corrections, several sections rewritten

- ◇ Stats: 91 files changed, 2048 insertions, 1936 deletions 7636 modifications (lines)

Changes in Edition 2.4 since Edition 2.3:

- ◇ Architecture and ISA pages improved
- ◇ HP-UX 11.x sections extended
- ◇ Processor sections improved
- ◇ Buses and SCSI sections improved
- ◇ Chipset section extended (Stretch, zx1, others)
- ◇ T-Class pages added
- ◇ Corrections to the PA-RISC OEM systems
- ◇ Operating systems pages updated
- ◇ Wording and spelling corrections

Changes in Edition 2.3 since Edition 2.2:

- ◇ Wax I/O adapter added
- ◇ CPU bus attachments of the PA-RISC processors added
- ◇ Memory and I/O controllers updated and extended
- ◇ HP-UX and other operating system support updated and revised
- ◇ Many pages rewritten and updated with general corrections
- ◇ More price and introduction date information for various HP 9000 systems

Changes in Edition 2.2 since Edition 2.1:

- ◇ Removal of several outdated pages: PDC Boot-ROM (only relevant to older systems, incomplete), LED error codes (same), Expansion cards (outdated and incomplete, just a collection of HP part numbers) and Memory modules (same)
- ◇ Almost all other pages have been updated and/or rewritten, especially the hardware sections (processors, chipsets, buses)

Changes in Edition 2.1 (October 2008) since Edition 2.0 (22 pages added):

- ◇ Convex Exemplar SPP1000, SPP1200 and SPP1600 (XA and CD) mainframes added
- ◇ HP/Convex Exemplar SPP2000 (S-Class/X-Class) mainframes added
- ◇ 3rd party PA-RISC computers information added: more Hitachi (3050RX, 3500 and 9000V OEM) and Mitsubishi (MELCOM ME RISC) and Oki (OKITAC 9000) OEM systems (relabelled HP)
- ◇ HP 9000/V2200 and V2250 Exemplar mainframes added
- ◇ HP 9000/V2500 and V2600 Exemplar mainframes added
- ◇ Cover page and several post-release spelling corrections

Changes in Edition 2.0 (May/June 2008) since Edition 1.2 (about 90 pages added and almost all other updated/modified):

- ◇ HP Itanium/IA64 servers added: rx1600/rx1620, rx2600/rx2620, rx4610, rx4640 and rx5670
- ◇ HP Itanium/IA64 workstations added: i2000, zx2000 and zx6000
- ◇ Much improved Other PA-RISC Operating Systems page (Mach 4/Lites, HPBSD, OSF/1, Mach 3, Chorus, and others)
- ◇ HP 9000 N4000 (rp7400) server section added
- ◇ Stretch and Cell-based (Superdome) chipset sections added
- ◇ HP 9000 N4000 (rp7405 and rp7410) server section added
- ◇ HP 9000 L1500 (rp5430) and L3000 (rp5470) server section added
- ◇ HP 9000 rp3410 and rp3440 (*rp3400 series*) server section added
- ◇ HP 9000 rp4410 and rp4440 (*rp4400 series*) server section added
- ◇ Reworked and more detailed HP 9000/500 FOCUS systems section
- ◇ Expanded and corrected early PA-RISC history/servers section
- ◇ Early PA-RISC 1.0 processors (TS-1, NS-1, NS-2, CMOS26B/PCX) section added
- ◇ Much improved and expanded Stratus Continuum servers section
- ◇ Winbond W89K and W90K embedded PA-RISC processors section added
- ◇ Synchronize with online OpenPA.net content
- ◇ Typographic polishing (T_EX and in the HTML sources)
- ◇ Improvements to and streamlining of the HTML-to-PDF conversion process
- ◇ Removal of (book-format) DIN A5 print format

Changes in Release 1.2 (December 2007) since First Edition 1.1:

- ◇ Typographic modifications for limited print edition

Changes in Release 1.1 (November 2007) since First (Prerelease) Edition 1.0:

- ◇ Text formatting and positioning
- ◇ Typographic improvements
- ◇ Addition of a (book-format) DIN A5 print format
- ◇ PA-RISC History page added, covering the early PA-RISC days
- ◇ Catch-up with all changes/updates from the OpenPA online edition (about one year worth of updates)

First (Prerelease) Edition 1.0 was published in July 2006.

5.2 SPEC Benchmarks

The processing power of PA-RISC and HP 9000 computers was often measured by industry benchmarks to compare the speed with other vendors. Frequently used in the 1990s and 2000s were SPEC scores in CPU92, CPU95 and CPU2000 varieties, as quoted in press releases, magazines and websites for comparing CPUs and workstations.

5.2.1 SPEC

SPEC, Standard Performance Evaluation Corporation, is a non-profit corporation founded in 1988 by workstation vendors to develop “fair and useful set of metrics to differentiate” Unix and computer systems. SPEC benchmarks are based on “standardized suite of source code” that have been “ported to a wide variety of platforms,” which then is compiled and tuned on target (benchmarked) systems.

SPEC both developed the benchmarks, source code and testing methodology and published the results in regular publications. Relevant are scores from SPEC’s Open Systems Group (OSG) for “processor and system benchmarks in an UNIX/NT/VMS environment,” including SPEC92, SPEC95 and SPEC2000 integer and FP scores for computing speed and SPEC95 and SPEC2000 rate scores for throughput (SMP capacity).

SPEC CPU92 was released in 1992 with CINT92 for integer computing (6 benchmarks written in C) and CFP92 floating-point operations (12 written in C, 2 in Fortran), with a DEC VAX11/780 as reference score.

SPEC CPU95 was released in 1995 as replacement for CPU92 with SPECint92 and SPECfp92 and significant changes to testing: Benchmarks were bigger to not fit into L1 caches, ran longer (minutes instead of seconds) and were more realistic, robust and consistent. Reference system was a Sun SPARCstation 10/40.

SPEC CPU2000 was the eventual successor to CPU95, after SPEC skipped the CPU98 version. CPU2000 consisted of two metrics: CINT2000 (12 benchmarks written in C and C++) and CFP2000 (14 benchmarks in FORTRAN and C) metrics, with a Sun Ultra 5 workstation as reference score.

5.2.2 PA-RISC and HP 9000

The following table is a collection of assorted SPEC92, 95 and 2000 scores for PA-RISC and HP 9000 systems from HP literature, websites and product briefs.

Table 5.2: PA-RISC computers SPEC benchmarks results

System	SPEC92int/fp	SPEC95int/fp	SPEC95 rate int/fp	SPEC2000int/fp	SPEC2000rate int/fp
705	21.9/33.0				
710	31.6/47.6	1.0/1.4			
712/60	67.0/85.3	2.1/2.7	18.7/23.9		
712/80	97.1/123.3	3.1/3.5	28.1/32.0		
712/100	117.2/144.2	3.8/4.1	33.8/36.3		
715/33	32.5/52.4	1.0/1.6			
715/50	49.2/78.8	1.5/2.5			
715/64	80.6/109.4	2.5/3.3			
715/75	82.6/127.2	2.5/3.8			

715/80	96.3/123.2	3.0/3.5			
715/100	115.1/138.7	3.8/4.0	30.0/38.3		
715/100XC	132.2/184.6	4.5/4.7	40.9/42.3		
720	36.4/58.2	1.2/2.0	14.1/18.2		
725/50	37.1/72.8	1.5/2.5			
725/75	80.3/126.8	2.5/3.8			
725/100		3.8/4.0			
730	47.8/75.4	1.5/2.3			
735/99	109.1/167.9	3.2/4.1	29.4/35.8		
735/125	136.0/201.0	4.0/4.6	36.3/40.9		
742i/50		1.5/2.5			
743i/64		2.5/3.3			
743i/100		3.8/4.0			
744/132L		6.4/6.7			
744/165L		7.9/7.6			
745i/50		1.5/2.5			
745i/100		3.2/4.1			
745/132L		6.4/6.7			
745/165L		7.9/7.6			
747i/50		1.5/2.5			
747i/100		3.2/4.1			
748i/64		2.5/3.3			
748i/100		3.8/4.0			
748/132L		6.4/6.7			
748/165L		7.9/7.6			
750	48.1/75.0	1.5/2.3			
755/99	109.1/167.9	3.2/4.0	29.4/35.8		
755/125	136.0/201.0	4.0/4.6	36.3/40.9		
A180					
A180C		9.2/8.6			
A500-5X				422/414	9.3/7.6
A500-7X				581/	6.74
B132L		6.4/6.7	58.1/60.3		
B132L+		6.8/7.2	61.5/64.6		
B160L		7.7/7.6	69.7/68.1		
B180L+		9.2/9.4	83.0/84.8		
B1000		23.9/39.3	217/378		
B2000		31.8/52.4	286/472	332/357	3.8/4.1
B2600				403/440	4.7/5.1
C100	140.0/224.0	5.0/6.6	44.8/59.4		
C110	167.0/269.0	6.0/8.1	54.0/73.3		
C132L		6.4/6.7	58.1/60.3		
C160L		7.7/7.6	69.7/68.1		
C160		10.4/16.3	93.6/147		
C180		11.8/18.7	107/169		
C200		14.2/21.4	129/193		
C240		17.1/25.4	156/229		
C360		26.0/28.1	234/252		
C3000		31.8/52.4	287/471	313/321	

C3600		42.0/64.0	379/576	432/433	5.0/5.0
C3650				508/542	5.9/6.3
C3700				604/576	7.0/6.7
C3750				678/674	
C8000				1001?/	
D200	115/146	2.2/2.9	19.2/25.8		
D210	152/194	3.7/4.1	33.6/36.7		
D220		6.6/6.7	59.2/60.5		
D230		7.9/7.6	70.8/68.3		
D250	144/218	5.0/6.8	45.1/61.0		
D260			2P: 114/143		
D270		10.4/15.0	93.9/135		
D280		12.3/17.4	111/157		
D300	115/146	2.2/2.9	19.2/25.8		
D310	152/194	3.7/4.1	33.6/36.7		
D320		6.6/6.7	59.2/60.5		
D330		7.9/7.6	70.8/68.3		
D350	144/218	5.0/6.8	45.1/61.0		
D360			114/143		
D370		10.4/15.0	93.9/135		
D380		12.3/17.4	111/157		
D390		15.5/25.5			
E25	45.0/66.7				
E35	65.6/98.5				
E45	82.1/122.9				
E55	108.0/163.4				
F10	22.0/36.6				
F20	33.6/56.1				
F30/G30/H30/I30	37.8/62.4				
G40/H40/I40	65.2/91.3				
G50/H50/I50	100.0/158.5				
G60/H60/I60	108.8/195.3				
G70/H70/I70	108.8/195.3				
Galaxy 1100		3.1/3.5			
i2000 733				FP 623	FP 7.2
i2000 800				365/610	
J200	139.4/222.5	5.0/4.5	44.8/61.3		
J210	168.7/269.2	6.0/5.4	54.0/73.4		
J210XC	183.9/305.9	6.4/5.7	57.6/81.5		
J280		11.8/19.3	107/174		
J282			211/261		
J2240		17.4/26.3	157/237		
J5000		32.5/54.0	302/486		
J5600		42.6/62.7	384/564		
J6000		42.6/62.7	384/564	441/433	9.7/8.0
J6700		57.6/85.9		603/581	13.4/10.5
J6750				676/651	14.9/11.5
J7000		32.5/54.0	302/486		
K100		4.9/6.8			

K200		4.9/6.8	44.3/61.2		
K210		5.9/8.1	53.3/73.4		
K220		6.4/9.1	57.7/82.0		
K250		10.7/18.8	96.0/169		
K260		11.8/20.2	107/182		
K370		14.6/23.0	132/207		
K380		17.4/28.5	157/257		
K400	136.7/221.2	4.9/6.8	44.3/61.2		
K410		5.9/8.1	53.3/73.4		
K420		6.4/9.1	57.7/82.0		
K450		10.7/18.8	96.0/169		
K460		11.8/20.2	107/182		
K570		14.6/23.0	132/207		
K580		17.4/28.5	157/257		
L2000-44		33.7/72.3			
L3000-5X				388/376	4.5/4.4
L3000-7X				581	6.7
N4000-36			215/355		
N4000-44			306/462		
N4000-5X			376/528		
N4000-6X				493/489	5.7/5.7
N4000-7X				551/524	6.4/6.1
PrecisionBook 132		6.5/6.5			
PrecisionBook 160		7.8/7.4			
PrecisionBook 180		9.2/9.4			
R380		12.3/17.4			
R390		15.5/25.5			
rp3440					18.7/19.2
rp4440					18.6/19.3
rx1600				837/1382	9.7/16.0
rx1620-2				1452/2692	16.8/31.2
rx2600				674/1151	7.8
rx2600				1408/2119	15.3
rx2620-2				1535/2675	17.8/31.0
rx4610				379/701	4.4/8.1
rx4640				1132/1891	13.1/21.9
rx5670				1312/2108	IP: 15.2/24.5
T520		5.2	47.2-531		
T600		11.8/14.9	106/134 1192/1151		
V2200		13.8/22.1	125-1865/2312		
V2250		16.4/24.8	2209/2471		
V2500			4002-7481		
V2600			5164-9315		
SPP1000/XA		3.3/4.0			
SPP1200/XA	/185				
SPP1600/CD			290/383 996/1444		
SPP2000		11.8/18.7	92.5/1411307/1413		
zx2000 900				668/1086	/12.6
zx6000 900				669/1139	7.8/13.2

zx6000 I.5				1315/2106	15.2/24.4
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5.2.3 spectable - SPEC92 and SPEC95

During the 1990s, John DiMarco regularly posted collected SPEC benchmark scores to USEnet groups. His *spectable* contained SPEC92 and SPEC95 results from many different sources collected over time. Last releases of the table were in late 2000, when official results became more easily available and SPEC switched to SPEC2000.

The table disappeared around 20 years ago and is only available anymore on archive.org. Following are excerpted SPEC95 int/fp and SPEC92 int/fp scores for various vendors and CPU architectures from his table, dated Dec 8, 2000.

SPECint95, SPECfp95

Source: Table 3, John DiMarco (2000)

System Name	CPU (NUMx)Type	ClkMHz ext/in	Cache Ext+I/D	SPECint 95	SPECfp 95	Info Date	Source Obtained
API UP2000	A21264	??/750	8M+64/64	42.7	77.5	Sep00	www.specb
API UP2000	A21264	??/833	8M+64/64	49.4	95.6	Sep00	www.specb
Compaq DS20	A21264	83/500	4M+64/64	27.7	58.7	Feb99	www.dec
Compaq ES40	A21264	83/500	4M+64/64	27.3	57.7	Apr99	www.dec
Compaq ES40	4xA21264	83/500	4M+64/64	?	104	Apr99	www.dec
Compaq GS60	A21264	88/525	4M+64/64	27.7	42.5	Dec98	www.dec
Compaq GS140	A21264	88/525	4M+64/64	27.8	45.2	Dec98	www.dec
Compaq XP1000	A21264	83/500	4M+64/64	26.9	52.2	Jul99	www.specb
DEC 200/4/100	A21064A	??/100	?+16/16	1.88	2.79	Aug96	Digital
DEC 200/4/166	A21064A	??/166	?+16/16	2.95	3.64	Aug96	Digital
DEC 200/4/233	A21064A	??/233	?+16/16	4.28	4.32	Aug96	Digital
DEC 250/4/266	A21064A	??/266	2M+16/16	5.18	6.27	Apr95	www.dec
DEC 255/233	A21064A	??/233	1M+16/16	4.27	5.09	Mar96	Digital
DEC 255/300	A21064A	??/300	1M+16/16	5.23	5.81	Mar96	Digital
DEC 500/266	A21164	43/266	2M+96+8/8	7.93	11.1	Mar96	Digital
DEC 500/333	A21164	46/333	2M+96+8/8	9.82	12.5	Mar96	Digital
DEC 500/400	A21164	53/400	2M+96+8/8	12.3	14.1	Jun96	Digital
DEC 500/500	A21164	48/500	8M+96+8/8	15.0	20.4	Aug96	Digital
DEC 600/5/266	A21164	38/266	4M+96+8/8	7.91	11.8	Sep95	Digital
DEC 600/5/300	A21164	75/300	4M+96+8/8	9.78	13.4	Sep95	Digital
DEC 600/5/333	A21164	83/333	4M+96+8/8	9.23	13.2	Feb96	Digital
DEC 600A/5/500	A21164	??/500	8M+96+8/8	14.8	17.4	May97	www.dec
DEC PW433AU	A21164	??/433	2M+96+8/8	13.9	18.1	Jul97	www.specb
DEC PW500AU	A21164	??/500	2M+96+8/8	15.7	19.5	Jul97	www.specb
DEC PW600AU	A21164	??/600	2M+96+8/8	18.4	21.3	Jun97	www.specb
DEC 3000/500	A21064	30/150	512+8/8	2.15	3.65	Sep95	Digital
DEC 3000/700	A21064A	38/225	2M+16/16	3.66	5.71	Sep95	Digital
DEC 3000/900	A21064A	39/275	2M+16/16	4.24	6.29	Sep95	Digital
DEC 2[01]00/5/250	A21164	35/250	4M+96+8/8	5.96	8.39	Feb96	Digital

DEC 2[01]00/5/300	A21164	42/300	4M+96+8/8	7.03	9.64	Feb96	Digital
DEC 2[01]00/5/300	2xA21164	42/300	4M+96+8/8	?	14.0	Feb96	Digital
DEC 2100/5/300	4xA21164	42/300	4M+96+8/8	?	19.2	Feb96	Digital
DEC 4100/5/300E	A21164	??/300	96+8/8	7.15	12.0	May96	www.dec
DEC 4100/5/300E	4xA21164	??/300	96+8/8	?	18.4	May96	www.dec
DEC 4100/5/300	A21164	??/300	2M+96+8/8	8.11	12.7	May96	www.dec
DEC 4100/5/300	4xA21164	??/300	2M+96+8/8	?	21.8	May96	www.dec
DEC 4[01]00/5/400	A21164	??/400	?M+96+8/8	12.1	17.2	Sep96	Digital
DEC 4[01]00/5/400	2xA21164	??/400	?M+96+8/8	12.1	24.2	Sep96	Digital
DEC 4100/5/400	4xA21164	??/400	?M+96+8/8	12.1	33.4	Sep96	Digital
DEC 4[01]00/5/466	A21164	??/466	4M+96+8/8	14.1	19.2	Feb97	Digital
DEC 4[01]00/5/466	2xA21164	??/466	4M+96+8/8	14.1	26.5	Feb97	Digital
DEC 4[01]00/5/466	4xA21164	??/466	4M+96+8/8	14.1	36.1	Feb97	Digital
DEC 4[01]00/5/600	A21164	??/600	8M+96+8/8	18.8	29.2	Dec97	www.specb
DEC 8[24]00/5/300	A21164	75/300	4M+96+8/8	7.43	12.4	Feb96	Digital
DEC 8[24]00/5/300	2xA21164	75/300	4M+96+8/8	?	18.1	Feb96	Digital
DEC 8[24]00/5/300	4xA21164	75/300	4M+96+8/8	?	25.9	Feb96	Digital
DEC 8[24]00/5/300	6xA21164	75/300	4M+96+8/8	?	30.1	Feb96	Digital
DEC 8400/5/300	8xA21164	75/300	4M+96+8/8	?	33.5	Feb96	Digital
DEC 8[24]00/5/350	A21164	88/350	4M+96+8/8	10.10	14.2	Feb96	Digital
DEC 8400/5/350	8xA21164	88/350	4M+96+8/8	?	38.5	Feb96	Digital
DEC 8[24]00/5/440	A21164	88/440	4M+96+8/8	13.6	17.0	Oct96	Digital
DEC 8[24]00/5/440	6xA21164	88/440	4M+96+8/8	?	34.3	Oct96	Digital
DEC 8400/5/440	8xA21164	88/440	4M+96+8/8	?	42.6	Oct96	Digital
DEC 8200/6/575	A21264	96/575	4M+64/64	30.1	44.8	Jul98	Digital
DEC 8400/6/575	A21264	96/575	4M+64/64	30.3	47.7	Jul98	Digital
Dell DimensionXPS	Pentium	66/100	512+8/8	3.16	2.75	Jan96	www.intel
Dell DimensionXPS	Pentium	60/120	512+8/8	3.53	2.92	Jan96	www.intel
Dell DimensionXPS	Pentium	66/133	512+8/8	3.90	3.28	Jan96	www.intel
Dell DimensionXPS	Pentium	66/200	512+8/8	5.10	4.18	Sep96	www.intel
Dell DimensionXPS	PentPro	180	256+8/8	7.28	5.59	Sep96	www.intel
Dell DimensionXPS	PentPro	200	256+8/8	8.20	6.21	Sep96	www.intel
Dell DimensionXPS	PentPro	200	512+8/8	8.58	6.48	Sep96	www.intel
Dell Optiplex	Pentium	60/120	512+8/8	3.51	2.80	Jan96	www.intel
Dell Optiplex	Pentium	66/133	512+8/8	3.90	2.99	Jan96	www.intel
Dell PW410	PentiumII	100/350	512+16/16	13.4	11.0	Jun98	www.specb
Dell PW410	PentiumII	100/400	512+16/16	15.3	12.4	Jun98	www.specb
Dell PW410	PentiumII	100/450	512+16/16	17.6	13.1	Sep98	www.specb
Dell PW410	PentiumIII	100/650	256+16/16	31.5	23.5	Mar00	www.specb
Dell PW410	PentiumIII	100/700	256+16/16	33.7	24.3	Mar00	www.specb
Dell PW410	PentiumIII	100/750	256+16/16	36.1	25.1	Mar00	www.specb
Dell PW420	PentiumIII	133/600	256+16/16	30.0	27.7	Mar00	www.specb
Dell PW420	PentiumIII	133/733	256+16/16	35.8	31.0	Mar00	www.specb
Dell PW420	PentiumIII	133/800	256+16/16	38.9	32.4	Mar00	www.specb
Dell PW610	P2Xeon	100/450	512+16/16	18.9	14.7	Sep98	www.specb
Dell PW610	P3Xeon	100/500	512+16/16	21.6	15.5	Mar99	www.specb
Dell PW610	P3Xeon	100/500	1M+16/16	22.1	16.2	Mar99	www.specb
Dell PW610	P3Xeon	100/550	512+16/16	24.3	16.8	Apr99	www.specb
Fuji/ICL J650i	PentPro	200	512+8/8	8.71	6.68	May96	www.spec
Gateway P5-75	Pentium	50/75	256+8/8	2.31	2.02	Jan96	www.intel

Gateway P5-90	Pentium	60/90	256+8/8	2.74	2.39	Jan96	www.intel
Gateway P5-100	Pentium	66/100	256+8/8	3.05	2.72	Jan96	www.intel
Gigabyte GA71X	Athlon	200/750	512+64/64	33.0	26.5	Mar00	www.specb
HAL 330	SPARC64	100	128/128	4.2	7.73	Feb96	www.hal
HAL 350	SPARC64	118	128/128	4.9	9.03	Feb96	www.hal
HAL 375	SPARC64II	141	128/128	7.51	13.7	Sep97	www.hal
HAL 385	SPARC64II	161	128/128	8.51	15.3	Sep97	www.hal
HP 9000/712/60	PA7100LC	60	64	2.08	2.66	Oct96	www.hp
HP 9000/712/80	PA7100LC	80	256	3.12	3.55	Oct96	www.hp
HP 9000/712/100	PA7100LC	100	256	3.76	4.03	Oct96	www.hp
HP 9000/715/100	PA7100LC	100	256	3.76	4.03	Oct96	www.hp
HP 9000/715/100XC	PA7100LC	100	1M	4.55	4.70	Oct96	www.hp
HP 9000/735	PA7100	99	256/256	3.22	4.06	Sep95	SPEC
HP 9000/735	PA7100	125	256/256	3.97	4.61	Sep95	SPEC
HP 9000/B132L	PA7300LC	132	1M+64/64	6.45	6.70	Sep97	www.hp
HP 9000/B160L	PA7300LC	160	1M+64/64	7.75	7.56	Oct96	www.hp
HP 9000/B180L	PA7300LC	180	1M+64/64	9.06	9.35	Sep97	www.hp
HP 9000/C160	PA8000	160	512/512	10.4	16.3	Jun96	www.hp
HP 9000/C160L	PA7300LC	160	1M+64/64	7.75	7.56	Oct96	www.hp
HP 9000/C180XP	PA8000	180	1M/1M	11.8	18.7	Jun96	www.hp
HP 9000/C200	PA8200	200	1M/1M	14.2	21.4	Sep97	www.hp
HP 9000/C240	PA8200	236	2M/2M	17.1	25.4	Sep97	www.hp
HP 9000/D[23]20	PA7300LC	132	1M+64/64	6.5	6.7	Feb98	www.hp
HP 9000/D[23]30	PA7300LC	160	1M+64/64	7.8	7.5	Feb98	www.hp
HP 9000/D[23]70	PA8000	160	512/512	10.4	15.0	Feb98	www.hp
HP 9000/D[23]80	PA8000	180	1M/1M	12.3	17.4	Feb98	www.hp
HP 9000/J200	PA7200	100	256/256	3.52	6.32	Sep95	SPEC
HP 9000/J210	PA7200	120	256/256	4.21	7.60	Sep95	SPEC
HP 9000/J210	2xPA7200	120	256/256	?	10.10	Sep95	SPEC
HP 9000/J280	PA8000	180	1M/1M	11.8	19.3	Oct96	www.hp
HP 9000/J2240	PA8200	236	2M/2M	17.4	26.3	Jan98	www.hp
HP 9000/K420	PA7200	120	1M/1M	4.61	8.24	Feb96	www.hp
HP 9000/K260EG	PA8000	180	1M/1M	11.8	19.4	Jun96	www.hp
HP 9000/K460EG	PA8000	180	1M/1M	11.8	20.2	Jun96	www.hp
HP 9000/K[35]70	PA8200	200	2M/2M	14.6	23.0	Jul97	www.specb
HP 9000/V2200	PA8200	200	2M/2M	?	22.1	Dec97	www.specb
IBM 250	MPC601	66	32	1.82	2.32	Sep96	www.ibm
IBM 380	POWER2	59	32/64	2.84	7.20	Sep96	www.ibm
IBM 390	POWER2	67	32/64	3.14	7.50	Sep96	www.ibm
IBM 390	POWER2	67	1M+32/64	3.25	7.71	Sep96	www.ibm
IBM 397	POWER2SC	160	32/128	8.61	25.8	Oct97	www.ibm
IBM 397	POWER2SC	160	32/256	8.62	26.6	Oct98	www.ibm
IBM 590	POWER2	66	32/256	3.33	10.4	Sep96	www.ibm
IBM 591	POWER2	77	32/256	3.84	12.4	Sep96	www.ibm
IBM 595	POWER2SC	135	32/128	6.17	17.6	Oct96	www.ibm
IBM 860	MPC603e	166	256+16/16	3.94	2.71	Oct96	www.ibm
IBM E20	MPC604	100	512+16/16	3.67	3.13	Jun96	www.ibm
IBM [EF]30	MPC604	133	512+16/16	4.74	3.49	Jun96	www.ibm
IBM E30	MPC604	233	512+16/16	9.41	6.01	Oct98	www.ibm
IBM F40	MPC604e	166	512+32/32	5.73	4.75	Oct96	www.ibm

IBM F40	MPC604e	233	1M+32/32	8.71	5.87	Oct98	www.ibm
IBM 39H	POWER2	67	1M+32/128	3.29	9.61	Sep96	www.ibm
IBM 39H	POWER2	67	2M+32/128	3.42	10.2	Sep96	www.ibm
IBM 42[TW]	MPC604	120	16/16	3.21	2.74	Sep95	www.ibm
IBM 42[TW]	MPC604	120	512+16/16	4.01	3.53	Sep95	www.ibm
IBM 43P	MPC604	100	512+16/16	3.59	3.20	Sep96	www.ibm
IBM 43P	MPC604	120	512+16/16	4.24	3.41	Sep96	www.ibm
IBM 43P	MPC604	133	512+16/16	4.72	3.76	Sep96	www.ibm
IBM 43P/140	MPC604e	166	512+32/32	6.15	4.83	Oct96	www.ibm
IBM 43P/140	MPC604e	200	1M+32/32	7.22	6.91	Oct96	www.ibm
IBM 43P/140u	MPC604e	233	1M+32/32	8.66	5.63	Apr97	www.ibm
IBM 43P/140n	MPC604e	233	1M+32/32	9.24	5.75	Apr97	www.ibm
IBM 43P/140	MPC604e	333	1M+32/32	12.9	6.21	Oct97	www.ibm
IBM 43P/150	MPC604e	375	1M+32/32	15.1	10.1	Oct98	www.ibm
IBM 43P/240	MPC604e	233	512+32/32	5.73	4.60	Oct96	www.ibm
IBM 43P/240	2xMPC604e	233	1M+32/32	8.71	5.87	Apr97	www.ibm
IBM 43P/260	POWER3	200	4M+32/64	13.2	30.1	Oct98	www.ibm
IBM 44P/170	MPC630+	333	1M+32/64	19.8	35.6	Jul00	www.ibm
IBM 44P/170	MPC630+	400	4M+32/64	25.3	47.9	Jul00	www.ibm
IBM 44P/270	MPC630+	375	4M+32/64	24.3	48.2	Jul00	www.ibm
IBM 59H/R20	POWER2	66	1M+32/128	3.37	9.80	Sep96	www.ibm
IBM [FH]50	MPC604e	332	256+32/32	14.4	12.6	Jun98	www.ibm
IBM H70	RS64-2	340	4M+64/64	16.0	21.2	Apr99	www.ibm
IBM [FH]80	RS64-3	450	2M+128/128	21.0	25.4	Jul00	www.ibm
IBM M80	RS64-3	500	4M+128/128	24.1	29.1	Jul00	www.ibm
IBM R24	POWER2	71	2M+32/128	3.47	10.2	Sep96	www.ibm
IBM SP2/66Thin	POWER2	67	2M+32/128	3.31	9.35	Nov96	www.ibm
IBM SP2/77Wide	POWER2	77	32/256	3.84	12.4	Nov96	www.ibm
IBM SP2/120Thin	POWER2SC	120	32/128	5.61	16.6	Nov96	www.ibm
IBM SP2/160Thin	POWER2SC	160	32/128	8.61	25.8	Oct97	www.ibm
Intel XXpress	Pentium	66/100	1M+8/8	3.30	2.59	Jan96	www.intel
Intel XXpress	Pentium	60/120	1M+8/8	3.72	2.81	Nov95	www.intel
Intel XXpress	Pentium	66/133	1M+8/8	4.14	3.12	Nov95	www.intel
Intel XXpress	Pentium	60/150	1M+8/8	4.27	3.04	Jan96	www.intel
Intel XXpress	Pentium	66/166	1M+8/8	4.76	3.37	Jan96	www.intel
Intel 82430VX	Pentium	66/133	512+8/8	4.00	3.44	Apr97	www.intel
Intel 82430VX	Pentium	60/150	512+8/8	4.10	3.42	Apr97	www.intel
Intel 82430VX	Pentium	66/166	512+8/8	4.56	3.84	Apr97	www.intel
Intel 82430VX	Pentium	66/200	512+8/8	5.10	4.18	Apr97	www.intel
Intel 82430VX	PentiumMMX	66/166	512+16/16	5.59	4.30	Apr97	www.intel
Intel 82430VX	PentiumMMX	66/200	512+16/16	6.41	4.66	Apr97	www.intel
Intel LT430TX	Pentium	66/133	512+8/8	4.01	3.50	Jul97	www.specb
Intel LT430TX	Pentium	60/150	512+8/8	4.13	3.53	Jul97	www.specb
Intel LT430TX	Pentium	66/166	512+8/8	4.58	3.92	Jul97	www.specb
Intel LT430TX	PentiumMMX	66/166	512+16/16	5.60	?	Jul97	www.specb
Intel LT430TX	Pentium	66/200	512+8/8	5.17	4.32	Jul97	www.specb
Intel LT430TX	PentiumMMX	66/200	512+16/16	6.44	4.87	Jul97	www.specb
Intel LT430TX	PentiumMMX	66/233	512+16/16	7.12	5.21	Jul97	www.specb
Intel Alder	PentPro	150	256+8/8	6.08	5.42	Jan96	www.intel
Intel Alder	PentPro	166	512+8/8	7.11	6.21	Jan96	www.intel

Intel Alder	PentPro	180	256+8/8	7.29	6.08	Jan96	www.intel
Intel Alder	PentPro	200	256+8/8	8.09	6.75	Jan96	www.intel
Intel Aurora	PentPro	150	256+8/8	?	4.71	Jan96	www.intel
Intel Aurora	PentPro	166	256+8/8	?	5.20	Jan96	www.intel
Intel PD440FX	PentiumII	66/233	512+16/16	9.49	6.43	May97	www.intel
Intel PD440FX	PentiumII	66/266	512+16/16	10.8	6.89	May97	www.intel
Intel SE440BX-2	PentiumII	100/300	512+16/16	12.9	9.20	Mar98	www.intel
Intel SE440BX-2	PentiumII	100/333	512+16/16	14.0	10.0	Mar98	www.intel
Intel SE440BX-2	PentiumII	100/350	512+16/16	14.9	11.4	Mar98	www.intel
Intel SE440BX-2	PentiumII	100/400	512+16/16	16.9	12.8	Mar98	www.intel
Intel SE440BX-2	PentiumII	100/450	512+16/16	18.5	13.3	Mar98	www.intel
Intel SE440BX-2	PentiumIII	100/450	512+16/16	18.7	13.7	Mar98	www.intel
Intel SE440BX-2	PentiumIII	100/500	512+16/16	20.6	14.7	Mar98	www.intel
Intel SE440BX2pre	PentiumIII	100/650	256+16/16	31.6	22.9	Oct99	www.intel
Intel SE440BX2pre	PentiumIII	100/700	256+16/16	33.8	23.5	Oct99	www.intel
Intel AL440LX	Celeron	66/300	16/16	8.81	6.97	Mar99	www.specb
Intel AL440LX	Celeron	66/300	128+16/16	11.9	9.21	Mar99	www.specb
Intel AL440LX	Celeron	66/333	128+16/16	12.9	9.65	Mar99	www.specb
Intel AL440LX	Celeron	66/366	128+16/16	13.9	10.1	Mar99	www.specb
Intel AL440LX	Celeron	66/400	128+16/16	14.9	10.6	Mar99	www.specb
Intel AL440LX	Celeron	66/433	128+16/16	15.8	10.9	Mar99	www.specb
Intel 0R840pre	PentiumIII	133/667	256+16/16	33.0	29.0	Oct99	www.intel
Intel 0R840pre	PentiumIII	133/733	256+16/16	35.6	30.4	Oct99	www.intel
RDI PowerLite170	TurboSP	85/170	512+16/16	3.08	2.74	Jan97	www.rdi
Ross 200S-100	HyperSP	50/100	256+8/0	2.65	3.39	Apr95	www.ross
Ross 200S-200/512	HyperSP	50/200	512+8/0	5.30	5.05	May97	www.ross
Ross HS20	HyperSP	50/125	256+8/0	3.16	4.35	Dec96	www.ross
Ross HS20	HyperSP	50/150	512+8/0	4.10	4.98	Dec96	www.ross
Ross HS30	HyperSP	66/142	1M+8/0	3.97	5.06	Dec96	www.ross
SGI Indy-R5000	R5000	??/150	32/32	3.07	4.20	Jul96	www.specb
SGI Indy-R5000	R5000	??/150	512+32/32	3.82	4.78	Jul96	www.specb
SGI Indy-R5000	R5000	??/180	512+32/32	4.32	4.78	Jul96	www.specb
SGI Indigo2-R10k	R10000	175	1M+32/32	8.0	10.3	Oct96	www.sgi
SGI Indigo2-R10k	R10000	195	1M+32/32	8.88	10.6	Oct96	www.specb
SGI 02-R5kPC	R5000	180	32/32	3.70	4.55	Oct96	www.specb
SGI 02-R5kSC	R5000	180	512+32/32	4.82	5.42	Oct96	www.specb
SGI 02-R10kSC	R10000	175	1M+32/32	7.62	6.60	Dec96	www.sgi
SGI PChall-R10k	R10000	195	1M+32/32	8.75	12.4	Jul96	www.specb
SGI PChall-R10k	R10000	195	2M+32/32	8.85	13.8	Jul96	www.specb
SGI Origin200	R10000	180	1M+32/32	8.59	15.6	Nov96	www.specb
SGI Origin200	R10000	225	2M+32/32	13.0	20.4	Oct98	www.sgi
SGI Origin2000	R10000	195	4M+32/32	9.48	19.0	Nov96	www.specb
SGI Octane	R10000	175	1M+32/32	8.4	15.5	Feb97	www.sgi
SGI Octane	2xR10000	175	1M+32/32	8.5	15.5	Feb97	www.sgi
SGI Octane	R10000	195	1M+32/32	9.3	17.0	Feb97	www.sgi
SGI Octane	2xR10000	195	1M+32/32	9.4	17.4	Feb97	www.sgi
SGI Octane	R10000	225	1M+32/32	12.2	18.0	May98	www.sgi
SGI Octane	2xR10000	225	1M+32/32	12.2	23.8	May98	www.sgi
SGI Octane	R10000	250	1M+32/32	13.6	20.3	Jan98	www.sgi
SGI Octane	2xR10000	250	1M+32/32	13.6	26.6	May98	www.sgi

SGI Octane	R12000	300	2M+32/32	17.3	27.4	Apr99	www.sgi
SGI Octane	2xR12000	300	2M+32/32	?	34.3	Apr99	www.sgi
SNI/Pyr Cel1000	PentiumII	??/300	512+16/16	11.9	8.56	Sep97	SNI/Pyr
SNI/Pyr RM200-225	R4600	133	16/16	2.41	?	Sep95	c.bmarks
SNI/Pyr RM200-C20	R4600	133	16/16	2.64	?	Dec95	c.bmarks
SNI/Pyr RM300-C20	R4600	133	16/16	2.64	?	Dec95	c.bmarks
SNI/Pyr RM300-C40	R5000	90/180	512+32/32	4.75	?	Aug96	SNI/Pyr
SNI/Pyr RM300-C50	R5000	??/200	2M+32/32	5.78	?	Feb97	SNI/Pyr
SNI/Pyr RM300-C60	R4400	100/200	1M+16/16	3.55	?	Dec95	c.bmarks
SNI/Pyr RM400-630	R4400	100/200	4M+16/16	3.95	?	Sep95	c.bmarks
SNI/Pyr RM400-C60	R4400	100/200	1M+16/16	3.49	?	Dec95	c.bmarks
SNI/Pyr RM400-C70	R4400	100/200	4M+16/16	3.92	?	Dec95	c.bmarks
SNI/Pyr RM600-E60	R10000	250	8M+32/32	14.7	?	Nov97	SNI/Pyr
SNI/Pyr RM1000	R4400	120/240	4M+16/16	5.04	?	Jul96	SNI/Pyr
Sun SS10/40	SuprSP	40	20/16	1.13	1.38	Mar96	c.bmarks
Sun SS[45]/110	MicroSP2	110	16/8	1.59	1.99	Mar96	c.bmarks
Sun SS5/170	TurboSP	85/170	512+16/16	3.53	3.00	Apr97	www.specb
Sun SS20/71	SuprSP2	50/75	1M+20/16	3.11	3.10	Mar96	c.bmarks
Sun SS20/151	HyperSP	50/150	512+8/0	4.02	4.73	Mar96	c.bmarks
Sun Ultra1/140	UltSP	71/143	512+16/16	4.66	7.90	Mar96	c.bmarks
Sun Ultra1/170	UltSP	83/167	512+16/16	6.26	9.06	Apr97	Sun intro
Sun Ultra1/200E	UltSP	100/200	512+16/16	7.44	10.40	Feb97	Sun intro
Sun Ultra2/1170	UltSP	83/167	512+16/16	6.20	9.27	Apr96	Sun intro
Sun Ultra2/2170	2xUltSP	83/167	512+16/16	6.39	11.8	Apr96	Sun intro
Sun Ultra2/1200	UltSP	100/200	1M+16/16	7.67	11.1	Apr96	Sun intro
Sun Ultra2/2200	2xUltSP	100/200	1M+16/16	7.88	14.7	Apr96	Sun intro
Sun Ultra2/1300	UltSP2	100/300	2M+16/16	12.1	15.5	Apr97	Sun intro
Sun Ultra2/2300	2xUltSP2	100/300	2M+16/16	12.3	20.2	Apr97	Sun intro
Sun Ultra2/1400	UltSP2	100/400	2M+16/16	17.2	22.3	May99	www.sun
Sun Ultra2/2400	2xUltSP2	100/400	2M+16/16	17.2	25.9	May99	www.sun
Sun Ultra5/270	UltSP2i	90/270	256+16/16	9.1	10.6	Nov98	www.sun
Sun Ultra5/333	UltSP2i	111/333	2M+16/16	14.1	18.3	Nov98	www.sun
Sun Ultra5/360	UltSP2i	90/360	256+16/16	12.1	13.1	Nov98	www.sun
Sun Ultra10/300	UltSP2i	100/300	512+16/16	12.1	12.9	Jan98	www.sun
Sun Ultra10/333	UltSP2i	111/333	2M+16/16	14.1	18.3	Nov98	www.sun
Sun Ultra10/360	UltSP2i	120/360	2M+16/16	15.2	19.9	Nov98	www.sun
Sun Ultra10/440	UltSP2i	110/440	2M+16/16	17.9	22.7	May99	www.sun
Sun Ultra30/300	UltSP2	100/300	2M+16/16	12.1	18.3	Jan98	www.sun
Sun Ultra30/250	UltSP2	83/250	1M+16/16	10.0	14.9	Jul97	Sun intro
Sun Ultra30/300	UltSP2	100/300	2M+16/16	12.1	18.3	Jul97	Sun intro
Sun Ultra60/1300	UltSP2	100/300	2M+16/16	13.0	18.3	Jan98	www.sun
Sun Ultra60/2300	2xUltSP2	100/300	2M+16/16	13.0	23.5	Jan98	www.sun
Sun Ultra60/1360	UltSP2	120/360	4M+16/16	16.1	23.5	Jun98	www.sun
Sun Ultra60/2360	2xUltSP2	120/360	4M+16/16	16.1	29.5	Jun98	www.sun
Sun Ultra60/1450	UltSP2	113/450	4M+16/16	19.7	27.0	Jun98	www.sun
Sun Ultra60/2450	2xUltSP2	113/450	4M+16/16	19.7	32.7	Jun98	www.sun
Sun Ultra80/1450	UltSP2	113/450	4M+16/16	19.7	27.9	Nov99	www.sun
Sun Ultra80/2450	2xUltSP2	113/450	4M+16/16	19.7	36.1	Nov99	www.sun
Sun Ultra80/4450	4xUltSP2	113/450	4M+16/16	19.7	44.6	Nov99	www.sun
Sun Ultra250/300	UltSP2	100/300	2M+16/16	12.8	17.3	Sep98	www.specb

Sun Ultra250/300	2xUltSP2	100/300	2M+16/16	?	20.6	Sep98	www.specb
Sun Ultra250/400	UltSP2	100/400	2M+16/16	16.8	21.9	Feb99	www.specb
Sun Ultra250/400	2xUltSP2	100/400	2M+16/16	?	26.4	Feb99	www.specb
Sun Ultra450/300	UltSP2	100/300	2M+16/16	12.1	15.5	Aug97	Sun intro
Sun Ultra450/400	UltSP2	100/400	4M+16/16	17.4	25.7	Nov98	www.specb
Sun Ultra450/400	2xUltSP2	100/400	4M+16/16	?	32.9	Nov98	www.specb
Sun Ultra450/400	4xUltSP2	100/400	4M+16/16	?	40.8	Nov98	www.specb
Sun UltraAXi	UltSP2i	111/333	2M+16/16	14.3	17.0	Jun98	www.specb
Sun UltraX000	UltSP	83/167	512+16/16	6.25	8.73	Sep96	Sun
Sun UltraX000	UltSP	83/167	1M+16/16	6.60	9.37	Sep96	Sun
Sun UltraX000	UltSP2	83/250	1M+16/16	9.74	11.7	Jan97	Sun
Sun UltraX000	UltSP2	83/250	4M+16/16	10.4	15.0	Apr97	Sun
Sun UltraX000	6xUltSP	83/167	512+16/16	?	19.3	Apr96	www.sun
Sun UltraX000	12xUltSP	83/167	512+16/16	?	22.6	Apr96	www.sun

SPECint92, SPECfp92

Source: Table 7, John DiMarco (2000)

System Name	CPU (NUMx)Type	ClkMHz ext/in	Cache Ext+I/D	SPECint 92	SPECfp 92	Info Date	Source Obtained
DEC VAX11/780	VAX	5	8	1.0	1.0	Jan89	SPEC Ref
ALR PowerVEISA	80487SX	20	64+8	10.7	4.9	Mar93	SPEC news
CDC 4330	R3000	33	32/32	24.9	23.9	Sep92	SPEC news
CDC 4360	R3000	33	64/64	24.9	26.7	Sep92	SPEC news
CDC 4680	R6000	66	512+64/16	40.6	45.1	Sep92	SPEC news
Compaq Deskpro	80487SX	16	0+8	9.3	4.3	Mar93	SPEC news
Compaq Deskpro	80487SX	25	64+8	14.2	6.7	Mar93	SPEC news
Compaq Deskpro	80486DX	33	128+8	18.2	8.3	Sep92	SPEC news
Compaq Deskpro	80486DX2	25/50	256+8	25.7	12.2	Mar93	SPEC news
Compaq Deskpro	80486DX2	33/66	256+8	32.2	16.0	Mar93	SPEC news
Compaq DeskproXL	Pentium	66	256+8/8	65.1	63.6	Sep93	SPEC news
Mobius P5-60	Pentium	60	?	50.0	46.7	Jan94	c.sun.hw
Nekotech MachI	A21066	??/166	1M+16	70	105	Jun94	m.sale.wk
Nekotech MachI	A21066	??/200	1M+16	105	135	Jun94	m.sale.wk
Nekotech MachII	A21066	??/210	2M+16	130	184	Jun94	m.sale.wk
Nekotech MachII	A21066	??/225	2M+16	135	205	Jun94	m.sale.wk
Nekotech MachII	A21066	??/275	2M+16	170	240	Jun94	m.sale.wk
DEC VAX3100/38	?	?	?	3.5	3.8	Mar93	DECinfo
DEC VAX3100/76	REX520	?	128	7.1	6.6	Mar93	DECinfo
DEC VAX4000VLC	SOC	?	25	5.8	6.3	Mar93	DECinfo
DEC VAX4000/60	KA46	22.2	?	11.1	12.6	Mar93	DECinfo
DEC VAX4000/90	NVAX	71	2/8	?	30.2	Sep92	SPEC news
DEC VAX6000/410	KA660	36	128	?	7.1	Feb90	uproc rpt
DEC VAX6000/510	KA650	62	512	?	13.3	Sep92	SPEC news
DEC VAX6000/610	KA680	83	2M	?	39.2	Sep92	SPEC news
DEC 5000/900	R3000	40	64/64	27.3	29.9	Sep92	SPEC news
DEC 5000/20	R3000	20	64/64	13.5	18.4	Jun93	DECinfo

DEC 5000/25	R3000	25	64/64	15.7	21.7	Jun93	DECinfo
DEC 5000/33	R3000	33	64/128	20.9	23.4	Sep92	SPEC news
DEC 5000/50,150	R4000	50/100	1M+8/8	46.7	45.9	Sep93	c.arch
DEC 5000/120	R3000	20	64/64	13.8	18.4	Jun93	DECinfo
DEC 5000/125	R3000	25	64/64	16.1	21.7	Jun93	DECinfo
DEC 5000/133	R3000	33	64/128	20.9	29.1	Jun93	DECinfo
DEC 5000/200	R3000	25	64/64	19.5	26.7	Jun93	DECinfo
DEC 5000/240	R3000	40	64/64	27.9	35.8	Jun93	DECinfo
DEC 5000/260	R4400	60/120	1M+16/16	57.1	54.5	Sep93	c.arch
DEC 5000/280	R4400	60/120	1M+16/16	56.9	55.6	Jun93	DECinfo
DEC 2000/300	A21064	30/150	512+8/8	80.9	110.2	Oct93	c.arch
DEC 3000/300	A21064	30/150	256+8/8	66.2	91.5	Apr93	c.sun.mc
DEC 3000/300L	A21064	20/100	256+8/8	45.9	63.6	Apr93	c.sun.mc
DEC 3000/300LX	A21064	25/125	256+8/8	63.5	75.5	May94	SPEC news
DEC 3000/300X	A21064	35/175	256+8/8	84.4	100.5	May94	SPEC news
DEC 3000/400	A21064	27/133	512+8/8	74.7	112.2	Apr93	c.arch
DEC 3000/500	A21064	30/150	512+8/8	84.4	127.7	Apr93	c.arch
DEC 3000/500X	A21064	40/200	512+8/8	110.9	164.1	Apr93	c.sun.mc
DEC 3000/600S	A21064	35/175	2M+8/8	114.1	162.1	Oct93	c.arch
DEC 3000/700	A21064A	38/225	2M+16/16	162.6	230.6	Jul94	Digital
DEC 3000/800S	A21064	40/200	2M+8/8	138.4	187.6	May94	c.sun.hw
DEC 3000/900	A21064A	39/275	2M+16/16	189.3	264.1	Jul94	Digital
DEC 4000/610	A21064	40/160	1M+8/8	94.6	137.6	Oct93	Digital
DEC 4000/710	A21064	38/190	4M+8/8	122.3	185.4	Oct93	c.arch
DEC 7000/610	A21064	50/200	4M+8/8	132.6	200.1	Oct93	c.arch
DEC 7000/710	A21064A	39/275	4M+16/16	193.8	292.6	Aug94	Digital
DEC 10000/610	A21064	50/200	4M+8/8	116.5	193.6	Oct93	Digital
DEC 200/4/100	A21064	??/100	512+8/8	74.6	95.2	Feb95	Digital
DEC 250/4/266	A21064A	??/266	2M+16/16	198.6	262.5	Apr95	www.dec
DEC 255/233	A21064A	??/233	1M+16/16	180.0	210.0	Mar96	Digital
DEC 255/300	A21064A	??/300	1M+16/16	215.0	245.0	Mar96	Digital
DEC 500/266	A21164	43/266	2M+96+8/8	329.0	405.0	Mar96	Digital
DEC 500/333	A21164	46/333	2M+96+8/8	389.6	480.1	Mar96	Digital
DEC [24]00/4/166	A21064	33/166	512+8/8	116.2	134.8	Jul95	Digital
DEC [24]00/4/233	A21064A	39/233	512+16/16	157.7	183.9	Apr95	Digital
DEC 600/5/266	A21164	38/266	2M+96+8/8	289.0	405.0	Jul95	Digital
DEC 600/5/266	A21164	38/266	4M+96+8/8	292.8	433.5	Jul95	Digital
DEC 600/5/300	A21164	75/300	4M+96+8/8	337.8	502.1	Jul95	Digital
DEC 600/5/333	A21164	83/333	4M+96+8/8	412.4	545.2	Jan96	Digital
DEC 1000/4/200	A21064	40/200	2M+8/8	135.8	177.0	Nov94	Digital
DEC 1000/4/233	A21064	??/233	2M+8/8	165.3	222.9	May95	Digital
DEC 2[01]00/4/200	A21064	47/190	1M+8/8	131.8	161.0	Nov94	Digital
DEC 2[01]00/4/233	A21064A	38/233	1M+16/16	177.3	215.0	Apr95	Digital
DEC 2[01]00/4/275	A21064A	39/275	4M+16/16	202.9	292.6	Apr95	Digital
DEC 2[01]00/5/250	A21164	35/250	4M+96+8/8	277.1	410.4	Apr95	Digital
DEC 2[01]00/5/300	A21164	42/300	4M+96+8/8	319.3	477.3	Feb96	Digital
DEC 8[24]00/5/300	A21164	75/300	4M+96+8/8	341.4	512.9	Apr95	Digital
DEC 8[24]00/5/350	A21164	88/350	4M+96+8/8	432.8	602.2	Feb96	Digital
DG 4100	88100	20	16/16	13.1	?	Sep92	SPEC news
DG 4300	88100	25	16/16	17.4	?	Sep92	SPEC news

DG 4600	88100	33	16/16	22.6	?	Sep92	SPEC news
DG 4605	88100	33	64/32	26.1	?	Sep92	SPEC news
DG 5225	2x88100	25	128/128	20.3	12.1	May93	c.sun.hw
DG 5500	88100	40	128/128	32.3	41.4	Oct93	
DG 6240	4x88100	25	256/256	20.1	?	Sep92	SPEC news
HP 425t	68040	25	4/4	12.3	10.3	Jun93	DECinfo
HP 425e	68040	25	4/4	12.2	9.3	Jun93	DECinfo
HP 705	PA1.1	35	32/64	21.9	33.0	Nov92	Sunflash
HP 710	PA1.1	50	32/64	31.6	47.6	Oct92	c.arch
HP 712/60	PA7100LC	60	64	67.0	85.3	Jun95	www.hp
HP 712/80i	PA7100LC	80	256	84.1	79.0	Jan94	HP
HP 712/80	PA7100LC	80	256	97.1	123.3	Jun95	www.hp
HP 712/100	PA7100LC	100	256	117.2	144.2	Jun95	www.hp
HP 715/33	PA7100	33	64/64	32.5	52.4	Jan94	HP
HP 715/50	PA7100	50	64/64	49.2	78.8	Jan94	HP
HP 715/75	PA7100	75	256/256	82.6	127.2	Jan94	HP
HP 715/64	PA7100LC	64	256	80.6	109.4	Jun95	www.hp
HP 715/80	PA7100LC	80	256	96.3	123.2	Jun95	www.hp
HP 715/100	PA7100LC	100	256	115.1	138.7	Jun95	www.hp
HP 715/100XC	PA7100LC	100	1M	132.2	184.6	Jun95	www.hp
HP 720	PA1.1	50	128/256	38.5	66.1	Jun93	DECinfo
HP 725	PA7100	50	64/64	37.1	72.8	Apr93	Sunflash
HP 725/75	PA7100	75	256/256	80.3	126.8	May94	HP
HP 730	PA1.1	66	128/256	47.8	75.4	May92	c.sun.hw
HP 7[35]5	PA7100	99	256/256	109.1	167.9	Jan94	HP
HP 7[35]5/125	PA7150	125	256/256	136	201	Apr94	HP
HP 750	PA1.1	66	256/256	48.1	75.0	Oct92	c.arch
HP C100	PA7200	100	256/256	140	224	Dec95	www.hp
HP C110	PA7200	120	256/256	167	269	Dec95	www.hp
HP F10	PA1.1	32	32/64	22.0	36.6	Mar93	SPEC news
HP [F-I]30	PA1.1	48	256/256	37.8	62.4	Mar93	SPEC news
HP [FH]20	PA1.1	48	64/64	33.6	56.1	Mar93	SPEC news
HP [GHI]30	PA1.1	48	256/256	37.8	62.4	Apr94	www.hp
HP [GHI]40	PA1.1	64	256/256	65.2	91.3	Apr94	www.hp
HP [GHI]50	PA7100	96	256/256	100.0	158.5	Apr94	www.hp
HP [GHI]60	PA7100	96	1M/1M	108.8	195.3	Apr94	www.hp
HP E25	PA7100LC	48	64	45.0	66.6	Mar95	www.hp
HP E35	PA7100LC	64	256	65.6	98.5	Mar95	www.hp
HP E45	PA7100LC	80	256	82.1	122.9	Mar95	www.hp
HP E55	PA7100LC	96	1M	108.0	163.4	Mar95	www.hp
HP J200	PA7200	100	256/256	139.4	222.5	Jun95	www.hp
HP J210	PA7200	120	256/256	168.7	269.2	Jun95	www.hp
HP 807	PA1.1	32	64/32	20.2	?	Sep92	SPEC news
HP 827/17	PA1.1	48	64/64	31.4	?	Sep92	SPEC news
HP 847	PA1.1	?	?	34.8	?	Apr93	DECinfo
HP 867	PA1.1	64	256/256	45.6	?	Sep92	SPEC news
HP 877	PA1.1	64	256/256	45.8	?	Sep92	SPEC news
HP 897S	PA7100	96	1M/1M	78.3	141.6	Sep92	SPEC news
IBM N40	MPC601	50	32	41.7	51.0	Mar95	www.ibm
IBM [2M]20	RSC3308	33.3	8	20.4	29.1	Sep93	c.arch

IBM 230	RSC4608	45.5	128+8	28.5	39.9	Sep93	c.arch
IBM 250	MPC601	66	32	62.6	72.2	Jul94	www.ibm
IBM 250	MPC601	80	32	77.6	89.4	Jul94	www.ibm
IBM 25T	MPC601	66	32	62.6	78.8	Mar95	www.ibm
IBM 25T	MPC601	80	32	72.2	90.4	Mar95	www.ibm
IBM B50	MPC603e	375	1M+32/32	15.1	10.1	Jul00	www.ibm
IBM C10	MPC601	80	32	78.8	90.4	Jul94	www.ibm
IBM C10	MPC601	80	1M+32	90.5	100.8	Jul94	www.ibm
IBM C20	MPC604	120	16/16	118.2	116.5	Jun95	www.ibm
IBM C20	MPC604	120	1M+16/16	155.0	150.2	Jun95	www.ibm
IBM E20	MPC604	100	512+16/16	139.6	131.6	Oct95	www.ibm
IBM 320H	POWER	25	8/64	20.9	39.4	Nov92	Sunflash
IBM 340	POWER	33	8/32	27.7	51.9	Oct92	c.arch
IBM 350	POWER	41.6	8/32	35.4	74.2	Nov92	Digital
IBM 355	POWER	41.6	32/32	48.1	83.3	Sep93	c.arch
IBM 365,570	POWER	50	32/32	57.5	99.2	Sep93	c.arch
IBM 37[05T]	POWER	62.5	32/32	70.3	121.1	Sep93	c.arch
IBM 380	POWER2	59	32/64	99.3	187.2	Mar95	www.ibm
IBM 390	POWER2	67	1M+32/64	114.3	205.3	Feb95	www.ibm
IBM 39H	POWER2	67	32/64	122.2	244.6	May95	c.bmarks
IBM 39H	POWER2	67	1M+32/64	129.1	260.7	May95	c.bmarks
IBM 39H	POWER2	67	2M+32/64	130.2	266.6	Mar95	www.ibm
IBM 40P	MPC601	66	32	63.7	67.8	Mar95	www.ibm
IBM 40P	MPC601	66	256+32	75.1	77.0	Mar95	www.ibm
IBM 41[TW]	MPC601	80	512+32	88.1	98.7	Jul94	www.ibm
IBM 41[TW]	MPC601	80	32	78.8	90.4	Jul94	www.ibm
IBM 42[TW]	MPC604	120	16/16	118.2	116.5	Jun95	www.ibm
IBM 42[TW]	MPC604	120	512+16/16	150.2	146.5	Jun95	www.ibm
IBM 43P	MPC604	100	256+16/16	128.1	120.2	Jun95	www.ibm
IBM 43P	MPC604	120	512+16/16	157.9	139.2	Jun95	www.ibm
IBM 43P	MPC604	133	512+16/16	176.4	156.5	Jun95	www.ibm
IBM 520H	POWER	25	8/32	20.9	39.6	May92	c.sun.hw
IBM 530H	POWER	41.6	8/64	28.5	64.6	Mar93	c.sun.hw
IBM 550	POWER	41.6	8/64	35.4	71.7	May92	c.sun.hw
IBM 560	POWER	50	8/64	42.0	85.6	Oct92	c.arch
IBM [59]80	POWER	62.5	32/64	73.3	134.6	Sep93	c.arch
IBM 580H	POWER2	55	32/256	97.6	203.9	Sep93	c.arch
IBM 590	POWER2	66.6	32/256	121.6	259.7	Jul94	c.bmarks
IBM 59H	POWER2	66.6	1M+32/128	122.4	250.7	Mar95	www.ibm
IBM 591/R21	POWER2	77	32/256	143.5	307.9	Jul95	www.ibm
IBM 970B	POWER	50	32/64	58.8	108.9	Sep93	c.arch
IBM 990	POWER2	71.5	32/256	126.0	260.4	Sep93	c.arch
IBM R24	POWER2	71.5	2M+32/128	134.1	273.8	Jul94	c.bmarks
Mips Magnum	R4000	50/100	16	36.8	40.0	Oct92	c.arch
SGI 4D/25	R3000	20	64/32	14.0	11.1	Jun93	DECinfo
SGI 4D/35	R3000	36	64/64	28.0	33.4	Jun93	DECinfo
SGI Challenge	R4400	50/100	1M+16/16	62.4	66.5	Apr93	c.arch
SGI Onyx	R4400	100/200	4M+16/16	142	143.3	Jul95	SGI
SGI Onyx	R4400	??/?/250	4M+16/16	177.5	180.2	Nov95	SGI Ptabl
SGI PowerChl, Onyx	R8000	75	4M+16/16	108.7	310.6	Jun94	c.arch

SGI PowerChl, Onyx	R8000	90	4M+16/16	132.2	396.1	Aug95	SGI Ptabl
SGI Crimson	R4000	50/100	1M+8/8	61.7	63.4	Oct92	c.arch
SGI Crimson	R4400	75/150	1M+16/16	86.0	93.2	Nov94	SGI Ptabl
SGI Indigo	R3000	33	32/32	22.4	24.2	Nov92	Sunflash
SGI Indigo2	R4600	66/133	512+16/16	94.8	72.0	Nov94	SGI Ptabl
SGI Indigo2	R4400	75/150	1M+16/16	90	87	Apr93	c.bmarks
SGI Indigo2	R4400	100/200	2M+16/16	140	131	Jul95	SGI
SGI Indigo2	R4400	??/250	2M+16/16	176	165	Jul95	SGI
SGI PowerIndigo2	R8000	75	2M+16/16	113	269	Oct95	www.sgi
SGI IndigoR4000	R4000	50/100	1M+8/8	57.6	60.3	Mar93	c.sun.hw
SGI IndyPC	R4000	50/100	8/8	34	35	Jul93	SGI anno
SGI IndyPC	R4600	50/100	16/16	62.8	49.9	May94	SGI anno
SGI IndyPC	R4600	44/133	16/16	84.9	61.0	Feb95	SGI anno
SGI IndySC	R4600	44/133	512+16/16	113.5	73.7	Feb95	SGI anno
SGI IndySC	R4400	50/150	1M+16/16	91.7	97.5	Nov94	SGI Ptabl
SGI IndySC	R4000	50/100	1M+8/8	59	61	Jul93	SGI anno
SGI IndySC	R4400	44/175	1M+16/16	122.6	115.5	Feb95	SGI anno
SGI IndySC	R4400	50/200	1M+16/16	140.2	131.0	Jan96	SGI
Sun SS/ELC	FJMB86903	33	64	18.2	17.9	Nov92	Sunflash
Sun SS/IPC	FJMB86902	25	64	13.8	11.1	Nov92	Sunflash
Sun SS/IPX	FJMB86903	40	64	21.8	21.5	Nov92	Sunflash
Sun SS2	RT601	40	64	21.8	22.8	Oct92	c.arch
Sun SS2/PowerUp	WeitekPwUP	40/80	16/8	32.2	31.1	Jun93	c.sun.an
Sun SS10/20	SuprSP	33	20/16	39.8	46.6	Nov92	Sunflash
Sun SS10/30	SuprSP	36	20/16	45.2	54.0	Apr93	Cockcroft
Sun SS10/40	SuprSP	40	20/16	50.2	60.2	Apr93	Sunflash
Sun SS10/41	SuprSP	40/40.3	1M+20/16	53.2	67.8	Apr93	Cockcroft
Sun SS10/51	SuprSP	40/50	1M+20/16	65.2	83.0	Apr93	Sunflash
Sun Classic,LX	MicroSP	50	4/2	26.4	21.0	Nov92	Sunflash
Sun Voyager	MicroSP2	60	16/8	43.2	36.2	Mar94	Sun
Sun SS4/70	MicroSP2	70	16/8	59.6	46.8	Jan95	Sunflash
Sun SS4/85	MicroSP2	85	16/8	65.3	53.1	May95	SunIntro
Sun SS5/70	MicroSP2	70	16/8	57.0	47.3	Mar94	Sunflash
Sun SS5/85	MicroSP2	85	16/8	65.3	53.1	May95	SunIntro
Sun SS5/110	MicroSP2	110	16/8	78.6	65.3	May95	SunIntro
Sun SS5/Turbo160	TurboSP	80/160	512+16/16	132	111	Nov96	FujiMicro
Sun SS20/50	SuprSP	50	20/16	76.9	80.1	May95	SunIntro
Sun SS20/51	SuprSP	40/50	1M+20/16	81.8	89.0	May95	SunIntro
Sun SS20/61	SuprSP	50/60	1M+20/16	98.2	107.2	May95	SunIntro
Sun SS20/71	SuprSP2	50/75	1M+20/16	125.8	121.2	Jan95	SunIntro
Sun SS20/612	2xSuprSP	50/60	1M+20/16	?	127.1	Sep94	SPEC news
Sun SS20/HS11	HyperSP	50/100	256+8/0	104.5	127.6	Nov94	SunIntro
Sun SS20/HS21	HyperSP	50/125	256+8/0	131.2	153.0	May95	SunIntro
Sun SS20/151	HyperSP	50/150	512+8/0	169.4	208.2	Nov95	SunWorld
Sun Ultra1/140	UltSP	71/143	512+16/16	215	303	Nov95	SunIntro
Sun Ultra1/170	UltSP	83/167	512+16/16	252	351	Nov95	SunIntro
Sun Ultra2/2200	2xUltSP	100/200	1M+16/16	332	505	Nov95	SunIntro
Sun SS1000	SuprSP	40/50	1M+20/16	?	79.9	Jan95	Cockcroft
Sun SS1000	2xSuprSP	40/50	1M+20/16	?	92.3	Jan95	Cockcroft
Sun SS1000	4xSuprSP	40/50	1M+20/16	?	112.8	Jan95	Cockcroft

Sun SS1000	8xSuprSP	40/50	1M+20/16	?	123.1	Jan95	Cockcroft
RDI PowerLite170	TurboSP	85/170	512+16/16	143	119	Jan97	www.rdi
Ross 100S-55	HyperSP	40/55	256+8/0	57	74	Aug94	Ross
Ross 100S-66	HyperSP	40/66	256+8/0	67	87	Aug94	Ross
Ross 100S-72	HyperSP	40/72	256+8/0	75	96	Aug94	Ross
Ross 100S-90	HyperSP	40/90	256+8/0	98	116	Aug95	www.ross
Ross 100S-110/1M	HyperSP	40/110	1M+8/0	135	165	Aug95	www.ross
Ross 100S-125	HyperSP	40/125	256+8/0	126	146	Aug95	www.ross
Ross 200S-66	HyperSP	50/66	256+8/0	72	94	Aug94	Ross
Ross 200S-72	HyperSP	50/72	256+8/0	80	105	Aug94	Ross
Ross 200S-90	HyperSP	50/90	256+8/0	103	120	Aug95	www.ross
Ross 200S-100	HyperSP	50/100	256+8/0	111	130	Apr95	www.ross
Ross 200S-110	HyperSP	50/110	256+8/0	122	142	Apr95	Ross
Ross 200S-110/1M	HyperSP	50/110	1M+8/0	137	171	Aug95	www.ross
Ross 200S-125	HyperSP	50/125	256+8/0	133	154	Aug95	www.ross
Ross 200S-125/512	HyperSP	50/125	512+8/0	152	181	Aug95	www.ross
Ross 200S-125/1M	HyperSP	50/125	1M+8/0	155	191	Mar96	www.ross
Ross 200S-133/512	HyperSP	50/133	512+8/0	160	191	Mar96	www.ross
Ross 200S-166/512	HyperSP	50/166	512+8/0	194	226	Mar96	www.ross
Ross HS20	HyperSP	50/125	256+8/0	132	154	Dec96	www.ross
Ross HS20	HyperSP	50/150	512+8/0	178	209	Dec96	www.ross
Ross HS30	HyperSP	66/142	1M+8/0	174	212	Dec96	www.ross
Ross HS30	HyperSP	66/200	512+8/0	219	239	Dec96	www.ross
Solbourne 6/901	SuprSP	33	16+1M+20/16	44.0	52.5	Dec92	SPEC news
HAL 330	SPARC64	100	128/128	181	230	Sep95	www.hal
HAL 350	SPARC64	118	128/128	212	271	Sep95	www.hal
SNI/Pyr PC/E5S	Pentium	30/60	256+8/8	60.6	55.1	Sep93	SPEC news
SNI/Pyr PC/E5S	Pentium	33/66	256+8/8	67.4	61.5	Sep93	SPEC news
SNI/Pyr PC/E5S	Pentium	30/90	256+8/8	86.3	72.7	Jul94	c.bmarks
SNI/Pyr PC/E5S	Pentium	33/100	256+8/8	96.2	81.2	Jul94	c.bmarks
SNI/Pyr PC/D5T	Pentium	30/60	256+8/8	65.9	52.4	Nov94	c.bmarks
SNI/Pyr PC/D5T	Pentium	30/90	256+8/8	86.0	68.3	Nov94	c.bmarks
SNI/Pyr RM200-125	R4600	50/100	16/16	76.3	?	Nov94	c.bmarks
SNI/Pyr RM200-225	R4600	133	16/16	91.7	?	Dec94	SNI/Pyr
SNI/Pyr RM200-C20	R4600	133	16/16	104.6	?	Dec95	c.bmarks
SNI/Pyr RM300-C20	R4600	133	16/16	104.6	?	Dec95	c.bmarks
SNI/Pyr RM300-C60	R4400	100/200	1M+16/16	140.9	?	Dec95	c.bmarks
SNI/Pyr RM400-120	R4400	50/100	16/16	45.6	?	Oct93	c.bmarks
SNI/Pyr RM400-120	R4400	50/100	128+16/16	49.7	?	Jan94	c.bmarks
SNI/Pyr RM400-220	R4400	50/100	512+16/16	68.2	?	Nov94	c.bmarks
SNI/Pyr RM400-340	R4400	50/100	1M+16/16	71.4	?	Nov94	c.bmarks
SNI/Pyr RM400-420	R4400	75/150	512+16/16	92.0	?	Nov94	c.bmarks
SNI/Pyr RM400-440	R4400	75/150	1M+16/16	100.4	?	Nov94	c.bmarks
SNI/Pyr RM400-540	R4400	75/150	4M+16/16	108.7	?	Nov94	c.bmarks
SNI/Pyr RM400-C70	R4400	100/200	4M+16/16	150.7	?	Dec95	c.bmarks
SNI/Pyr RM600-120	R4400	50/100	1M+16/16	55.8	?	Nov93	Siemens
SNI/Pyr RM600-220	R4400	75/150	4M+16/16	94.2	?	Nov93	Siemens
SNI/Pyr RM600-340	R4400	100/200	4M+16/16	143.7	?	Jun95	SNI/Pyr
SNI/Pyr RM600-420	R4400	125/250	4M+16/16	181.3	?	Dec95	SNI/Pyr
SNI/Pyr RM600-720	R4400	125/250	4M+16/16	188.1	?	Jun96	SNI/Pyr

SNI/Pyr RM1000	R4400	100/200	4M+16/16	152.1	?	Aug95	SNI/Pyr
Dell DimensionXPS	Pentium	60/120	512+8/8	160.7	105.4	Nov95	www.intel
Dell DimensionXPS	Pentium	66/133	512+8/8	177.9	116.0	Nov95	www.intel
Micronics M4P	80486DX4	33/100	256+16	51.4	26.6	Mar94	c.arch
Intel 486DX	80486	50	256+8	30.1	14.0	Oct92	c.arch
Intel 486DX2	80486DX2	33/66	0+8	32.4	16.1	Sep92	uproc rpt
Intel Xpress	Pentium	60	256+8/8	70.4	55.1	Mar95	www.intel
Intel Xpress	Pentium	66	256+8/8	78.0	63.6	Mar95	www.intel
Intel Xpress	Pentium	50/75	512+8/8	89.1	68.5	Mar95	www.intel
Intel Xpress	Pentium	60/90	512+8/8	106.5	81.4	Mar95	www.intel
Intel Xpress	Pentium	60/90	1M+8/8	110.1	84.4	Mar95	www.intel
Intel Xpress	Pentium	66/100	512+8/8	118.1	89.9	Mar95	www.intel
Intel Xpress	Pentium	66/100	1M+8/8	121.9	93.2	Mar95	www.intel
Intel Xpress	Pentium	60/120	512+8/8	133.7	99.5	Mar95	www.intel
Intel Xpress	Pentium	60/120	1M+8/8	140.0	103.9	Mar95	www.intel
Intel Xpress	Pentium	66/133	512+8/8	147.5	109.6	Jun95	www.intel
Intel Xpress	Pentium	66/133	1M+8/8	155.5	116.9	Jun95	www.intel
Intel XXpress	Pentium	66/100	1M+8/8	137.7	?	Jan96	www.intel
Intel XXpress	Pentium	60/120	1M+8/8	157.3	108.4	Jan96	www.intel
Intel XXpress	Pentium	66/133	1M+8/8	174.2	120.6	Jan96	www.intel
Intel XXpress	Pentium	60/150	1M+8/8	181.4	?	Jan96	www.intel
Intel XXpress	Pentium	66/166	1M+8/8	197.5	?	Jan96	www.intel
Intel Alder	PentPro	150	256+8/8	243.9	220.0	Jan96	www.intel
Intel Alder	PentPro	166	512+8/8	327.1	261.3	Nov95	www.intel
Intel Alder	PentPro	180	256+8/8	287.1	254.6	Jan96	www.intel
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