Finding and Exploiting CPU Features using MSR Templating

IEEE Symposium on Security and Privacy 2022

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CISPA Helmholtz Center for Information Security

Agenda

- **Motivation**
- **Framework**
  - Detection
  - Classification
  - Extensions
- **Case Studies**

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Motivation

- **Model Specific Registers** (MSRs)
  - 2^{32} 64-bit Registers
  - Documented
  - Undocumented

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- **Influences** on instructions

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- **Influences** on instructions
- **Security** patches

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Motivation

- **Model Specific Registers** (MSRs)
  - 2^{32} 64-bit Registers
  - Documented
  - Undocumented
- **Influences** on instructions
- **Security** patches
- **Hidden** features (e.g., Domas [1])

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The Framework: MSR Scanning

$\underbrace{\qquad\qquad\qquad}_{\textbf{MSR Detection}}$ $\underbrace{\qquad\qquad\qquad\qquad\qquad\qquad}_{\textbf{MSR Classification}}$

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The Framework: MSR Scanning

- **Scan** all MSR addresses
  - `rdmsr` → GP-Fault?
  - `wrmsr` → GP-Fault?

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The Framework: MSR Scanning

- **Scan** all MSR addresses
  - `rdmsr` → GP-Fault?
  - `wrmsr` → GP-Fault?

✓ Complete MSR list

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The Framework: MSR Scanning

- **Scan** all MSR addresses
  - `rdmsr` → GP-Fault?
  - `wrmsr` → GP-Fault?

✓ Complete MSR list

✓ *R*, *W*, *RW* or *not*-present

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The Framework: Documented vs Undocumented

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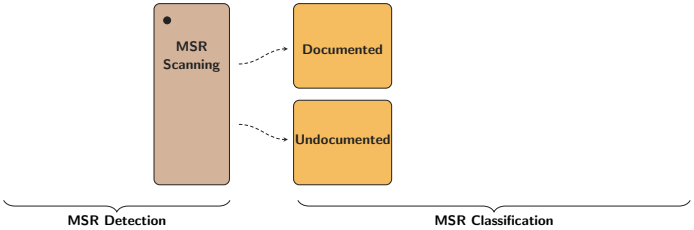
The Framework: Documented vs Undocumented



- **Parse** official PDFs
  - AMD's Reference
  - Intel's SDM

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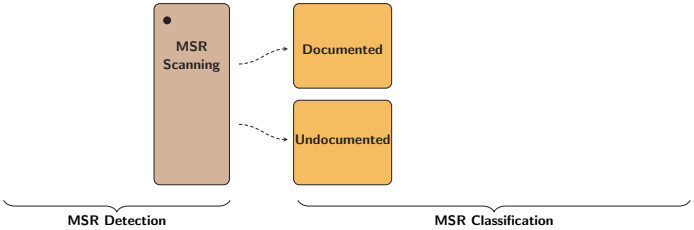
The Framework: Documented vs Undocumented



- **Parse** official PDFs
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- **Extract** table structures
  - Python script

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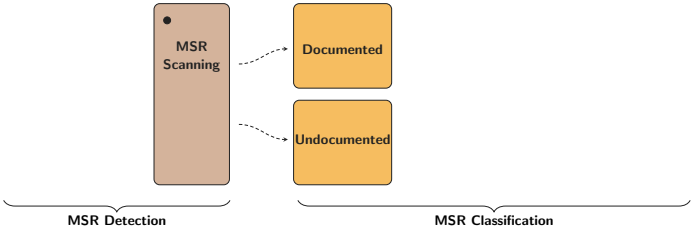
The Framework: Documented vs Undocumented



- **Parse** official PDFs
  - AMD's Reference
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- **Extract** table structures
  - Python script

✓ Documented MSRs

✓ Undocumented MSRs

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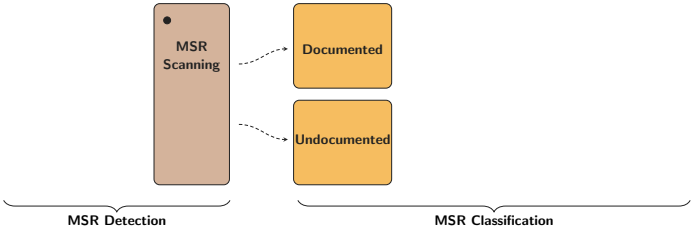
The Framework: Dynamic Analysis



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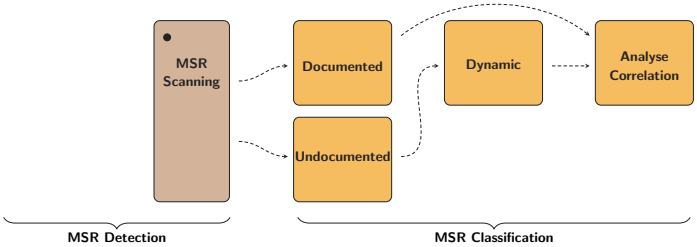
The Framework: Dynamic Analysis



- **Dynamic** MSR:
  - Changing signals

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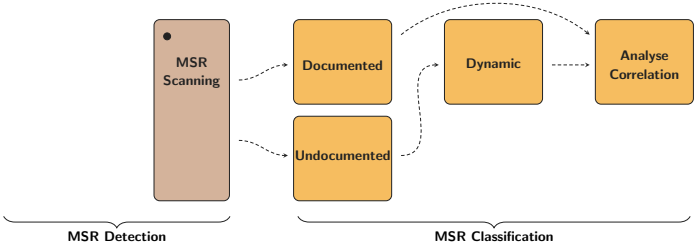
The Framework: Dynamic Analysis



- **Dynamic** MSR:
  - Changing signals
- **Correlation** analysis
  - Similarity
  - Source

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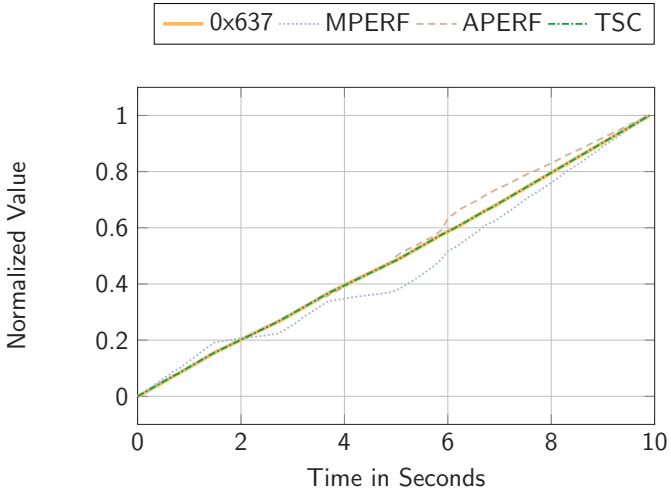
The Framework: Dynamic Analysis



- **Dynamic** MSR:
  - Changing signals
- **Correlation** analysis
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- **Example:** MSR 0x637

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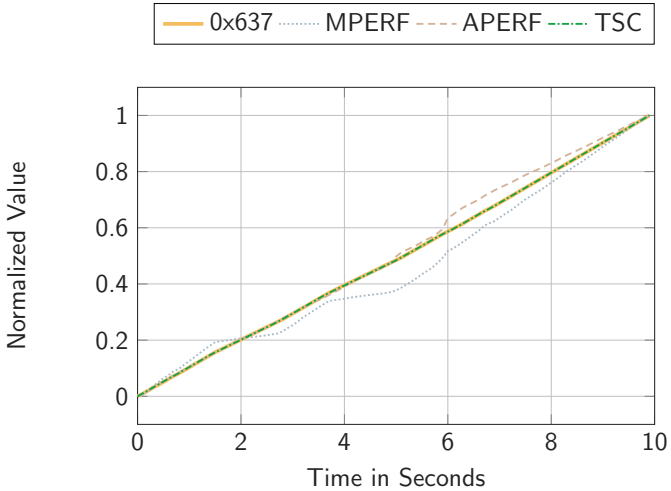
The Framework: Dynamic Analysis



- **Dynamic** MSR:
  - Changing signals
- **Correlation** analysis
  - Similarity
  - Source
- **Example:** MSR 0x637

✓ Similar MSRs

✓ Source hints

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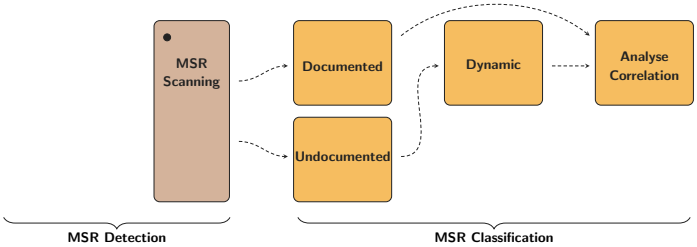
The Framework: Static Analysis



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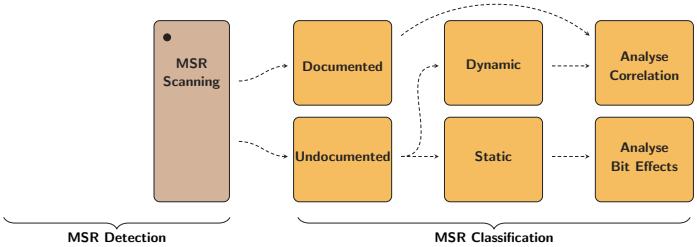
The Framework: Static Analysis



- **Static** MSR:
  - Configuration bits

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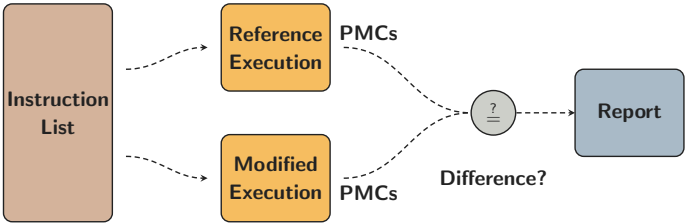
The Framework: Static Analysis



- **Static** MSR:
  - Configuration bits
- **Execute** instruction twice
  - Reference
  - Modified

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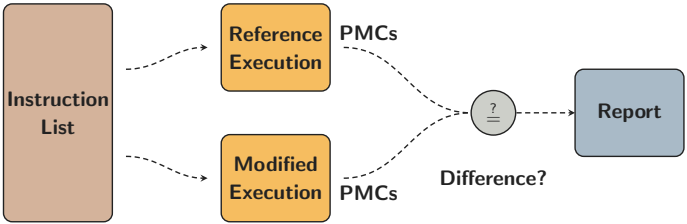
The Framework: Static Analysis



- **Static** MSR:
  - Configuration bits
- **Execute** instruction twice
  - Reference
  - Modified
- **Analyze** PMC differences

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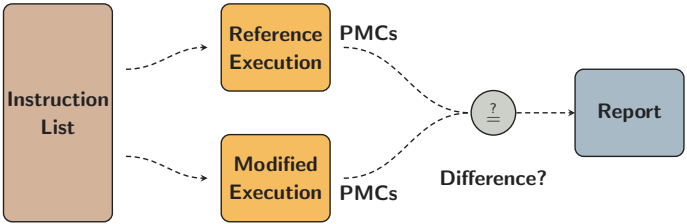
The Framework: Static Analysis



- **Static** MSR:
  - Configuration bits
- **Execute** instruction twice
  - Reference
  - Modified
- **Analyze** PMC differences

✓ Influenced instructions

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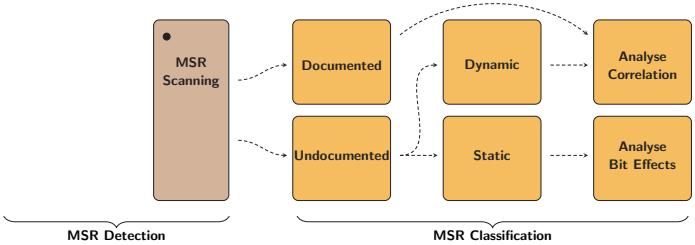
The Framework: BIOS Templating



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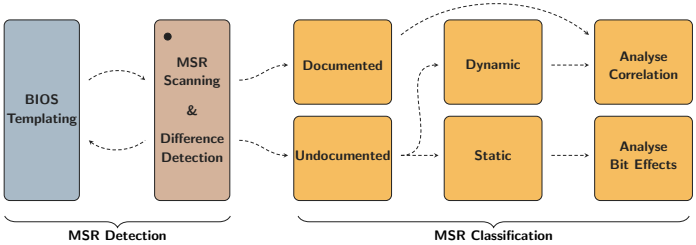

- **Extend** search space

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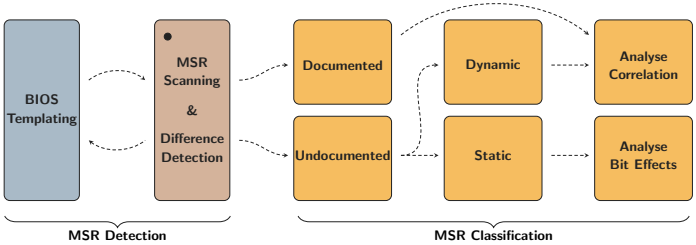

- **Extend** search space
- **Change** BIOS feature

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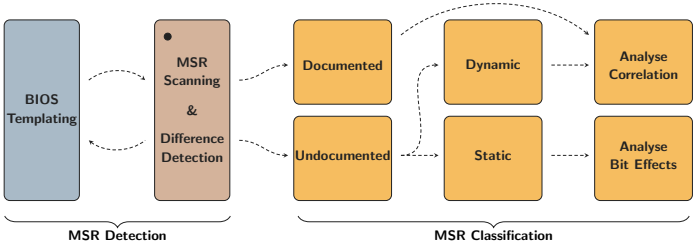

- **Extend** search space
- **Change** BIOS feature
- **Trace** differences

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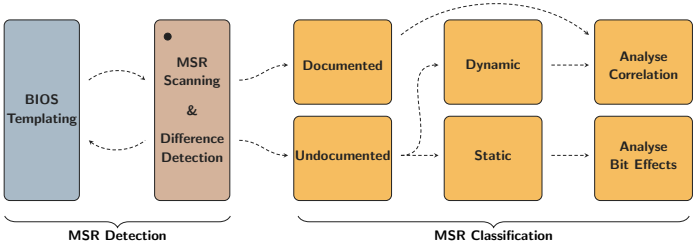

- **Extend** search space
- **Change** BIOS feature
- **Trace** differences
- ✓ Changed MSRs

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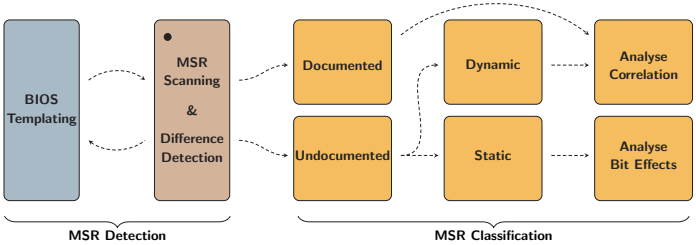
The Framework: Summary



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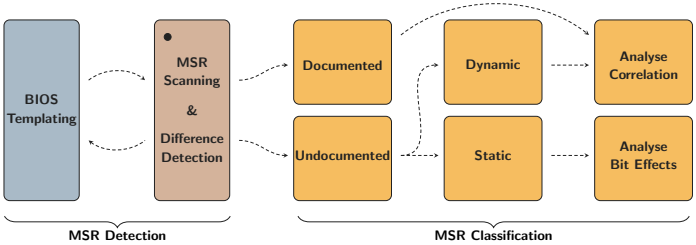

✓ List (R, W, RW, or NP)

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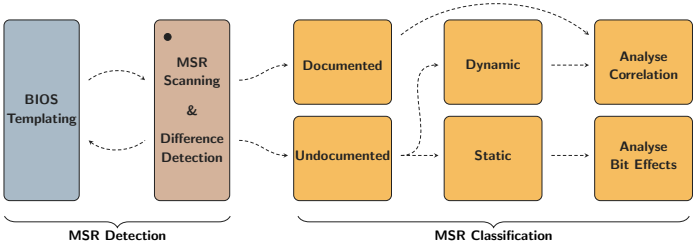
The Framework: Summary



- ✓ List (*R*, *W*, *RW*, or *NP*)
- ✓ Dynamic: similar MSRs

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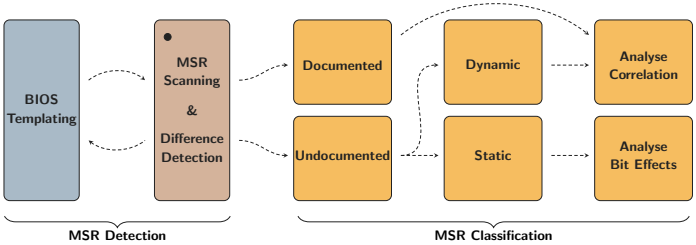
The Framework: Summary



- ✓ List (*R*, *W*, *RW*, or *NP*)
- ✓ Dynamic: similar MSRs
- ✓ Static: influenced instruction

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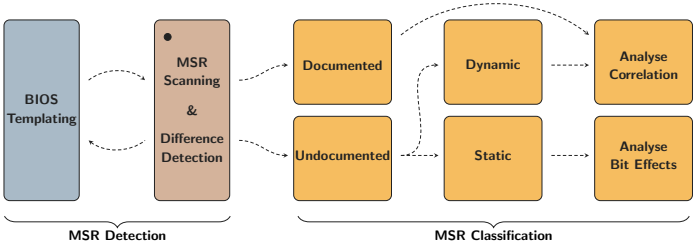
The Framework: Summary



- ✓ List (*R*, *W*, *RW*, or *NP*)
- ✓ Dynamic: similar MSRs
- ✓ Static: influenced instruction
- ✓ BIOS: changed MSRs

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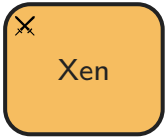
Case Studies



- **Attack** case studies

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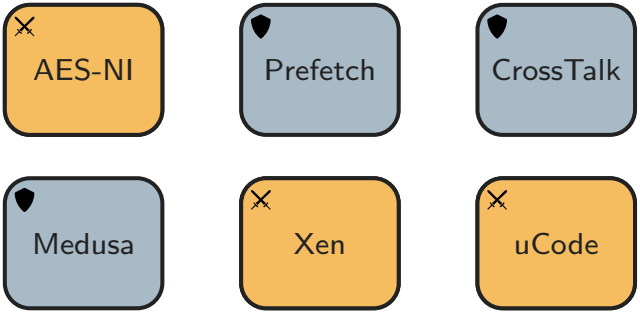
Case Studies



- **Attack** case studies
- **Defense** case studies

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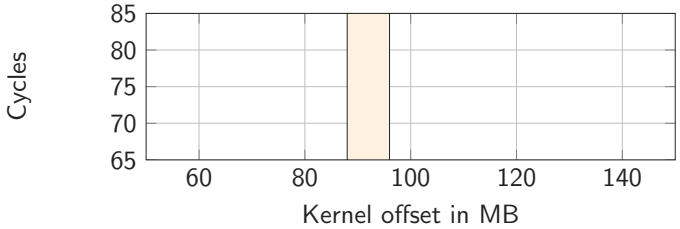
Case Study: Prefetch



- **Prefetch-based** attacks [2]

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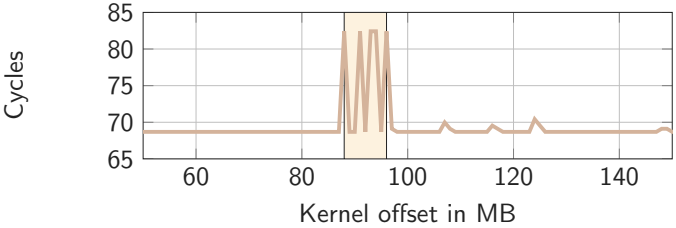
Case Study: Prefetch



- **Prefetch-based** attacks [2]

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Case Study: Prefetch

Instruction	MSR	PMC Effect
`PREFETCHNTA`	Bit 2	-1 LdDispatch
`PREFETCHT0`	Bit 3	-1 LdDispatch
`PREFETCHT1`	Bit 4	-1 LdDispatch
`PREFETCHT2`	Bit 5	-1 LdDispatch
`PREFETCHW`	Bit 6	-1 LdDispatch
`PREFETCH`	Bit 7	-1 LdDispatch

- **Prefetch-based** attacks [2]
- **Search** configuration bits

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Case Study: Prefetch

Instruction	MSR	PMC Effect
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- **Prefetch-based** attacks [2]
- **Search** configuration bits
- **Disable** `prefetch*`

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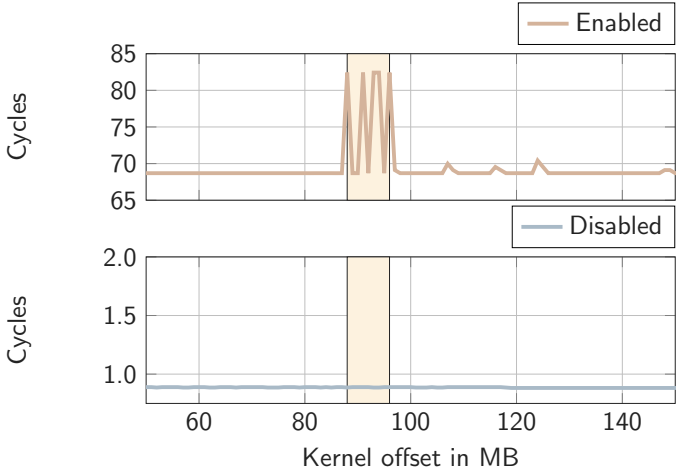
Case Study: Prefetch



- **Prefetch-based** attacks [2]
- **Search** configuration bits
- **Disable** `prefetch*`

✓ **No** prefetch-based attacks

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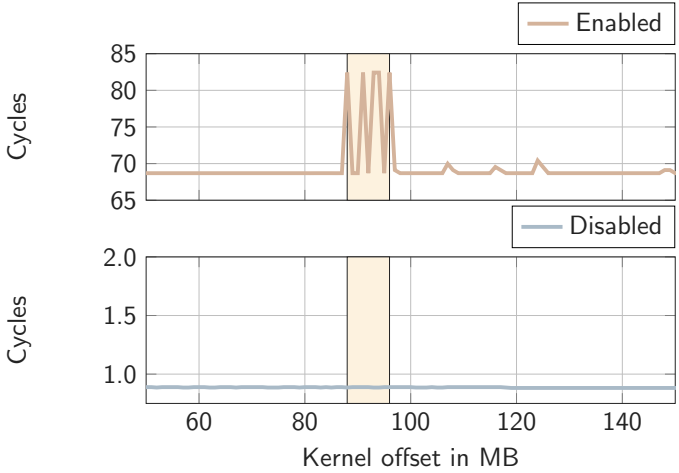
Case Study: Prefetch



- **Prefetch-based** attacks [2]
- **Search** configuration bits
- **Disable** `prefetch*`

✓ **No** prefetch-based attacks

✓ 1% Binaries → 0.04% SPEC

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Case Study: AES-NI

- **Lock** bit

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Case Study: AES-NI

- **Lock** bit
- **Disable** at runtime

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Case Study: AES-NI

```
/* ... */
if( mbedtls_aesni_has_support( MBEDTLS_AESNI_AES ) )
        return( mbedtls_aesni_setkey_enc( ctx->rk, key, keybits ) );
/* ... */
switch( ctx->nr ) {
    case 10:
        for( i = 0; i < 10; i++, RK += 4 ) {
            RK[4]  = RK[0] ^ RCON[i] ^
            ( FSb[ ( RK[3] >>  8 ) & 0xFF ]       ) ^
            ( FSb[ ( RK[3] >> 16 ) & 0xFF ] <<  8 ) ^
            ( FSb[ ( RK[3] >> 24 ) & 0xFF ] << 16 ) ^
            ( FSb[ ( RK[3]       ) & 0xFF ] << 24 );

            RK[5]  = RK[1] ^ RK[4];
            RK[6]  = RK[2] ^ RK[5];
            RK[7]  = RK[3] ^ RK[6];
        }
        break;
    /* additional cases for different key lengths */
}
/* ... */
```

- **Lock** bit
- **Disable** at runtime
- **MbedTLS** in SGX

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Case Study: AES-NI

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```

- **Lock** bit
- **Disable** at runtime
- **MbedTLS** in SGX
  - Check AES-NI

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Case Study: AES-NI

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```

- **Lock** bit
- **Disable** at runtime
- **MbedTLS** in SGX
  - Check AES-NI
  - Fallback T-Tables

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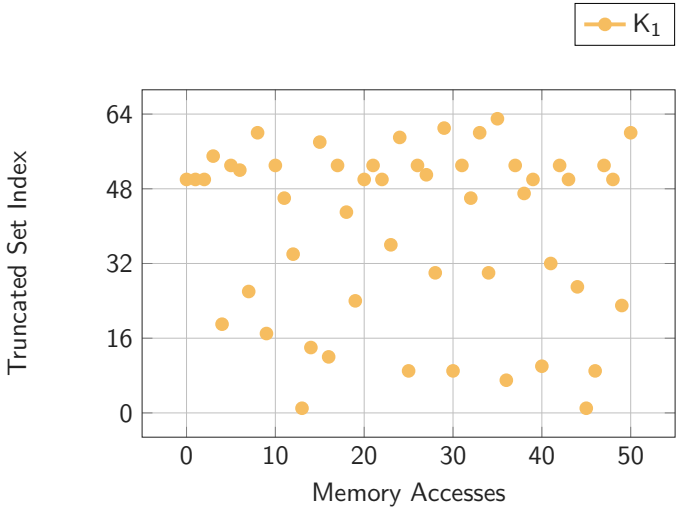
Case Study: AES-NI



- **Lock** bit
- **Disable** at runtime
- **MbedTLS** in SGX
  - Check AES-NI
  - Fallback T-Tables
  - LLC P+P

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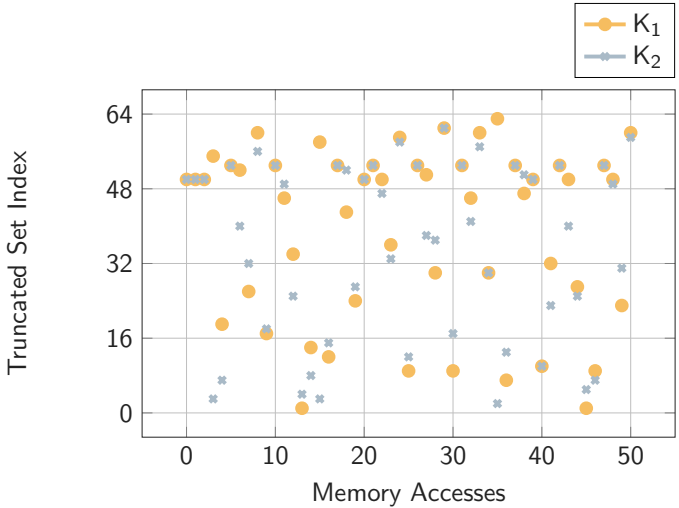
Case Study: AES-NI



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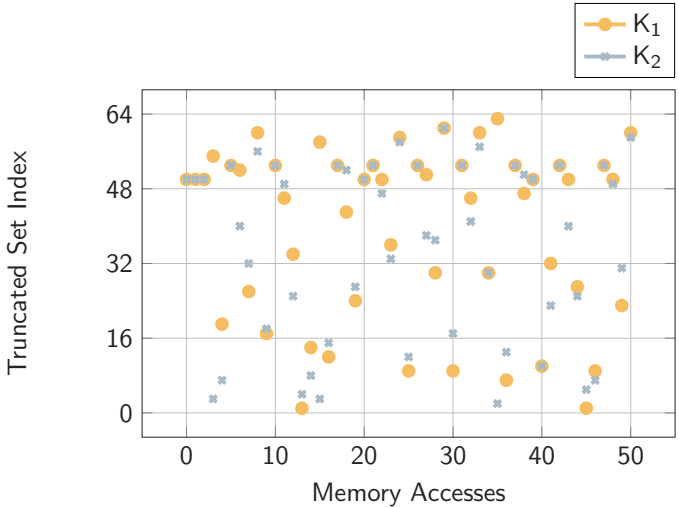
Case Study: AES-NI



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  - Z3 Solver

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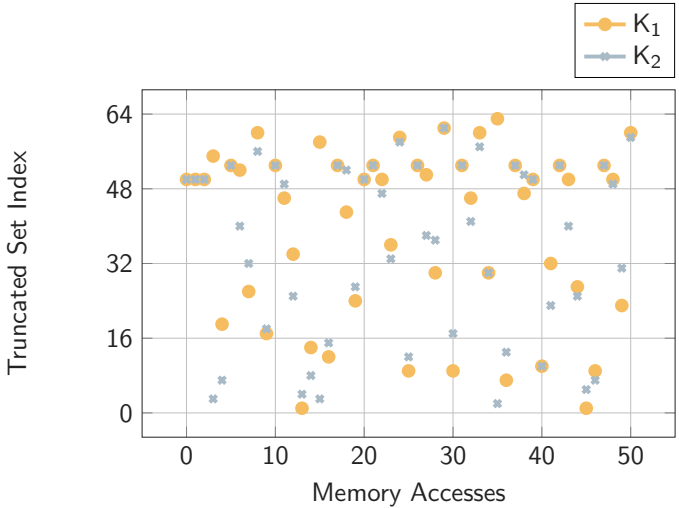
Case Study: AES-NI



- **Lock** bit
- **Disable** at runtime
- **MbedTLS** in SGX
  - Check AES-NI
  - Fallback T-Tables
  - LLC P+P
  - Z3 Solver

✓ Full key

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Case Study: CrossTalk

- **CrossTalk** attack [3]

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Case Study: CrossTalk

- **CrossTalk** attack [3]
- **Unpriviledged** leakage
  - `cpuid` → 88.9%
  - `rdseed` → 0.4%

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Case Study: CrossTalk

- **CrossTalk** attack [3]
- **Unpriviledged** leakage
  - `cpuid` → 88.9%
  - `rdseed` → 0.4%
- **Search** configuration bits

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Case Study: CrossTalk

- **CrossTalk** attack [3]
- **Unpriviledged** leakage
  - `cpuid` → 88.9%
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- **Search** configuration bits
- **CPUID** trap

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Case Study: CrossTalk

- **CrossTalk** attack [3]
- **Unpriviledged** leakage
  - ~~`cpuid` → 88.9%~~
  - `rdseed` → 0.4%
- **Search** configuration bits
- **CPUID** trap

✓ Reduced by **211.4** times

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Case Study: Xen Foreshadow

Hardware:

Xen HV:

Guest:

```
rdmsr
```

- **Hypervisor** handles MSRs

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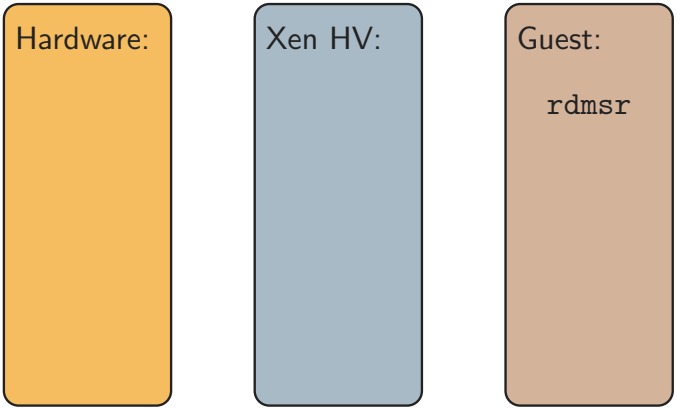
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
- **XEN** deny list

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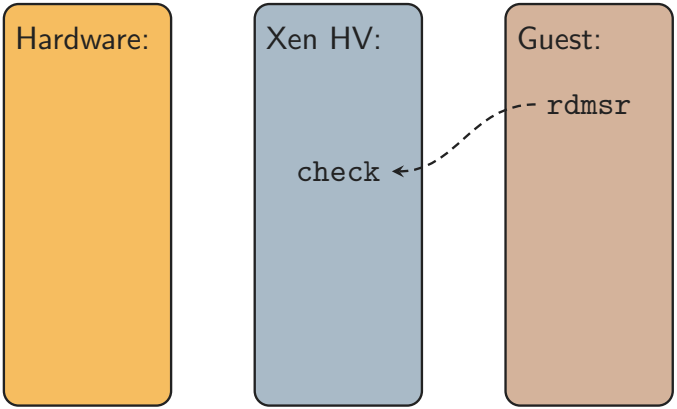
Case Study: Xen Foreshadow



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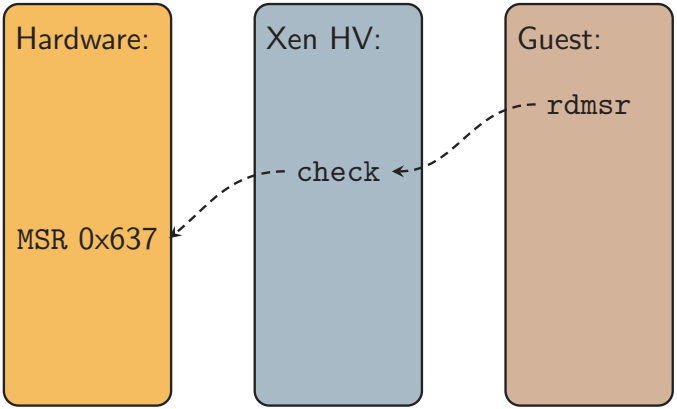
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
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- **Unrestricted** read access

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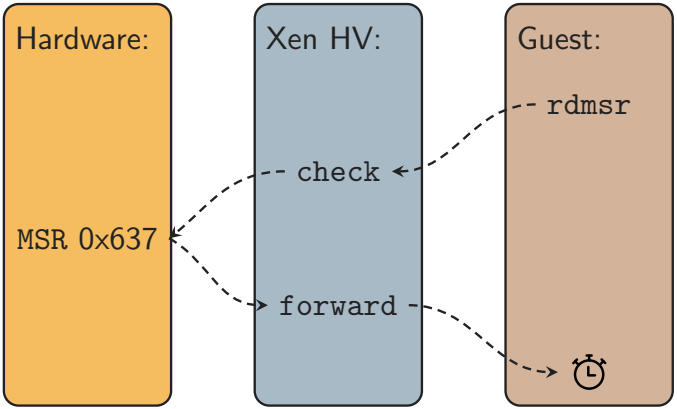
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
- **XEN** deny list
- **Unrestricted** read access
- **Timer** MSR

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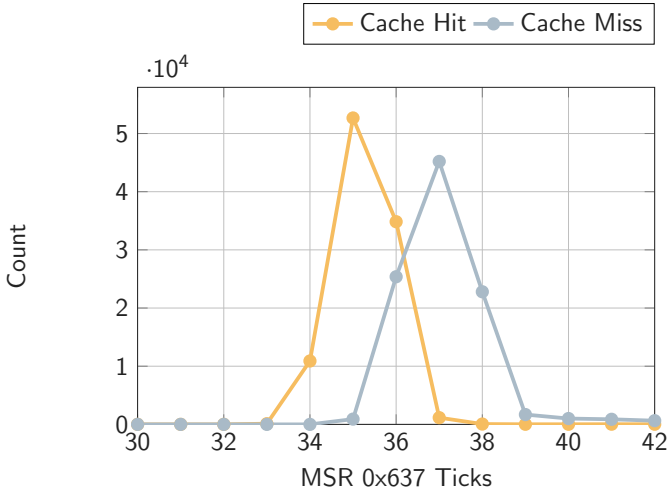
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
- **XEN** deny list
- **Unrestricted** read access
- **Timer** MSR
  - Cache hit vs miss

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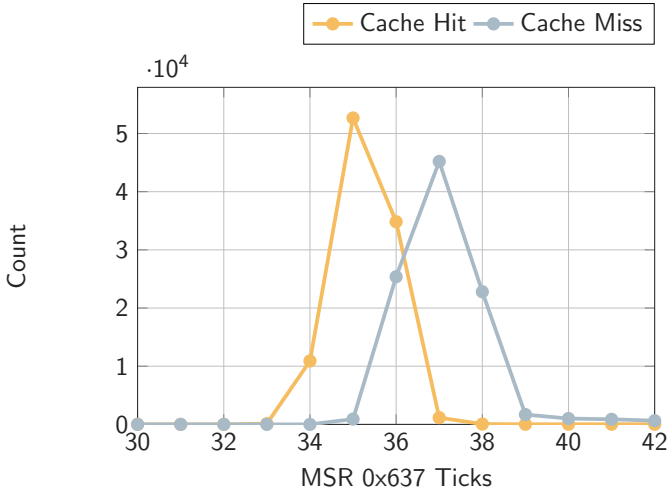
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
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- **Unrestricted** read access
- **Timer** MSR
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  - Foreshadow attack [4]

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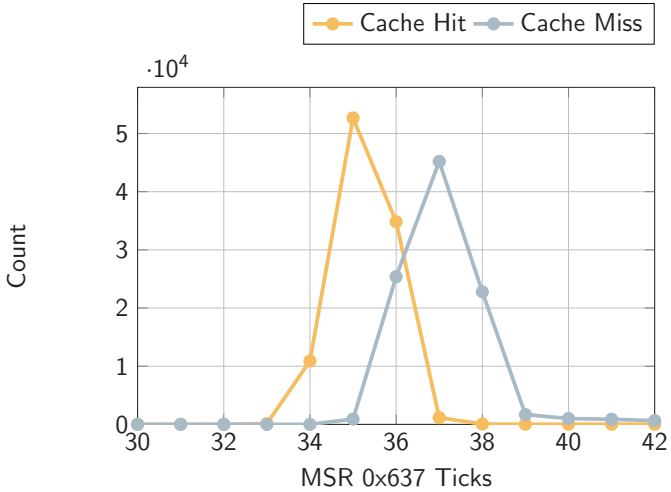
Case Study: Xen Foreshadow



- **Hypervisor** handles MSRs
- **XEN** deny list
- **Unrestricted** read access
- **Timer** MSR
  - Cache hit vs miss
  - Foreshadow attack [4]

✓ Leak **214** Byte/s

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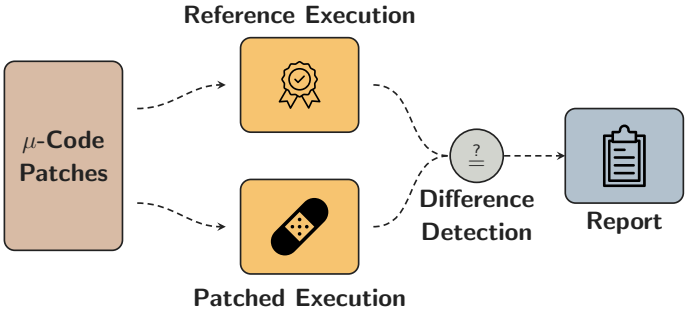
Case Study: uCode Diffing



- **Analyze** μ-Code Patches

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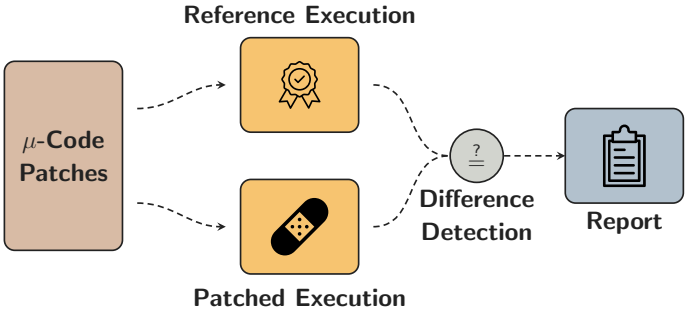
Case Study: uCode Diffing



- **Analyze** μ-Code Patches
- **Detect** new

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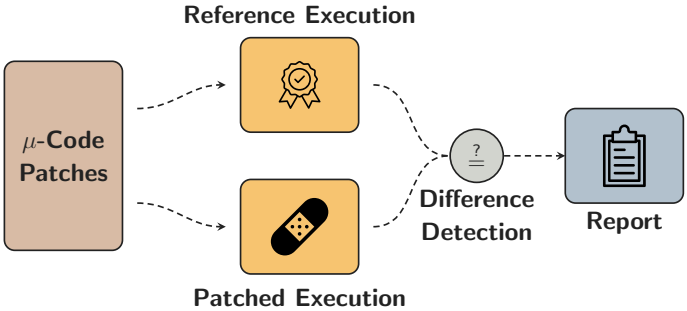
Case Study: uCode Diffing



- **Analyze** μ-Code Patches
- **Detect** new
- **Detect** affected instructions

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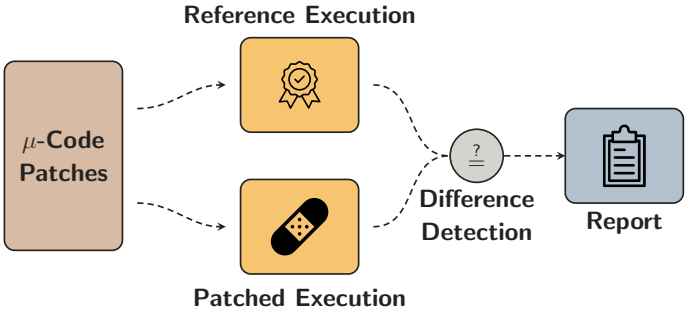
Case Study: uCode Diffing



- **Analyze** μ-Code Patches
- **Detect** new
- **Detect** affected instructions

✓ Before public disclosure

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Conclusion

- **Framework** https://github.com/IAIK/msrevelio

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Conclusion

- **Framework** `https://github.com/IAIK/msrevelio`
- **Case Studies**

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Conclusion

- **Framework** https://github.com/IAIK/msrevelio
- **Case Studies**
- **MSRs** enable defenses

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Conclusion

- **Framework** https://github.com/IAIK/msrevelio
- **Case Studies**
- **MSRs** enable defenses
- **MSRs** open new attack vectors

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Conclusion

- **Framework** https://github.com/IAIK/msrevelio
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- **MSRs** enable defenses
- **MSRs** open new attack vectors
- For more details ...

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Conclusion

- **Framework** https://github.com/IAIK/msrevelio
- **Case Studies**
- **MSRs** enable defenses
- **MSRs** open new attack
- For more details

Read the Paper

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Finding and Exploiting CPU Features using MSR Templating

IEEE Symposium on Security and Privacy 2022

Andreas Kogler **@0xhilbert** **andreas.kogler@iaik.tugraz.at**

References i

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- Daniel Gruss, Clémentine Maurice, Anders Fogh, Moritz Lipp, and Stefan Mangard. Prefetch Side-Channel Attacks: Bypassing SMAP and Kernel ASLR. In: CCS. 2016.
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Overall Results

CPU	AMD	Intel			
	Threadripper 1920X	i7-6700k	i7-8700k	i9-9900k	Xeon Silver 4208
μ-**Arch**	Zen	Skylake	Coffee Lake	Coffee Lake	Cascade Lake
μ-**Code**	0x8001137	0x9e	0xb4	0xde	0x5003102
# Found[1]	5244 (5223, 17, 4)	477 (363, 108, 5)	517 (388, 122, 7)	537 (413, 117, 7)	1109 (957, 142, 10)
# Undoc[1]	4876 (4873, 2, 1)	105 (68, 35, 2)	126 (89, 35, 2)	136 (99, 35, 2)	647 (591, 52, 4)
# Static[2]	4873 (4871, 2)	99 (68, 31)	121 (89, 32)	132 (99, 33)	601 (553, 48)
# Dynamic[2]	2 (2, 0)	4 (0, 4)	3 (0, 3)	2 (0, 2)	42 (38, 4)
# Similar	0	2	3	2	42

[1] $\sum$ (RW, RO, WO) [2] $\sum$ (RW, RO)

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