

GNU Jitter and the illusion of simplicity

or

Copying, patching and combining compiler-generated code in executable memory

or

The Anarchist's guide to GCC

or

The fun of playing with fire

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Binary Tools Summit 2022

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The master copy is at <http://ageinghacker.net/talks/>



Hello future viewers

The following resources are for those watching a recording of this presentation who want to occasionally pause the video and follow along:

- Source tarball for Structured, including GNU Jitter as a sub-package
<http://ageinghacker.net/bts2022/structured-simple-1.0.tar.gz> (recommended)
- Source tarball for GNU Jitter, including Structured as a sub-package (yes, this is not a mistake), requiring bootstrap with the Autotools to compile Structured as in this demo:
<http://ageinghacker.net/bts2022/jitter-0.9.285.tar.gz>
- Git source repository <http://git.ageinghacker.net/jitter>, requiring bootstrap with the Autotools plus Flex, GNU Bison, GNU Texinfo and so on. Use the tag **binary-tools-summit-2022** to get today's version.



History and rationale

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Demo: the Structured programming language

The Structured programming language

- Distributed along with Jitter as an example;
- Boring, unimaginative:
 - Pascal-style imperative language;
 - integer variables;
 - conditionals, loops;
 - recursive subprograms.
- Simple, clean implementation
 - Two VM code generators:
 - stack-based code;
 - register-based code
 - (choose with a command-line-option);
 - minimal build system example including Jitter, with Autoconf / Automake;
- Fast with little effort

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Demo



Jitter contains some assembly

We are currently supporting ELF and COFF configurations using GCC on:

- aarch64-unknown-linux-gnu
- alphaev4-unknown-linux-gnu
- alphaev67-unknown-linux-gnu
- arm-beaglebone-linux-gnueabihf
- arm-replicant-linux-androideabi
(Android 6, tested on my Replicant. More recent versions probably work as well)
- m68k-unknown-linux-gnu
- mipsel-unknown-linux-gnu
- mips-unknown-linux-gnu
- powerpcle-unknown-linux-gnu
- powerpc-unknown-linux-gnu
- riscv32-unknown-linux-gnu
- riscv64-unknown-linux-gnu
- s390x-ibm-linux-gnu
- sparc64-unknown-linux-gnu
- sparc-unknown-linux-gnu
- x86_64-unknown-haiku (64-bit Haiku)
- x86_64-unknown-linux-gnu
- x86_64-w64-mingw32
- x86_64-unknown-*bsd*

Not all of these configuration are supported as efficiently as you saw, yet.

More will come.



Simple dispatches and why we are ignoring them

As an alternative to what you saw in the demo the **same** VMs can also run as **interpreters instead of JITs**.

One of two techniques:

- **switch** dispatch
- **direct-threading** dispatch

These are **slower** portability fallbacks, with **identical semantics**; [Saiu, 2017] shows how they work. **extremely portable**.

[If I have time: **minimal-threading** dispatch also exists as a middle-ground compromise between interpreter and JIT]

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Specialisation

Turn a generic VM instruction definition...

add VM instruction: Jitter specification

```
instruction add (?R, ?Rn 1, !R)
  code
    JITTER_ARGN2 = JITTER_ARGNO + JITTER_ARGN1;
  end
end
```

... into every possible instantiation of register and immediate.

One example:

add specialisation < /n1/r4: Generated C, macroexpanded, simplified

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add_r4_n1_r4_begin:
  _local_state.r4 = _local_state.r4 + 1;
add_r4_n1_r4_end:
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add specialisation < /n1/r4, compiled

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Replication

(The same block of hardware instructions shown above, delimited by two labels:)

add specialisation r4/n1/r4, compiled

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Easy: copy memory between the two labels into executable memory (allocated with `mmap`):

JIT-time replication: append an add/r4/n1/r4 instruction

```
size_t vm_instruction_size_in_chars  
= ((char *) && add_r4_n1_r4_end  
    - (char *) && add_r4_n1_r4_begin);  
memcpy (executable_memory_end,  
        && add_r4_n1_r4_begin,  
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executable_memory_end += vm_instruction_size_in_chars;
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How do we specialise add %r4, 3, %r4?

- As add_r4_nR_r4 ...

nR means that the literal number is Residual: we load into a register or memory via assembly code, filled in by the Jitter runtime.

add/_r4_nR_r4 compiled, with 0x3 as nR

- `movl $0x3,%r12d`
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We can even have different assembly code for different constants.
For example on x86_64 **the literal 0x0 can be loaded in a more efficient way than other numbers.**

add/_r4_nR_r4 compiled with 0x0 as rR

```
xorl %r12d,%r12d  # This only works for 0x0
movq %r12,%r8
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Same for small constants on most RISCs.

(A hardware register has been reserved)

This is **very architecture-specific**, and a little laborious, but...

... VM-independent: **the complexity is all in Jitter!**



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How do we perform jumps from a VM instruction to another?

- One way would be by materialisation:

That works (I used to do that) but is **slow**.

- Much better solution: generate something like

b \$f compiled, with \$t being patched in

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Fast branches (2/2)

There are two main problems

- How to present this to the user in a friendly way
 - `JITTER_BRANCH_FAST(label)`,
 - `JITTER_BRANCH_FAST_IF_NONZERO(expression, label)`
 - `JITTER_PLUS_BRANCH_FAST_IF_OVERFLOW(lvalue, rvalue, rvalue, label)` ...
- How to implement this (**where to patch**)?
 - We need a new idea: `patch-ins`.

[Quick demo with uninspired

[unless I am very late]

- conditional branch
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Patch-ins

The fast-branching macro expands to something like:

(Macro-expanded) GNU C, simplified

```
asm goto (".pushsection .data, 42\n"
          ".quad hole_to_fill_%=\n"
          ".quad \" SPECIALIZED_INSTRUCTION_ID \"\n"
          ".quad \" PATCH_IN_CASE \"\n"
          ".popsection\n"
          "hole_to_fill_%=: \n"
          ".skip \" ROUTINE_LENGTH_IN_BYTES \"\n"
          : /* inputs... */
          : unreachable_label_jumping_where_gcc_cant_know);
```

This trick uses subsections. A pointer to the memory to patch is stored in a global table; the displacement between that address and an instruction start address is a literal constant.



C restrictions: global variables

C globals are accessed with **PC-relative** instructions on modern architectures.

- `a_global`

$\Rightarrow (* \text{ } \text{_a_local_struct-} \gt \text{a_global_address})$

- wrapping mechanism:

```
#define a_global \
    (* \text{_a_local_struct-} \gt \text{a_global_address})
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Jitter specification

```
wrapped Globals
  my_datum
  prompt_string
end
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```
wrapped-global
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end
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C restrictions: calling C functions (1/3)

Functions are also accessed with **PC-relative** instructions.

Same trick necessary...

- `a_function`

$\Rightarrow (* \text{ } \text{_a_local_struct-} \gt \text{a_function_address})$

$\text{a_function_address} = \text{a_function_addr}$

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Jitter specification

wrapped-functions

 putc

 getc

end

... but this is not enough!



C restrictions: calling C functions (1/3)

Functions are also accessed with **PC-relative** instructions.

Same trick necessary...

- `a_function`

$\Rightarrow (* \text{ } \text{_a_local_struct-} \gt \text{a_function_address})$

- wrapping mechanism:

```
#define a_function \
    (* \text{_a_local_struct-} \gt \text{a\_function\_address})
```

Jitter specification

```
wrapped-functions
```

```
    putc
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C restrictions: calling C functions (2/3)

On some architectures / ABIs **calling a C function clobbers CPU state**: for example the global pointer register on Alpha, or a floating point status register on SH4. [If I have time: violating the C ABI with respect to call-clobbered registers can be useful]

- A wrapped function call should expand to an expression “like”:

```
{ PRE_PROCEDURE_CALL_CODE;  
  int _res  
  = (* _a_local_struct->a_function_address) (args);  
  POST_PROCEDURE_CALL_CODE;  
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```

↳ <http://ageinghacker.net/2012/05/10/calling-c-functions-on-alpha/>

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- The macro must work with any arity, any input type, **any output type** — and **void** is special.
- The actual definition is **complex** and requires **GNU C** (but is well factored).



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- The actual macro needs:
 - statement-expressions;
 - `typeof`;
 - `__builtin_choose_expr`;
 - `__builtin_types_compatible_p`;
 - different definition for functions returning void.

For more information use `git grep 'Function wrapping'`

- Still very easy to use:

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C operators implemented as out-of-line routines

Very architecture-dependent:

- Sometimes solvable by command-line options.

Ex.: struct assignment on PowerPC:

`-mblock-move-inline-limit=8192`

↳ <http://www.h3xpl0it.com/2011/05/17/powerpc-struct-move/>

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http://ageinghacker.net/jitter/2012/07/01/c-operators-implemented-as-out-of-line-routines/



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What we have learned up to this point:

- VM instruction **code blocks require care**:
 - write C...
 - ...think assembly
- No restrictions in called C functions;
- No restrictions in **non-relocatable** VM instructions;
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- **Relatively minor** annoyances.



What can *really* go wrong

GCC can compile C in ways that are **legitimate**, but **break our strategy** of copying and recombining hardware instruction blocks.

- reorder;
- tail-merging;
- inconsistent register assignments across branches;
- far branches;
- PC-relative loads to materialise constants.



What can go wrong: reorder (1/2: the problem)

When replicating we `memcpy` from `the_beginning` to `the_end`:

A specialised instruction, compiled

`the_beginning:`

...

...

`the_end:`

But GCC might (legitimately) `reorder blocks`:

A specialised instruction, compiled — negative length?

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.foo:  
  ...  
the_end:  
  ...  # Something else  
the_beginning:  
  ...  
  jmp .foo
```

Code from `different` VM instructions may even be `intertwined`.



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In this case the solution is easy: GCC has a
-fno-reorder-blocks option

The generated file *umprefix-vm2.c* **must** be compiled with
-fno-reorder-blocks.

This GCC optimisation option is **necessary for correctness!**

`JITTER_CFLAGS` contains it.

(Out of defensiveness, VM code checks at startup that specialised instruction blocks are disjoint and sizes are non-negative.)



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Two VM instructions happen to behave the same way at the end:

foo VM instruction

foo_beginning:

...

xxx

yyy

foo_end:

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Use **GNU C assembly constraints** to pretend there are dependencies, and that a variable is modified in many different ways: **prevent factoring by making tails appear different**.

foo VM instruction, in C

```
foo_beginning:
...
asm (: "+X" (variable),
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The variable must actually be used.

[The Array's base is in a reserved register: the obvious candidate, but I am not speaking of The Array in this presentation]

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Register-assignments across branches

Can we guarantee that GCC uses the same register assignment at a branch site and at the target site?

- the target is always the beginning of a VM instruction

compiled code going to Ltarget

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jmp .Ltemp
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.Ltemp:
    mov ..., %rdx # Register assignment now compatible with Ltarget
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[To do: There will be no time for the details: the solution uses `asm goto` in a creative way, lying to the compiler]



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→ Jitter is the right way to factor

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http://ageinghacker.net/jitter/

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Code reuse

- Good architecture-dependent support is **complicated**
- Possibly **unjustified effort** for a single VM
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Is this the right thing?

Is this complexity necessary?

- In an ideal world a VM generator would be simpler.
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↳ The complexity of the environment is reflected in the complexity of the jitter generator.
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It is not necessary to have a complex VM generator to implement jitter. It is not necessary to have a complex environment to implement jitter. It is not necessary to have a complex C compiler to implement jitter.

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Any questions?



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