Characterization and Design of Sequential Circuit Elements to Combat Soft Error[1]

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Abstract - **This paper performs analysis and design of latches and flip-flops while considering the effect of event upsets caused by energetic particle hits. First it is shown that the conventional analysis of this effect in sequential circuit elements (SCEs) tends to underestimate the threat posed by such events. More precisely, there exists a timing window close to the triggering edge of the clock during which a SCE is more vulnerable to the particle hit. This phenomenon has been ignored by previous work, resulting in false negatives. Next the paper explains how to size transistors of a familiar SCE i.e., a clocked CMOS latch, to make it more robust to such events. Experimental results to validate the characterization and transistor sizing steps are provided and discussed.**

I. INTRODUCTION

As CMOS transistors are scaled down toward the 32nm CMOS technology node, circuit reliability cannot be ignored. One of the important reliability concerns in today's VLSI circuits is the incidence of soft errors which occur due to various types of radiations, i.e., high energy neutrons present in terrestrial cosmic radiations or alpha particles which originate from impurities in the packaging materials. When these energetic particles hit a sensitive region in a sequential circuit element (SCE), they generate charges which can be collected by source/drain diffusion nodes, causing a single-event upset (SEU). SEU can thereby alter the logic state of the node resulting in a soft error.

Due to technology scaling, the supply voltage and the node capacitance in the VLSI circuit decrease. The resulting quadratic reduction in stored charge is the main reason for increased vulnerability to soft errors in nanometer scale technologies. There are different hardening techniques to protect a SCE against the soft error. These techniques may generally be classified into three categories vis-à-vis device-level, system-level and circuit-level [1] as reviewed below

    i.   Device-level hardening approaches are mainly focused on the reduction of the effects of the charge collection at the site of the particle hit. These techniques typically involve changes to the device fabrication process. However, the cost may be too much for mainstream applications.

   ii.   System-level hardening approaches resort to adding redundancy in the design or applying error detection/correction circuitry. However, the irregular multilevel structure of the combinational logic results in high design overhead for these techniques, which diminishes their benefit in most designs.

  iii.   Circuit-level hardening techniques include the insertion of resistance and capacitances in the gate cell to slow down the propagation of transient voltages, increasing node capacitances to alleviate the SEU, avoiding dynamic logic families, and removal of floating nodes in the circuits. In this paper, we focus on the circuit-level hardening techniques.

In an integrated circuit, both sequential and combinational logics are all susceptible to soft errors. A number of researchers have addressed soft errors on combinational logic and proposed solutions to alleviate their effect as single event transition (SET) [2]. The soft error reliability issue for the SCEs (i.e., latches and flip-flops) has also been investigated. In [3] SEU due to particle hit in latches was investigated, and stack tapering and use of explicit capacitance at the feedback node were proposed as hardening techniques. Although this work discusses the effect of radiation on the latches holding some value (the latch is in its opaque mode), it does not consider the case where the latch is in the transient phase of its operation. The authors of [4] showed that by proper sizing, it is possible to create immunity from SETs generated in the combinational logic gates. The proposed technique leverages temporal masking by selectively increasing length of the latching windows of the flip-flops, thereby preventing faulty transients from being registered. Unfortunately, this work does not consider the effects of radiation-induced SEUs on soft error rates.

In this paper we study the effect of the radiation on the master-slave flip-flops during their transition mode (i.e., from a timing viewpoint, the particle hit occurs near the triggering edge of the clock). We show that a flip-flop which has been hardened to the radiation during its opaque phase may still be susceptible to the radiation with the same energy level during a timing window close to the triggering edge of the clock.

The remainder of the paper is organized as follows. Section II provides background on the model which is used to evaluate the effect of the particle hits on the SCE characteristics. It also defines the terminology which will be used in subsequent sections. The effect of the particle hit in a specific critical timing window close to the triggering edge of the clock for the flip-flop is described in Section III. An analytical model formulation of the transistor sizing method to combat the soft error is presented in Section IV. Section V reports our simulation results whereas section VI concludes the paper.

II. BACKGROUND

This section provides the outline of the soft error model that we use. We first explain the model for a single particle strike. Next,

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we review the notion for the setup time, hold time, and clock-to-q delay for flip-flops and latches. Finally, we describe the transparent and opaque operation phases for latches.

A. Technology and Particle Strike Model

All results reported in this paper are obtained by HSPICE [8] simulations using a predictive 90nm CMOS technology model [9] with 1.2V for the supply voltage and 0.397V (–0.339V) for nominal threshold voltages of NMOS (PMOS) transistors.

The transient current through a reverse-biased p-n junction because of the charge deposition due to a particle hit at a node in the circuit may be modeled as a current pulse I_{hit} at the site of the particle strike [5] as follows:

$$I_{hit}(t) = \frac{2Q}{\tau\sqrt{\pi}}\sqrt{\frac{t}{\tau}}\exp\left(\frac{-t}{\tau}\right) \qquad (1)$$

where Q is the charge deposited as a result of the particle strike and τ is a technology dependent pulse shaping parameter. Figure 1 shows I_{hit} dependencies on Q and τ. The authors of [6] calculated τ for 90nm technology using device level 3D simulations and reported it to be 90ps. In this paper we use the same value for τ.
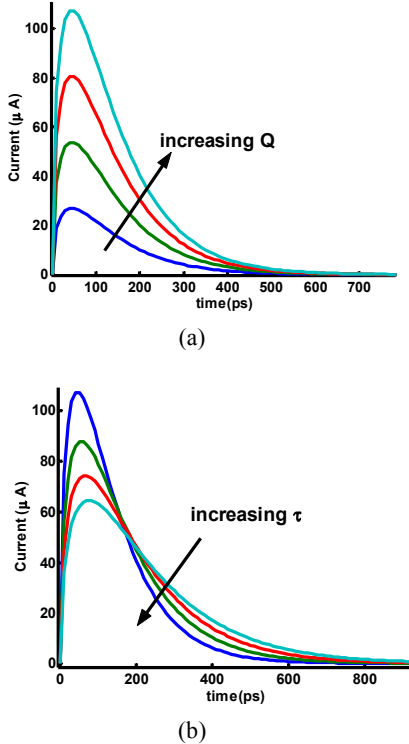

(a)

(b)

Figure 1. I_{hit} variations by (a) Q and (b) τ.

A soft error occurs when the collected charge, Q, exceeds some critical charge level, Q_{crit}, of a circuit node. Q_{crit} is the minimum charge injected in order to flip the value of the node. When a particle hits the p-type diffusion area, it generates a current which tries to upset bit 0 stored in the node. If the area is n-type, the current tries to upset the stored bit with value 1.

In [7] a methodology for estimating the particle-induced soft error rate (SER) has been proposed, according to which the dependence of SER on circuit and environmental parameters is expressed as:

$$SER \propto N_{flux}C_S \exp\left(-\frac{Q_{crit}}{Q_S}\right) \qquad (2)$$

where N_{flux} is the intensity of the Neutron flux and C_S is the area of the cross section of the node (drain or source region). Moreover, Q_S is the collection slope, which strongly depends on the doping concentration of the drain and source and also the supply voltage level.

B. Sequential Circuit Elements

Latches and flip-flops are sequential circuit elements used in synchronous designs where a clock edge is used to sample and store a logic value on a data line. The **setup time,** τ_s, is the *minimum time before* the active edge of the clock that the input data line must be valid for reliable latching. Similarly, the **hold time**, τ_h, represents the *minimum time* that the data input must be held stable *after* the active clock edge. The active clock edge is the transition edge (either low-to-high or high-to-low) at which data transfer/latching occurs. The **clock-to-q** delay refers to the propagation delay from the 50% transition of the active clock edge to the 50% transition of the output, q, of the latch/register. Figure 2 illustrates the setup and hold times, which are denoted by τ_s and τ_h, respectively.
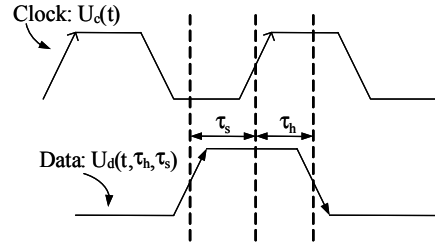

Figure 2. Definitions of the setup and hold times.

Latches have two operational phases: one is transparent phase when they can capture the input data and another one is opaque phase when they keep the captured input data. For a positive latch, when the clock is high, the latch is in the transparent phase and when the clock is low, it is in the opaque phase. For negative latches it is vice versa. Figure 3 shows transparent and opaque phases for a positive latch.
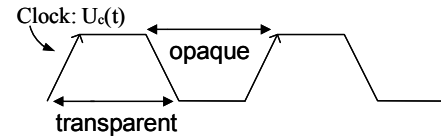

Figure 3. Transparent and opaque phases for a positive latch.

III. SOFT ERROR VULNERABILITY

The susceptibility of the latches to the particle hit has been previously investigated, but all of the published work that we have seen considers particle hits in the opaque phase of a latch. Here we show that there is a timing window close to the triggering edge of the clock during which the latch is more vulnerable to the particle hit than it is during its opaque phase. It means the Q_{crit} for this timing window is lower than the Q_{crit} for an opaque latch. We call this window *Soft Error Vulnerability Window* (SEVW). We point out that in general, the SEV window is different from setup/hold time window. Figure 4 shows SEVW for a positive latch.
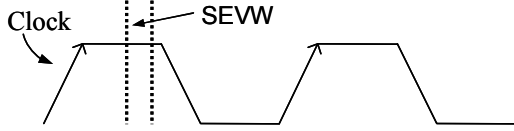
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Figure 4. Soft Error Vulnerability Window for a positive latch.

In our experimental setup, we first do HSPICE simulation to determine Q_{crit} for the latch in the opaque phase. Next we use this value to characterize the SEVW by sweeping the hitting time of the particle around the triggering edge of the clock. The SEVW is determined as the timing window where values of injected charge that are less than Q_{crit} will still cause a SEU in the latch. Figure 5 shows how a $Q < Q_{crit}$ causes a failure when the particle hits in the SEVW. The simulation is done for a master-slave flip-flop (master-slave flip-flop is explained in IV.A).

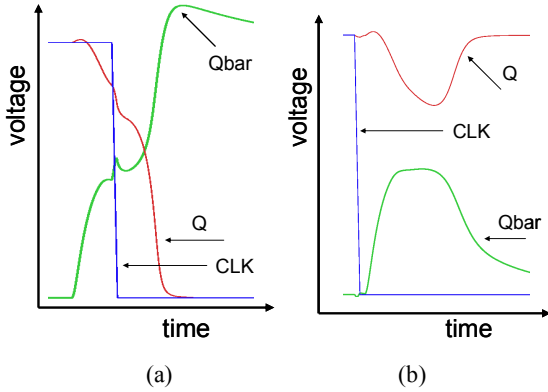(a)   (b)

Figure 5. Comparison between the effect of a particle hit (a) in the SEV window and (b) in the opaque phase of a positive latch considering the injected charge $Q < Q_{crit}$. In both cases, we set $Q=0.99Q_{crit}$.

IV. CIRCUIT LEVEL ANALYSIS

We describe a selective transistor-level sizing approach for a master-slave flip-flop. In this technique, we first analyze the circuit of the flip-flop which we want to make robust to the particle hit. Then we present an analytical model for characterizing the effect of a particle hit during the SEVW for a conventional master-slave flip-flop.

A. Conventional Master-Slave Flip-Flop

This MS flip-flop consists of a positive and a negative latch in series. From a soft error analysis perspective, these two latches have the same behavior. Thus, we analyze only one of the latches.

A positive edge latch is shown in Figure 6. It has positive setup time and negative hold time (i.e., the hold time window edge is before the active edge of the clock). This type of latch is common in ASIC designs. The latch circuit has a feedback path. In static logic circuits without the feedback, soft error can only result in a transient error which disappears after a while. The presence of the feedback path during the opaque phase may cause the value that this SCE holds to flip. The feedback forces the circuit to keep the faulty value for the remainder of the opaque phase. Memory elements such as the 6-transistor SRAM cell that have a feedback in their circuit also suffer from the same problem.

B. Analytical Model

Through analysis and simulations of the latch depicted in Figure 6, we know that $Qbar$ is a node which is sensitive to the particle hit. We show our analysis for this node (the analysis for Q is

similar). Without loss of generality, suppose the input to the latch is 1 i.e., $Qbar$ and Q values are 0 and 1, respectively. An energetic particle hits the p-diffusion area at $Qbar$ and creates a positive current which increases the voltage level of the node. The hit occurs at time t_{hit}, which is before the triggering edge of the clock. The analysis for the case in which the value of $Qbar$ is 1 and a particle hits the n-diffusion area at $Qbar$ is similar and omitted for brevity.

To do the analysis, we divide the time axis into two different zones. One is before the triggering edge of the clock and the other is after it. The reason is that when the triggering edge of the clock is applied to the latch, the topology of the latch circuit changes. Before the triggering edge (i.e., during the transparent phase of latch operation), the feedback loop is open and the input clocked-inverter passes the input data to the latch. In contrast, after the triggering edge (in the opaque phase of latch operation), the input clocked-inverter is open and the feedback loop is closed.
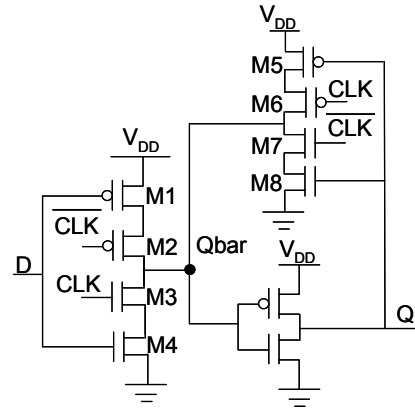

Figure 6. Transistor-level schematic of a positive C²MOS latch.

We consider a current (I_{hit}) given by equation (1) is injected into $Qbar$. The voltage of $Qbar$ following the particle hit is calculated by writing a KCL equation at the node. Figure 7 shows the current-based model of the positive latch when CLK is 1 (the transparent mode). Before the negative edge of the clock, the current equation of node $Qbar$ is as follows:

$$C_{Qbar} \frac{dV_{Qbar}}{dt} = I_{hit} + I_{in}(V_{Qbar}) \tag{3}$$

where C_{Qbar} is the capacitance at $Qbar$ and I_{in} is the discharging current of the pull-down network of the input clocked-inverter. Hence,

$$V_{Qbar} = \frac{1}{C_{Qbar}} \int_{t_{hit}}^{t_{clkedge}} \left(I_{hit} + I_{in}(V_{Qbar}) \right) dt \tag{4}$$

where $t_{clkedge}$ is time instance at which the falling edge of the clock arrives (latching action) and t_{hit} is the time instance for particle hit at $Qbar$.

The pull-down network of the input clocked-inverter, modeled as an equivalent NMOS transistor, is operating in the linear region. Therefore, we can write:

$$V_{Qbar}(t_{clkedge}) =$$

$$\frac{1}{C_{Qbar}} \int_{t_{hit}}^{t_{clkedge}} \left(\frac{2Q}{\tau\sqrt{\pi}} \sqrt{\frac{t}{\tau}} \exp\left(\frac{-t}{\tau} \right) + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(2(V_{GS} - V_{th})V_{Qbar} - V_{Qbar}^2 \right) \right) dt \tag{5}$$

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As mentioned in II.A, τ =90ps for the 90nm CMOS technology and Q is the amount of charge deposited by the particle hit in (5).
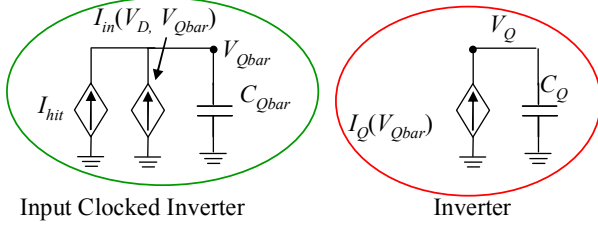

Figure 7. Current based model of a latch when feedback loop is open.

Applying the derivative operator on both sides of (5) gives:

$$\frac{dV_{Qbar}}{dt} - \alpha V_{Qbar} + \beta V_{Qbar}^2 = 0 \qquad (6)$$

where V_{Qbar} at time $t_{clkedge}$ is a function of $t_{skew} = (t_{clkedge} - t_{hit})$, and α and β are appropriate coefficients obtained by simplifying and collecting terms in the derivative expression. Since the input voltage at node D is 1, the initial voltage at node $Qbar$ is:

$$V_{Qbar}(t_{hit}) = 0 \qquad (7)$$

The voltage V_{Qbar} at time $t_{clkedge}$ is calculated easily by a numerical method such as the Euler method. Therefore the voltage of node $Qbar$ at $t_{clkedge}$, $V_{Qbar}(t_{skew})$, is given by solving equations (6) and (7). The voltage at node Q, $V_Q(t_{skew})$ is given by using the current model which is explained below. It is worth reiterating that the voltages at node Q and $Qbar$ for a specified particle hit (given Q and τ) are functions of t_{skew}.

Now, let us consider the latch after clock edge when the feedback loop is closed. Figure 8 shows the current based model of the latch when the feedback loop is closed. Again by considering the current equation (KCL) at node $Qbar$:

$$V_{Qbar}(t) = V_{Qbar}(t_{clkedge}) + \frac{1}{C_{Qbar}} \int_{t_{clkedge}}^{t} \left(I_{hit} + I_{Qbar}(V_Q, V_{Qbar}) \right) dt \qquad (8)$$

where I_{Qbar} is the discharging current of the pull-down network of the clocked-inverter in the feedback path, and C_{Qbar} is capacitance at node $Qbar$.

The current sources shown in Figure 8 are nonlinear functions of input-output voltages V_Q and V_{Qbar}. Depending on the input-output voltages, the transistors are in linear, saturation, or subthreshold regions and the current function is of quadratic, linear, or exponential forms.

There are two cases of for particle strike at time instances before the clock edge. We can solve equations (6) and (7) to determine V_{Qbar} for $t_{clkedge}$. However to solve the rest of the problem and see the evolution of V_{Qbar} after the clock edge (solving equation 8), we need to consider these two different scenarios. One is when a failure (SEU) occurs at the latch output and the other is when there is no failure at the output of the latch.

I.   Failure Scenario

In this case V_{Qbar} changes, and subsequently, the output of the latch changes value. In this case, since V_Q is still V_{DD} in the beginning (after the clock edge), the pull-down network of the clocked-inverter in the feedback path is ON whereas the pull-up is OFF. The pull-down has a discharging current and tries to keep V_{Qbar} at 0 level, but the charge that is injected in the stricken node ($Qbar$ node) is large and causes the Q flips from 1 to 0. Hence, the

pull-up network of the clocked-inverter in the feedback turns on and the pull-down network turns off. Now, we have a current from the pull-up network which charges up the node capacitances. After a while since the current injected from the hit is strong, even the current in the pull-up network becomes negative (flows toward V_{DD}). Figure 9 illustrates the changes in the currents of the pull-down and pull-up networks of the clocked-inverter in the feedback path for the failure scenario.
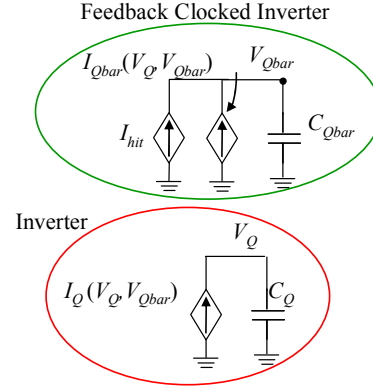

Figure 8. Current based model of a latch when feedback loop is closed.

So, the KCL at node $Qbar$ becomes:

$$V_{Qbar} = V_{Qbar}(t_{clkedge}) + \frac{1}{C_{Qbar}} \left(\begin{array}{c} \int_{t_{clock\ edge}}^{t_{Q\ flips}} \left(I_{hit} + I_{disch}(V_Q, V_{Qbar}) \right) dt \\ + \int_{t_{Q\ flips}}^{t_{end\ of\ tail}} \left(I_{hit} + I_{charge}(V_Q, V_{Qbar}) \right) dt \end{array} \right) \qquad (9)$$

where $t_{Q\ flips}$ is the time which Q flips from 0 to 1, $t_{end\ of\ tail}$ is the end time of the tail of the current induced by the hit, and I_{disch} and I_{charge} are the discharging and charging currents of the pull-down and pull-up networks of the clocked-inverter in the feedback path, respectively.

II.   Non-failure Scenario

In this case, V_{Qbar} does not change and keeps its original value (here 0). Similarly, the output voltage of the latch (V_Q) does not change. Since V_{Qbar} does not reach the threshold point ($V_{DD}/2$) for V_Q to flip from 1 to 0, the pull-down network of the clocked-inverter in the feedback path stays ON and tries to discharge the current which injected to the stricken node. Meanwhile, there is no current passing through the pull-up network which means the transistors in that path are OFF. Figure 10 depicts the changes in the currents of the pull-down and pull-up networks of the clocked-inverter in the feedback path for the non-failure scenario. There is a negligible variation in the current of the pull-up network during the clock transition from 1 to 0 due to the Miller effect of M6 and M7. So, the KCL at node $Qbar$ becomes:

$$V_{Qbar} = V_{Qbar}(t_{clkedge}) + \frac{1}{C_{Qbar}} \int_{t_{clkedge}}^{t} (I_{hit} + I_{Qbar}(V_Q, V_{Qbar})) dt \qquad (10)$$

By using equations (9) and (10) and knowing the voltage of node $Qbar$ at the clock edge from equations (6) and (7), we can evaluate that the circuit fails or latches the correct value. The purpose of presenting the above analysis was to show that the problem can be analytically set up and solved; the formulation also gives us insight about what the effect of various transistor sizes are on the failure or non-failure of the latch under particle strike condition.
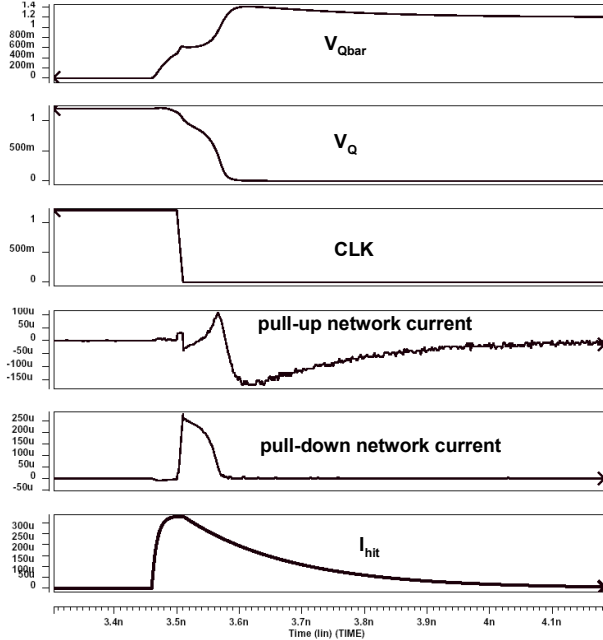
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Figure 9. Voltage waveforms for Qbar, Q and CLK signals and current variations in the pull-up and pull-down networks of the feedback clocked-inverter for the failure scenario.

V. EXPERIMENTAL RESULTS

In his section, we present the simulation results for the particle hit in the SEVW and a transistor sizing solution to overcome the soft error problem in a positive latch. Furthermore, we show the sensitivity of SEU to the sizing of each transistor in the discharging path of the input and feedback clocked-inverters. We also compare different hitting times of the particles in SEVW and their effect on the sizing approach. Moreover, we investigate the area and power consumption overheads of our technique. Finally, we show the Q_{crit} dependency to the hitting times of the particles to prove our claim for existence of SEVW.

A. Transistor-Level Sizing and Sensitivity Analysis

As mentioned in section III, SEVW is the time window which has higher vulnerability to the particle hit compared to the opaque phase of operation for the latch. However, even in this time window, there are more critical t_{hit}'s compared to other hitting times in SEVW. This phenomenon necessitates increase in the size of the transistors to combat the SEU for the most critical t_{hit}'s. We thus need to consider our sizing technique for the worst t_{hit} (the most critical one) to have the best SER-resilient latch.

As seen from the analytical model of section IV.B, the discharging paths in the circuit play a substantial role in the SER-resilience of the MS latch. Transistor sizing can be performed for different discharging paths in the circuit, i.e., discharging paths of the input and feedback clocked-inverters. Simulation results show the optimum discharging path is the clocked-inverter in the feedback. On the other hand, there are two transistors (M7 and M8) in the discharging path of the clocked-inverter of the feedback. We can analytically say that the best transistor to size is M8 because it is connected to Q, which is itself undergoing an erroneous transition from 1 to 0. This makes the current of M8 weaker. Now by increasing its width, one can linearly compensate

for the decrease in the discharging current to overcome the SEU. Simulation results also prove our analysis.
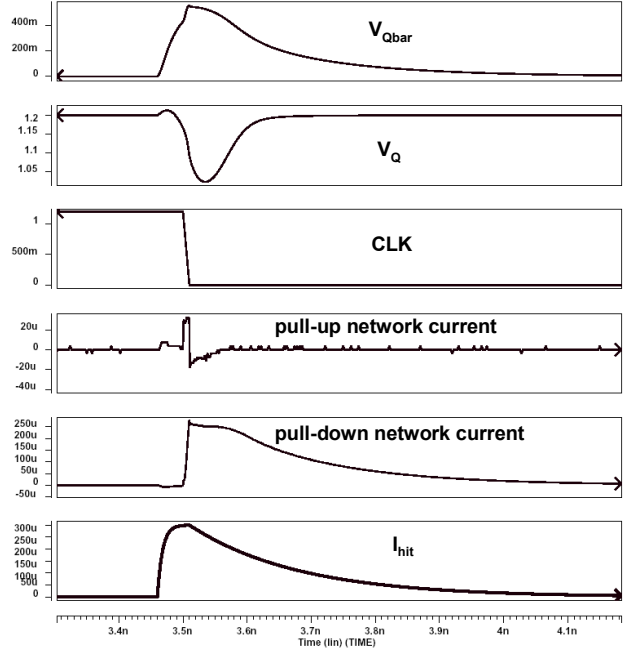

Figure 10. Voltage waveforms for Qbar, Q and CLK signals and current variations in the pull-up and pull-down networks of the feedback clocked-inverter for the non-failure scenario.

Increasing the width of transistor M7 is essentially the same as the techniques that increase the capacitance of the sensitive node of the circuit.

Note that in general we ought to do our design for the worst case and disregard the other special cases.

Table 1 and Table 2 show how much better our technique is in comparison with these other techniques. The important note is that to overcome the particle hit at the n-diffusion area (faulty transition at node *Qbar* from 1 to 0), we should increase the size of the PMOS transistors as well (the degradation effect on the discharging because of the increase in the size of the PMOS transistors is taken into the account). Since the circuit is symmetric, everything which is done for the NMOS transistors should also be considered for the PMOS transistors.

Note that in general we ought to do our design for the worst case and disregard the other special cases.

Table 1 shows the optimum sizing (i.e., a sizing solution which increases Q_{crit} for SEVW to Q_{crit} for the opaque phase) result for each discharging path considering the worst t_{hit}. Moreover, it shows the area and power consumption overheads for each case.

Next we report the simulation results for a t_{hit} in SEVW which is far from the clock edge and compare it to the case which particle hits the circuit at the worst time. In this particular case, there is enough time for the input clocked-inverter to discharge the charge injected by the particle hit before the triggering edge of the clock. Hence, the input clocked-inverter becomes more important than the one in the feedback path and appropriate sizing of its transistors can overcome the SEU. Table 2 shows the optimum sizing for each discharging path considering a non-

worst-case t_{hit}. As before, the table shows the area and power consumption overheads for each case.

Note that in general we ought to do our design for the worst case and disregard the other special cases.

TABLE 1: Optimum transistor sizing results for the positive latch considering worst-case T_{HIT}

Transistor names	size increase	Area increase	power consumption increase
Both M3 (M1) and M4 (M2)	25%	10%	8.8%
Both M7 (M5) and M8 (M6)	13%	5.2%	2.7%
M7 (M5)	49%	9.8%	4.7%
M8 (M6)	21%	4.2%	2.3%

TABLE 2: Optimum transistor sizing results for the positive latch considering a non-worst-case T_{HIT}

transistor names	size increase	area increase	power consumption increase
Both M3 (M1) and M4 (M2)	6%	2.4%	2.1%
Both M7 (M5) and M8 (M6)	10%	4%	2.1%
M7 (M5)	42%	8.4%	4%
M8 (M6)	15%	3%	1.7%

B. Hitting time and Q_{crit} dependency

In this section, we investigate the dependency of Q_{crit} on t_{hit}. It is obvious that Q_{crit} for SEVW is smaller than the other hitting times. Furthermore, for a hit inside the SEVW, there is a worst t_{hit} which yields the smallest Q_{crit}. To do this analysis precisely, we define $t_{skew} = t_{clkedge} - t_{hit}$, and with the aid of HSPICE simulation, we show the variation of Q_{crit} with t_{skew}. Negative t_{skew} means the hit occurs after the clock edge (during the opaque phase of latch operation). Figure 11 shows the result of the simulation which empirically validates the existence of a SEVW during which the flip-flop exhibits higher susceptibility to the particle hit compared to the opaque phase. On the other hand, when t_{skew} is larger than the upper bound of the SEVW (which occurs at some instance toward the end of the transparent phase of latch operation), as expected, Q_{crit} increases rapidly. For the large value of t_{skew}, Q_{crit} goes to infinity while the latch is still in the transparent phase.
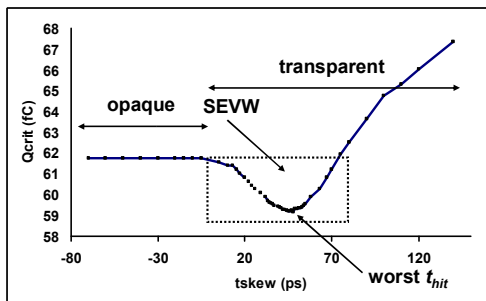

Figure 11. t_{skew} and Q_{crit} dependency.

VI. CONCLUSION

In this paper, we studied the effect of the particle hit at the sequential elements of the logic circuits. We started from the observation that the conventional analysis of this effect tends to underestimate the threat posed by such events by just considering the particle hits which occur in their opaque phase. We showed that there is a timing window close to the triggering edge of the clock which is more susceptible to the particle hit than their opaque phase. Consequently, we introduced an analytical model to calculate how to size the transistors in the conventional latch to combat the SEU. Finally, we validated our analysis and provided results of a simple sizing technique.

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