SYNCHRONOUS DERIVED CLOCK AND SYNTHESIS OF LOW POWER SEQUENTIAL CIRCUITS *

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Abstract Based on analyzing significance of controlling clock in design of low power sequential circuits, this paper proposes a technique where a gating signal is derived from the master latch in a flip-flop to make the derived clock have no glitch and no skew. The design of a decimal counter with half-frequency division shows that by using the synchronous derived clock the counter has lower power dissipation as well as simpler combinational logic. Computer simulation shows 20% power saving.

Key words Low power; Sequential circuit; Logic design; Derived clock

I. Introduction

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power considerations were mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed in VLSI design.[1] The continuing increase in chip scale and operating frequency has made power consumption a major concern in VLSI design. For example, the Power PC chip from Motorola consumes 8.5W, the Pentium chip from Intel consumes 16W, and DEC's alpha chip consumes 30W. The excessive power dissipation in integrated circuits not only discourages their use in a portable environment, but also causes overheating, which degrades performance and reduces chip life-time.[2] All of these factors drive designers to devote significant resources to reduce the circuit power dissipation. Indeed, the Semiconductor Industry Association had identified low-power design techniques as a critical technological need in 1992.[3]

In power dissipation of CMOS circuits the dominant term is the power required to charge or discharge the capacitor of the given node in the circuit. The relative power dissipation can be expressed by the following formula:

$$P = 0.5 C_L \cdot V_{DD}^2 \cdot f_{CLK} \cdot E_{SW} \quad ,$$

where C_L is the physical capacitance at the node, V_{DD} is the supply voltage, f_{CLK} is the clock frequency, E_{SW} (referred to as the average switching activity) is the average number of output transitions per clock cycle $1/f_{CLK}$.

The sequential circuits in a system are considered major contributors to the power dissipation since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. To distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the total node capacitance of the clock net. Recent studies indicate that the clock

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signals in digital computers consume a large (15% - 45%) percentage of the system power. Thus, the circuit power can be greatly reduced by reducing the clock power dissipation.

Most efforts for clock power reduction have focused on issues such as reducing voltage swings, buffer insertion and clock routing.[4] In many cases switching of the clock causes a lot of unnecessary gate activity. For that reason, circuits are being developed with controllable clocks. This means that from the master clock other clocks are derived which, based on certain conditions, can be slowed down or stopped completely with respect to the master clock. This circuit itself is partitioned in different blocks and each block is clocked with its own (derived) clock. The power savings that can be achieved this way are very application dependent, but can be significant.

In Ref.[5] the authors presented a technique for saving power in the clock tree by stopping the clock fed into idle modules. However, a number of engineering issues related to the design of the clock tree were not addressed. The added gates in the clock paths may introduce glitches in the clock signal. Also the propagation delays of gates are harder to control, thus introducing unwanted skew. Therefore, the proposed approach has not been adopted in practice.

Based on the above discussion, this paper looks for a secondary clock, which is derived from the master clock and meets all requirements, such as being glitch-free and having no additional skew. Next, this paper shows how to use a synchronous derived clock for designing a decimal counter with lower dissipation and simpler combinational logic. Circuit simulation is used to check the quality of the derived clock and its capability to reduce power dissipation of sequential circuits.

II. Derivation of A Qualified Clock from Master Clock

Assume that the master clock is NAND-gated by a control signal to obtain the derived clock. For the derived clock to be glitch-free, the control signal should be "clean". Suppose the original control signal comes from a combinational circuit. It may thus have some glitches, therefore, it must be filtered by a storage unit, e.g. a latch or a flip-flop. Fig.1(a) shows a CMOS flip-flop, where input D may contain glitches, clk_1 is considered the output of an inverting buffer.[6] clk_0 and clk_1 can be considered as last two stages in a clock tree. Since the original control signal D may contain glitches and may not be in synchrony with the clock, it cannot be directly used for gating the NAND gate in order to obtain the derived clock. Thus, in Fig.1(a) we may take the output Q of the flip-flop to gate clk_0 by using a NAND gate in the circuit instead. It seems that the derived clock clk_2 and clk_1 have the same phase delay with respect to clk_0. However, the timing diagram shown in Fig.1(b) indicates that the derived clock clk_2 has a skew of $(t_f + t_g)$, where t_f is the clock-to-Q delay and t_g is the delay of NAND gate. Besides, when Q makes a falling transition, it may have simultaneous high level with clk_0. A glitch may generated if they are ANDed each other. Therefore, the output Q (or $\overline{Q}$) of a flip-flop is directly used as the derived clock, instead of the gated signal, in design of asynchronous sequential circuits. (We say asynchronous, because now not all flip-flops are triggered at the same time.)

If we analyze the timing diagram shown in Fig.1(b) we can observe that the trouble is due to "simultaneous" changes of clk_0 and the gating signal Q. If the gating signal changes at the rising edge of clk_1 rather than at the falling edge, the derived clock will be qualified. Thus we add another latch to the master-slave flip-flop, as shown in Fig.2(a). We notice that the output Q' of this latch changes at the rising edge of clk_1 and it can be used to gate the original clock clk_0. From the timing diagram shown in Fig.2(b) we find that both transitions of clk_0 are covered by the zone

of Q' = 1 and the derived clock clk_3 is qualified, that is, without glitches and skew. Thus, it is synchronous with the clock clk_1.

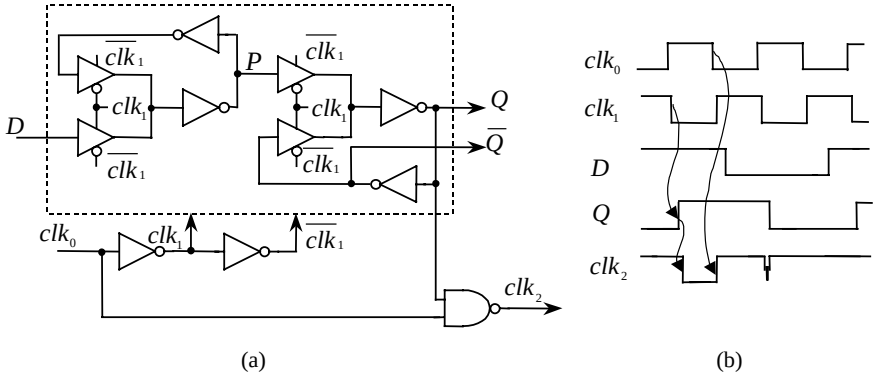

Fig. 1 Scheme 1 for gating clock

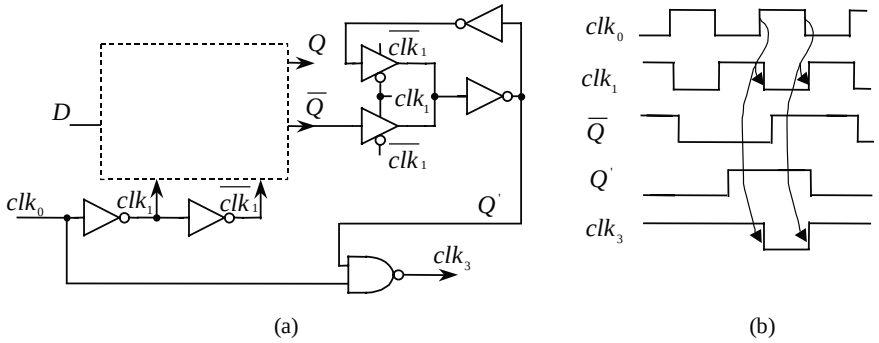

Fig. 2 Scheme 2 for gating clock

We should point out that if $\overline{Q}$ in Fig.1(a) acts as the excitation input of a D flip-flop, the master latch of this flip-flop thus can act as the "additional latch". Then its output, such as the internal node P in Fig.1(a), can be used as the gating signal. As a special case, if $\overline{Q}$ is fed back to D input of the same flip-flop, i.e. $D = \overline{Q}$, this flip-flop will work in the state of dividing frequency by two. In a sequential circuit, thus, as long as there is a flip-flop, which works as a circuit of dividing frequency by two, we can derive a qualified clock with half-frequency by using the output of its master latch. The derived clock will be synchronous with clk_1 and almost without expense.

III. Design of A Low Power Synchronous Counter

Taking a decimal counter as an example, the next state of the counter is shown in Tab.1. If D flip-flops are adopted we can obtain Karnaugh maps for its excitation functions D_3, D_2, D_1 and D_0 from the next states in Tab.1, as shown in Fig.3(a). In these maps an empty box represents the don't-care condition. The optimized excitation functions are:

$$D_3 = Q_2 \cdot Q_1 \cdot Q_0 + Q_3 \cdot \overline{Q_0},$$
$$D_2 = Q_2 \oplus (Q_1 \cdot Q_0),$$

$$D_1 = \overline{Q}_3 \cdot \overline{Q}_1 \cdot Q_0 + Q_1 \cdot \overline{Q}_0,$$
$$D_0 = \overline{Q}_0$$

The corresponding circuit realization is shown in Fig.3(b). This is a traditional synchronous design for a decimal counter.

Tab.1. State table of a decimal counter

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

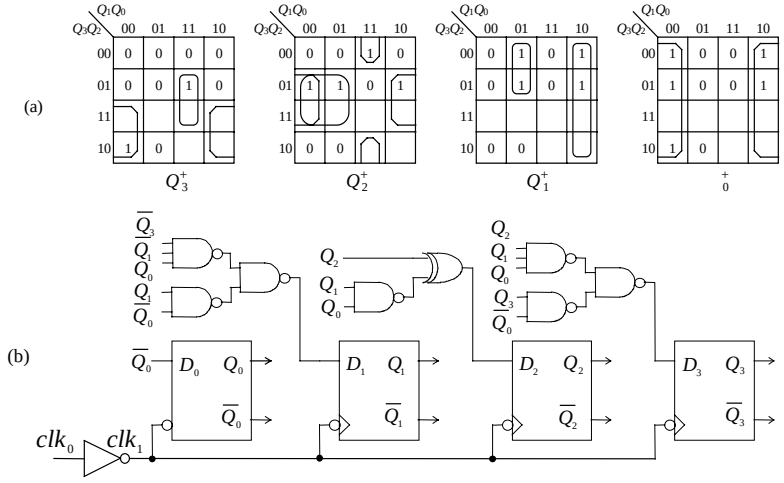

Fig. 3 Synchronous design of a decimal counter
(a) Karnaugh maps of D_3, D_2, D_1 and D_0, (b) circuit realization

If we check the state table in Tab.1 we find that three flip-flops, Q_3, Q_2, Q_1 make transitions only at the odd cycles when Q_0 makes a falling transition $1 \rightarrow 0$. Therefore, if negative edge-triggered flip-flops are adopted, Q_0 can be taken as the clock of other three flip-flops. In addition, we do not care about the values of D_3, D_2, D_1 in those cycles when $Q_0 = 0$. Thus three Karnaugh maps of Q_3, Q_2, Q_1 can be simplified to those shown in Fig.4(a). Three simplified excitation functions of D_3, D_2, D_1 can be derived from Fig.4(a):

$$D_3 = Q_2 \cdot Q_1, \quad D_2 = Q_2 \oplus Q_1, \quad D_1 = \overline{Q}_3 \cdot \overline{Q}_1,$$

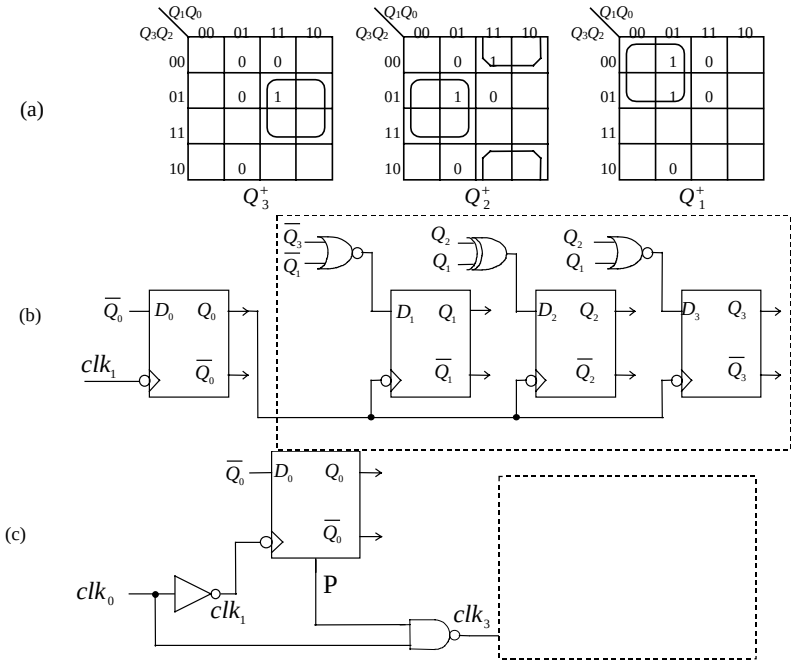

Fig. 4 Design of a decimal counter by using derived clock

(a) Karnaugh Maps of D_3, D_2 and D_1,

(b) circuit realization with an asynchronous clock,

(c) circuit realization with a synchronous clock.

The above functions also can be simply obtained by substituting $Q_0 = 1$ into the original excitation functions of the synchronous design. The corresponding circuit realization is shown in Fig.4(b). This is a traditional asynchronous design for a decimal counter. Obviously the corresponding combinational circuits are simpler. Besides, since three flip-flops Q_3, Q_2, Q_1 have no dynamic power dissipation half of the time when there is no clock triggering, and since the simpler combinational circuits have lower node capacitance, the asynchronous design has power savings. However, those advantage are at the expenses of the skew t_f between clk_1 and the "derived clock" Q_0.

We notice that the flip-flop Q_0 in Tab.1 exhibits a half-frequency divider, and its excitation function is $D_0 = \overline{Q_0}$. According to the discussion in the previous section, we can use the internal node P in flip-flop Q_0 to derive a synchronous clock, clk_3, for other three flip-flops Q_3, Q_2, Q_1, as shown in Fig.4(c). If we consider delay of the inverter and NAND gate being roughly the same, the falling transitions of clk_1 and clk_3 in the circuit will occur simultaneously. This design is synchronous in the sense that all flip-flops are triggered in synchrony with the global clock.

We simulated the new design in Fig.4(c) by SPICE 3f3 with 2μ CMOS technology and following MOS parameters:

nMOS：rsh=0, tox=250×10^{-10}, ld=0.125×10^{-6}, xj=0.175×10^{-6}, cj=1.3×10^{-4}, cjsw=1.5×10^{-10}, uo=600, vto=0.825, cgso=1.8×10^{-10}, cgdo=1.8×10^{-10}, nsub=3.5×10^{15}, theta=0.06, kappa=0.4, eta=0.14, vmax=14.5×10^{4}, pb=0.7, mj=0.5, mjsw=0.3, nfs=1×10^{10};

pMOS：rsh=0, tox=250×10^{-10}, ld=0.35×10^{-6}, xj=0.51×10^{-6}, cj=6.85×10^{-4}, cjsw=4.57×10^{-10}, uo=200, vto=-0.857, cgso=5.1×10^{-10}, cgdo=5.1×10^{-10}, tpg=-1, nsub=6×10^{15}, theta=0.03, kappa=0.4, eta=0.06, vmax=14.5×10^{4}, pb=0.7, mj=0.5, mjsw=0.3, nfs=1×10^{10}.

Simulation proved that the new design has an ideal logic operation. We also measure the power dissipation of two synchronous designs in Fig.3(b) and Fig.4(c).[7] The energy dissipation diagrams are shown in Fig.5, and prove that the new design reduces the power dissipation by 20%.

Fig. 5 Energy dissipation diagram

Design in Fig.4(c) can be modified to allow selective shut-down, as shown in Fig.6, where the control signal C_{shut} can be used to keep the LSB flip-flop Q_0 unchanged. If $C_{shut} = 0$, we have $D_0 = 1$ and $P = 0$, so that the NAND gate used to gate clk_0 is shut off and the other three flip-flops are isolated from the clock transitions. That is, three flip-flops Q_3, Q_2, Q_1 are totally isolated from heating.

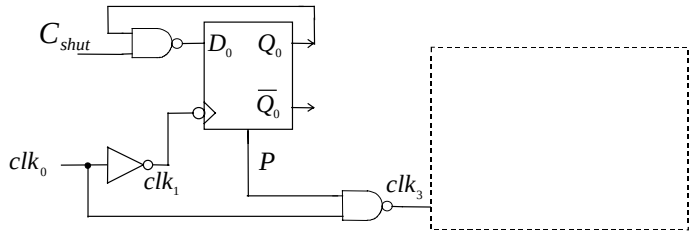

Fig. 6 Control for shutting off the counter

Finally, we should point out that the design proposed above can be used in other counters which have a LSB flip-flop and work as a circuit with half-frequency.

IV. Conclusion

Low power design has become a goal for all VLSI circuits, including custom integrated circuits. Considering that a large system can be partitioned in more functional units, we can try to redesign them to reduce their power dissipation or to shut them off during their idle cycles.

For an important sequential function unit, i.e. counter, this paper proposed a generation circuit of half-frequency synchronous clock from the master clock. The derived clock has no glitch and no skew. Since many even-counters have the common characteristic that the LSB flip-flop is switched at each clock cycle and other flip-flops only change their states with a half-frequency. Thus, by using the technique proposed in this paper the half frequency synchronous clock can be generated by the LSB flip-flop and used as a derived clock to switch the

rest of the flip-flops. Circuit simulations show that the derived clock with half-frequency in this paper has the expected quality and the designed decimal counter has lower power dissipation in comparison with the traditional design. This technique has practical value in the present IC design since in many sequential circuits we always can find a flip-flop, such as the LSB flip-flop in common decimal counter, works as a half-frequency divider.

In fact, the control signal does not need to be a half-frequency feedback signal. We can use various signals to gate the clock and derive a synchronous clock. Based on this scheme, the activity-derived clock design for low power circuits in Ref.[3] can be realized.

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