Interconnect Energy Dissipation in High-Speed ULSI Circuits

Payam Heydari
Department of Electrical and Computer Engineering
University of California
Irvine, CA 92697

Massoud Pedram and Soroush Abbaspour
Department of Electrical Engineering-Systems
University of Southern California
Los Angeles, CA 90089

Abstract - *In this paper, new formulations for the energy dissipation of lossy transmission lines driven by CMOS inverters are provided, and a new performance metric for the energy optimization under the delay constraint is proposed. The energy formulations are obtained by using approximated expressions for the driving-point impedance of lossy coupled transmission lines which itself is derived by solving Telegrapher's equations. The effect of electromagnetic (inductive and capacitive) couplings on the energy dissipation is accounted for in the derivations.A comprehensive analysis of energy is performed for a wide variety range of the gate aspect-ratios of the driving transistors. To accomplish this task, two stable circuits that are capable of modeling the transmission line for a broad range of frequencies are synthesized. Experimental results show that the energy calculated using these equivalent circuits are almost equal to the one calculated by solving the more complicated transmission line equations directly. Next, using a new performance metric the effect of geometrical variations of the interconnect and the driver on the energy optimization under the delay constraint is studied. The experimental results verify the accuracy of our models.*

1. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) predicts that by 2010 over one billion transistors will be integrated into a single monolithic die [1]. The wiring system of this one-billion transistor die will deliver signal and power to each transistor on the chip, provide low-skew and low-jitter clock to latches, flip-flops and dynamic circuits, and also distribute data and control signals throughout the

chip [2]. Providing the required global connectivity throughout the whole chip demands long on-chip wires. These global wires should deliver high frequency signals (presently at around 1-2GHz) to various circuits. This implies that the global wires exhibit transmission line effects including electromagnetic coupling. On the other hand, as technology sizes continue to decrease, many new effects are being observed due to the use of nanometer technologies. Some significant deep sub-quarter-micron effects are caused by increasing cross-coupling capacitance and coupling inductance. So far, the well-known $(1/2)CV^2$ model has been used as an interconnect energy model, where C includes the capacitance of the interconnect as well as the capacitances of driving and driven circuitries, and V is the voltage swing. This model, however, fails to predict the interconnect energy dissipation in the current range of clock frequencies, where the signal transients do not settle to a steady state value due to the small clock cycle-time. Moreover, this model does not consider coupling noise being imposed by neighboring wires as well as other transmission line properties. As we will see in this paper, these effects must be taken into account for in the energy calculations, that will otherwise lead to erroneous results. An analytical interconnect energy model with consideration of event coupling has been proposed in [3]. The authors used nodal equations for a system of inteconnects to obtain the state vector of the system. The state vectors were utilized in the interconnect energy dissipation expression. This approach does not capture the transmission line effects. It also assumes that the system reaches the steady-state. In [4], authors showed that using distributed RC circuits do not capture all behaviors of lossy transmission lines that can be captured otherwise using the transmission line equations. Taylor *et al.* proposed a deep sub-micron (DSM) aware power estimation methodology using a three-wire lookup table [5]. The dissipated energy of each individual interconnect is computed considering capacitive coupling effects of the immediate adjacent wires. Using a detailed SPICE simulation of all possible types of transitions on a group of three adjacent wires, a three-wire lookup table was created. To obtain the total energy dissipation, the sum of energy dissipations of each individual interconnect was computed [5]. [5], however, does not consider the transient behavior of the interconnect in the energy calculations.

In this paper, accurate expressions for the energy dissipation of coupled interconnects are obtained while addressing two important problems simultaneously. The first problem is to analyze the transmission line effects on the energy dissipations. The second problem is to consider the effect of electromagnetic coupling on the interconnect energy dissipation.

Section 2 presents two circuit model for the lossy transmission line; a new RLC circuit configuration called RLC-π circuit, and an RLC circuit. In section 3, the RLC-π and the RLC circuits are utilized to derive the total energy dissipation of a transmission line driven by a CMOS inverter for large W/L's and small W/L's of the driving transistors, respectively. Then a new metric is utilized that is very relevant for

the energy optimization under the delay constraint. Simulations and experimental results provided throughout this section confirms the accuracy of our model and the usefulness of our metric. Finally, section 4 presents the conclusions of our paper.

2. ENERGY DISSIPATION OF PASSIVE RLC CIRCUITS

One common way of studying the parasitic effects of an on-chip interconnect on the performance of a VLSI circuit is to model it by a large number of cascaded ladder RLC circuits. Therefore a relevant starting point for studying the energy dissipation of on-chip interconnects is to investigate the energy dissipation of a passive RLC circuit, demonstrated in Fig. 1, that is excited by a unit step voltage. Depending on the relative values of the circuit elements, this circuit exhibits either of the two possible transient responses as also depicted in Fig. 1.

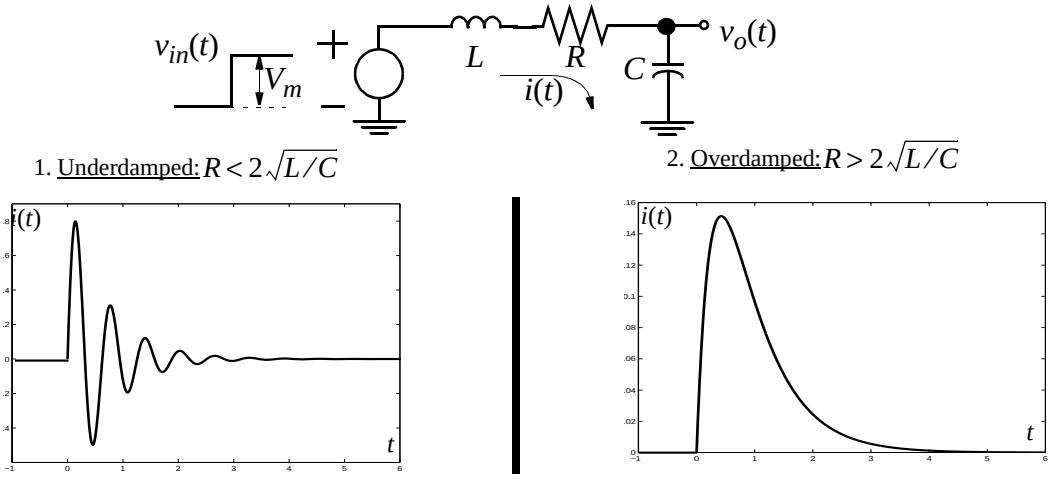

Fig. 1. An RLC circuit excited by a unit step voltage. Current waveforms are shown for both the underdamped and the overdamped cases.

The total energy delivered by the input source to the passive circuit is as follows:

$$E_{tot} = \int_{-\infty}^{\infty} v_{in}(t)\, i(t)\, dt \tag{1}$$

In the next two sub-sections we obtain the total as well as the dissipated energy for both underdamped and overdamped RLC circuits.

2.a. Energy dissipation of an underdamped RLC circuit

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. This transient behavior occurs when $R < 2\sqrt{L/C}$. In terms of energy, the stored energy in the capacitor and/or in the inductor is being transferred back and forth between reactive elements. If the circuit

is lossless ($R = 0$), this energy transfer will be performed endlessly. However with a resistor present in the circuit, a portion of the energy is dissipated in the resistor. To obtain the energy dissipated by the circuit, we first obtain the total energy generated by the input source.

$$E_{u,\,tot} = \int_0^\infty V_m\, i_u(t)\, dt \tag{2}$$

where $i_u(t)$ is the current flowing through the underdamped circuit. This current is easily obtained by solving the characteristic differential equation of the RLC circuit.

$$i_u(t) = \left(\frac{V_m}{L}\right)\frac{1}{\omega_{d_0}} e^{-\alpha_0 t} \sin \omega_{d_0} t \tag{3}$$

where α, the damping constant, is $\alpha_0 = R/2L$, ω_{n0}, the resonant frequency, is $\omega_{n_0}^2 = 1/LC$, and ω_{d0}, the oscillation frequency, is equal to $\omega_{d_0} = \sqrt{\omega_{n_0}^2 - \alpha_0^2}$. Replacing $i_u(t)$ in Eq. (2) with its equivalent expression given in Eq. (3) and computing the resulting integral leads to the following equation:

$$E_{u,\,tot} = \int_0^\infty V_m \left(\frac{V_m}{L}\right)\frac{1}{\omega_{d_0}} e^{-\alpha_0 t} \sin \omega_{d_0} t \; dt = \frac{V_m^2}{L\omega_{n_0}^2} = CV_m^2 \tag{4}$$

For the passive RLC circuit excited by a unit-step function, the magnetic energy across the inductor is transferred to the electric energy across the capacitor in the steady-state. Therefore, the total stored energy in reactive elements is $(1/2)CV_m^2$. Consequently, the energy dissipated in a passive underdamped RLC circuit is as follows:

$$E_{u,\,dissipated} = E_{u,\,tot} - \frac{1}{2}CV_m^2 = \frac{1}{2}CV_m^2 \tag{5}$$

From Eq. (5) it is concluded that the energy dissipated in any passive underdamped RLC circuit that is driven by a unit-step function is simply $(1/2)CV_m^2$.

Now let us assume that the input source to the RLC circuit is a periodic rectangular waveform, which is almost the case in digital integrated circuits. The total energy delivered by the input source during a low-to-high transition of the input source is as follows:

$$E_{u,\,tot}^{RLC} = CV_m^2\left[1 - \left(\frac{\omega_{n_0}}{\omega_{d_0}}\right) e^{-\frac{\alpha_0 T}{2}} \sin\left(\frac{\omega_{d_0} T}{2} + \Phi_0\right)\right] \tag{6}$$

Fig. 2 shows the energy variation as a function of the fundamental period, *T*, for an underdamped RLC circuit excited by a periodic rectangular voltage signal. Please note that for small periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

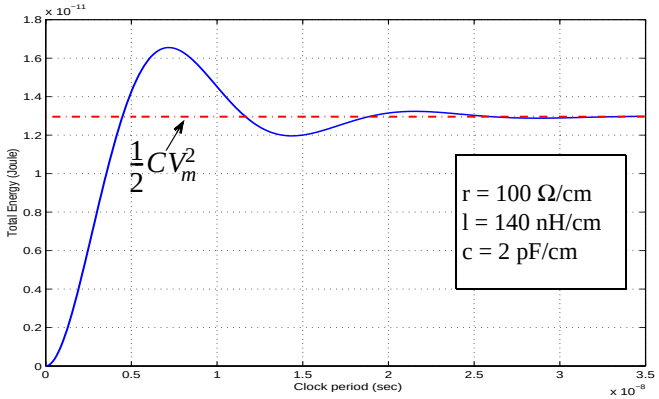

Fig. 2. The total delivered energy vs. the fundamental periods of oscillations for an underdamped RLC circuit

The dissipated energy in the low-high transition of the input source is:

$$E_{u,\,dissipated}^{L\to H} = \int_0^{T/2} R i_u^2(t)\,dt = \frac{1}{2}CV_m^2\left[1-\left(\frac{\omega_{n_0}}{\omega_{d_0}}\right)^2 e^{-\alpha_0 T}\left(1-\cos(\omega_{d_0}\boldsymbol{T}-\Phi_0)\cos(\Phi_0)\right)\right] \tag{7}$$

In equations (6) and (7), $\Phi_0 = \text{atan}(\omega_{d_0}/\alpha_0)$. As *T*, the fundamental period of the input waveform, becomes larger, the second term inside the bracket becomes smaller, and in the limit, the energy expression becomes identical to Eq. (5).

p

2.b. Energy dissipation of an overdamped RLC circuit

In the overdamped case, the resistor is sufficiently large (i.e., $R > 2\sqrt{L/C}$) such that it eliminates the resonances from current and voltage waveforms. The total energy delivered by the input source is the same as Eq. (1), which is rewritten here for convenience.

$$E_{o,\,tot} = \int_0^{\infty} V_m i_o(t)\,dt \tag{8}$$

where $i_o(t)$ is the current flowing through the overdamped circuit. This current is easily obtained by solving the characteristic differential equation of the RLC circuit.

$$i_o(t) = \left(\frac{V_m}{2L}\right)\frac{1}{\alpha_{d0}}e^{-\alpha_0 t}\left(e^{\alpha_{d0}t} - e^{-\alpha_{d0}t}\right) = \left(\frac{V_m}{L}\right)\frac{1}{\alpha_{d0}}e^{-\alpha_0 t}\sinh\alpha_{d0}t \tag{9}$$

where $\alpha_{d0} = \sqrt{\alpha_0^2 - \omega_{n_0}^2}$. The total delivered energy is:

$$E_{o,tot} = \int_0^{\infty} V_m \left(\frac{V_m}{2L}\right) \frac{1}{\alpha_{d_0}} e^{-\alpha_0 t}\left(e^{\alpha_{d0} t} - e^{-\alpha_{d0} t}\right) dt \;= \frac{2V_m^2}{2L\omega_{n_0}^2} = CV_m^2 \tag{10}$$

Similar to the underdamped case, consider a periodic rectangular waveform at the input. The total energy delivered by the input source is:

$$E_{o,tot}^{RLC} = \; V_m^2\left[1 - \left(\frac{\omega_{n_0}}{\alpha_{d_0}}\right) e^{-\frac{\alpha_0 T}{2}} \sinh\left(\frac{\alpha_{d_0} T}{2} + \Psi_0\right)\right] \tag{11}$$

Fig. 3 shows the energy variation in terms of the variation in the fundamental period. The error caused by using the $(1/2)CV^2$ model in the overdamped case is smaller than that in the underdamped case. However, in practice, the underdamped response is occurred more frequently.

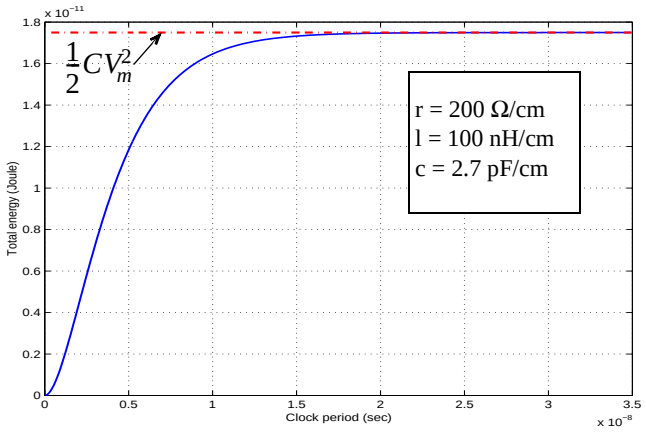

Fig. 3. The total delivered energy vs. the fundamental periods of oscillations for an overdamped RLC circuit

The energy dissipated in the low-high transition of the input source will be as follows:

$$E_{o,dissipated}^{L\to H} = \frac{1}{2}CV_m^2\left[1 + \left(\frac{\omega_{n_0}}{\alpha_{d_0}}\right)^2 e^{=\alpha_0 T}(1 - \cosh(\alpha_{d_0} T + \Psi_0)\cosh(\Psi_0))\right] \tag{12}$$

In equations (11) and (12), $\Psi_0 = \operatorname{atanh}(\alpha_{d_0}/\alpha_0)$. As T becomes larger the energy expression approaches $(1/2)CV_m^2$.

p

2.c. Frequency-domain analysis

From the above analysis some valuable conclusions are drawn. First of all, the energy dissipation of a passive RLC circuit excited by a *unit-step* input is $(1/2)CV_m^2$ irrespective of the circuit conditions (i.e., overdamped or underdamped). From another perspective, the capacitor charges up to the input step voltage, V_m, and in the steady-state is modeled as an open circuit. Therefore, the total stored energy appears as electric field energy across the capacitor ($(1/2)CV_m^2$).

An important task is to find a simple equivalent circuit corresponding to a given RLC circuit that can be directly utilized to obtain the total energy generated by the input source. To find such equivalent circuit, consider the driving-point admittance of RLC circuit of Fig. 1.

$$Y_{in}(s) = \frac{s/L}{s^2 + 2\alpha_0 s + \omega_{n_0}^2} \tag{13}$$

$Y_{in}(s \to 0)$ represents the equivalent DC driving-point admittance of an RLC circuit in the steady-state. This simple observation will be used later during the simplification of the driving-point admittance as well as the derivation of the energy dissipation of a coupled lossy transmission line. Direct calculations reveal that for the RLC circuit given in Fig. 1, $Y_{in}(s \to 0) = Cs$. The steady-state current flowing in the circuit is thus an impulse function, and the total delivered energy by the source is as follows:

$$E_{tot} = \int_0^\infty V_m i(t)dt = \int_0^\infty V_m^2 C\delta(t)dt \quad CV_m^2 \tag{14}$$

As a generalization, consider a circuit consisting of *N* RLC circuits in cascade with a unit step input, as shown in Fig. 4.a. The equivalent circuit for each RLC subsection solely consists of the capacitor of the RLC subsection. As a consequence, the equivalent circuit for the circuit of Fig. 4.a is an all-capacitive circuit shown in Fig. 4.b. The total energy delivered by the source is:

$$E_{tot} = \int_0^\infty V_m i(t)dt = \left(\sum_{k=1}^{N} C_k \right) V_m^2 \tag{15}$$

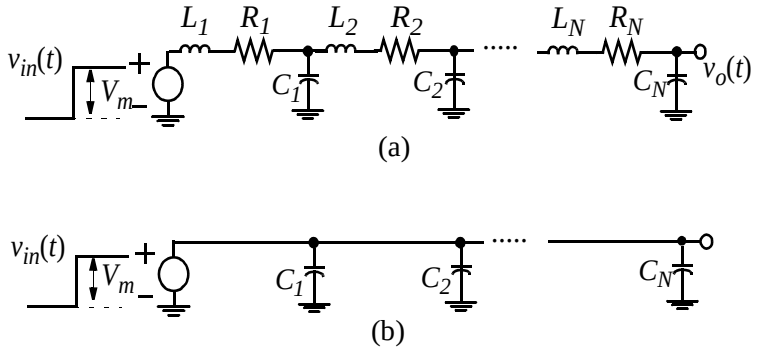

Fig. 4. A ladder of cascaded RLC circuits. (a) the circuit schematic. (b) the equivalent circuit for the energy analysis

The above discussion will be frequently used when we discuss the energy dissipation of coupled lossy lines.

3. ENERGY DISSIPATION OF LOSSY TRANSMISSION LINES

So far, our main attention has been focused on the energy analysis of single passive RLC circuits. There are, however, two major questions that also need to be addressed. In present-day digital and mixed-signal integrated circuits, the global on-chip interconnects must provide the required connectivity and performance for clock rates of 1.0-2.0GHz, which is in a microwave frequency range. This certainly demands a knowledge of electromagnetic-field theory to analyze the on-chip wiring effects. A related question that arises is whether the transmission line effects of on-chip interconnects can have any affect on the energy dissipation. On the other hand, high wiring density and high operating frequencies result in high capacitive and inductive coupling. Consequently, the second question is whether the electromagnetic coupling has any impact on the energy dissipation. This section addresses these questions.

The critical global interconnections, such as clock lines, control lines, and data buses (which can be 32-128 bits wide) between processor and on-chip cache reach more than 100K connections [2]. The propagation delay of signals traveling through these global wires is comparable to the time of flight. In other words, the line length is comparable to the propagated signal wavelength, λ, which is on the order of 0.7-2.2*cm*. This implies that transmission-line properties have to be taken into account. It was shown in [4] that any two uniform parallel conductors, the signal and the return paths, that are used to transmit electromagnetic energy can be considered transmission lines. The return path can be a ground plane, a ground conductor, or a mesh of ground lines on many layers. Solutions to Maxwell's equations for the electric and magnetic fields around conductors are current and voltage waves. The current and voltage wave solutions are a function of the *characteristic impedance*, Z_o, and the *propagation constant*, γ. Consider a single transmission line as shown in Fig. 5. The voltage and current waves in the frequency domain at any point *x* along the line are expressed as a combination of incident and reflected waves.

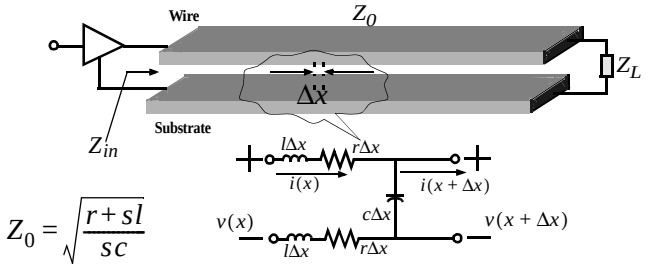

Fig. 5. The schematic of a lossy transmission line along with the circuit representation of a differential length Δx

$$V(x,s) = V_i e^{-\gamma x} + V_r e^{\gamma x} \tag{16}$$

$$I(x,s) = I_i e^{-\gamma x} - I_r e^{\gamma x} \tag{17}$$

where $\gamma = \sqrt{(r + sl)cs}$. The load termination determines how much of the wave is reflected upon arrival at the wire end. The *reflection coefficient*, Γ_L , determines the amount of the incident wave that is reflected back to the line as a result of impedance mismatch between the line and the load.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{18}$$

The concept of the reflection coefficient is generalized to define the reflected and incident quantities at any arbitrary point along the line.

$$\Gamma(x) = \frac{V_r(0)e^{\gamma x}}{V_i(0)e^{-\gamma x}} \quad \Gamma_L e^{2\gamma x} \tag{19}$$

The driving point impedance, Z_{in}, is the ratio of the voltage and current waves at the input source end.

$$Z_{in}\Big|_{x=-h} = \frac{V_i e^{\gamma h} + V_r e^{-\gamma h}}{I_i e^{\gamma h} - I_r e^{-\gamma h}} = Z_0\left(\frac{1 + \Gamma_L e^{-2\gamma h}}{1 - \Gamma_L e^{-2\gamma h}}\right) = Z_0 \frac{Z_L + Z_0 \tanh(\gamma h)}{Z_0 + Z_L \tanh(\gamma h)} \tag{20}$$

where h is the line length. In the above equation, the load impedance, Z_L, is normally a capacitive load in ULSI circuits, since the interconnect normally drives a CMOS circuit whose input impedance is purely capacitive.

To account for the electromagnetic coupling effects on the interconnect energy dissipation, the total line inductance and capacitance per unit length are modified accordingly. The effect of capacitive coupling is predicted by considering the switching transients of the immediate neighboring wires. The effect of nonadjacent lines are ignored because the capacitive coupling exhibits a near-field effect, and the adjacent aggressive lines behave as shield lines for non-adjacent wires. On the contrary, the inductive coupling exhibits a far-field effect. The non-adjacent lines have a considerable amount of inductive couplings on the victim line. This makes the analysis of inductive coupling particularly difficult. In addition, the current return paths cannot be easily configured in the circuit [4]. This causes the problem of inductive coupling to become even more complicated.

The effect of capacitive coupling is taken into account by using the Miller theorem as also shown in Fig. 6. The Miller capacitance per unit length seen across the input port of the transmission line 1 as a result of switching in line 2 is:

$$c_{c,M} = c_c\left(1 - \frac{V_2(-h, s)}{V_1(-h, s)}\right) \tag{21}$$

The voltage waves V_2 and V_1 are obtained by combining their incident and reflected wave components at their corresponding input ports, similar to Eq. (16). To verify the accuracy of Eq. (21), the two transmission lines in Fig. 6 are simulated using star-HSPICE.

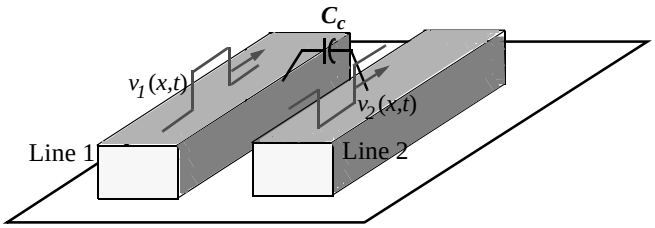

Fig. 6. Two capacitively coupled transmission lines. The traveling voltage waves are 180◦ out of phase.

Input sources are 180° out of phase as depicted in Fig. 6. Fig. 7.a shows current and voltage waveforms of line 1. Line 1 is then decoupled from line 2 by replacing cross-coupling capacitance c_c with its Miller capacitance $c_{c,M}$ from line 1 to ground-plane, and then simulate this new circuit with HSPICE again. The voltage and current waveforms are depicted in Fig. 7.b. Comparing voltage and current waveforms in Fig. 7.a with those in Fig. 7.b verifies the accuracy of Eq. (21).

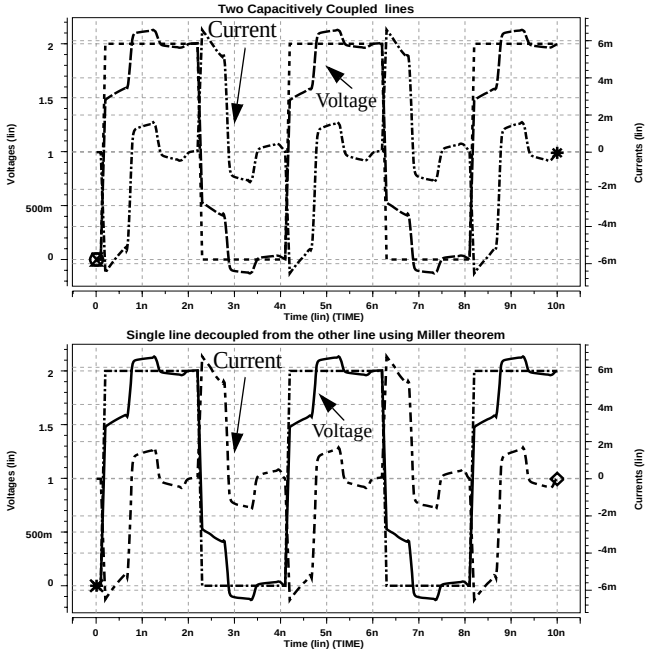

Fig. 7. The source voltage as well as driving-point current and voltage waveforms in a lossy coupled transmission line. (a) results obtained using HSPICE simulation on the coupled line. (b) results obtained using HSPICE on the decoupled line after applying Miller theorem

The inductive couplings between transmission lines are accounted for by an algebraic summation of each line's self inductance and all mutual inductances between that line and other lines considering also the current direction flowing through the lines. For example in a set of N coupled transmission lines, the total per unit length inductance of the *j*-th line that is magnetically coupled to other lines is:

$$l_{int,tot_j} = l_{int_j} + \sum_{i \neq j} (\pm M_{ij}) \tag{22}$$

After characterizing the capacitive and inductive couplings, the next step is to obtain a relevant rational expression for the driving-point impedance of a coupled transmission line. According to Eq. (20), the input impedance of a transmission line is a nonlinear function of frequency. Direct substitution of this nonlinear expression into the energy equation does not yield a closed-form expression for the energy dissipation of the lossy transmission line. Still it is possible to simplify Eq. (20), using some observations, and obtain an accurate expression for the energy dissipation.

Observation 1. If the abrupt transitions of the input waveform are sufficiently far away in time so as to allow the circuit to come very close to its steady-state response, then the total energy delivered by the input source is obtained using the driving-point impedance of the circuit evaluated at low frequencies.

This observation is utilized here to simplify Eq. (20). We evaluate *tanh*(.) at low frequencies by expanding its Taylor expansion around $s = 0$ and truncating higher order terms. Depending upon the order of the truncation, two stable equivalent circuits are extracted.

A. First-order truncation

The first-order Taylor expansion of $\tanh(\gamma h)$ is γh. This leads to the following approximated rational function:

$$Z_{in}\big|_{x=-h} = \frac{1}{C_L s}\left[\frac{1+\left(\gamma^2 h^2 \dfrac{C_L}{C_{int,tot}}\right)}{1+\dfrac{C_{int,tot}}{C_L}}\right] \tag{23}$$

where $C_{int,tot}$ is the total interconnect capacitance including the Miller capacitance of the neighboring lines that are capacitively coupled to the line, and the interconnect-to-substrate capacitance. Using Eq. (22) a series RLC circuit is synthesized as depicted in Fig. 8, where R_{eq} and L_{eq} are defined as follows:

$$R_{eq} = \frac{C_L}{C_L + C_{int,tot}} R_{int} \quad , \quad L_{eq} = \frac{C_L}{C_L + C_{int,tot}} L_{int,tot} \tag{24}$$

R_{int} is the line resistance. $L_{int,tot}$ is the total inductance of the lossy line including the self and mutual inductances and is obtained by Eq. 22. The inductive couplings between transmission lines are accounted for by an algebraic summation of each line's self inductance and all mutual inductances between that line and other lines considering also the current direction flowing through the lines.

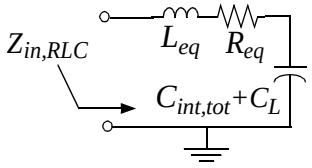

Fig. 8. The circuit realization of Eq. (23)

B. Second-order truncation

The second-order truncation of the Taylor series expansion of $\tanh(\gamma h)$ is:

$$\tanh(\gamma h) = \frac{\sinh(\gamma h)}{\cosh(\gamma h)} \rightarrow \frac{2\gamma h}{2+\gamma^2 h^2} \quad , \textit{ for small values of } |s| \qquad (25)$$

This leads to the following relationship:

$$Z_{in}\big|_{x=-h} = \frac{1}{C_L s}\left[\frac{2+\gamma^2 h^2 + \left(2\gamma^2 h^2 \frac{C_L}{C_{int,tot}}\right)}{2+\gamma^2 h^2 + \left(2\frac{C_{int,tot}}{C_L}\right)}\right] \qquad (26)$$

To find out how accurately Eq. (23) follows the actual driving-point impedance of a lossy line given by Eq. (20), we utilize the per unit length parameters of the top-level metal layer in 0.11µm CMOS technology that are directly calculated from interconnect parameters provided by ITRS'2001 [1]. A comparison is made between magnitude response of the driving-point impedance given by Eq. (20) and the magnitude response of the expression in Eq. (23) for four different lengths. Fig. 8 shows such a comparison in a logarithmic scale. Obviously, the approximation is accurate in a broad range of frequencies. For longer lengths of the line the discrepancy begins to appear at lower frequencies.

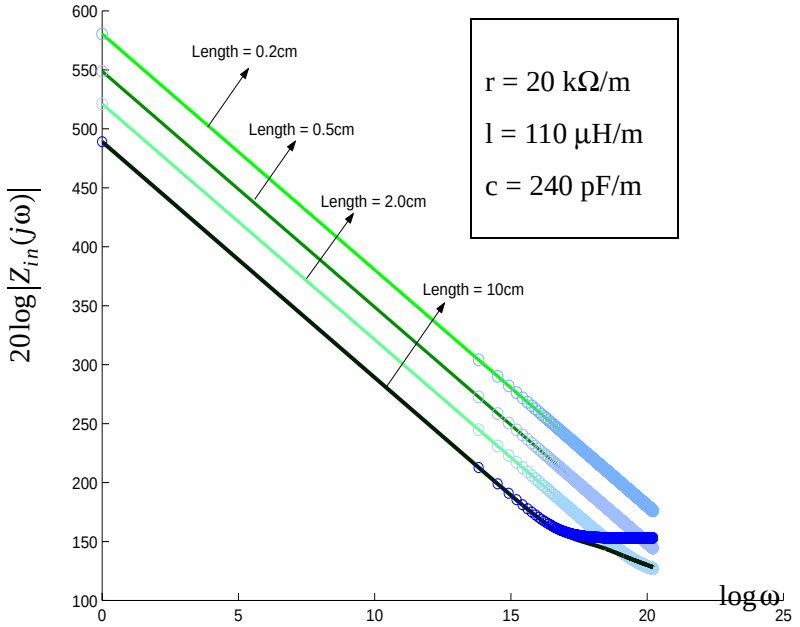

Fig. 8. A comparison between the magnitude response of line's actual driving-point impedance (Eq. (20)) and that of line's approximated rational impedance function (Eq. (26)) for four different line lengths

It would be instructive if one could propose a stable circuit realization whose impedance is expressed by Eq. (26). For a lossy transmission line whose driving-point impedance near the DC frequency is expressed by Eq. (26), a stable equivalent circuit realizationcalled RLC-π is synthesized whose topology is demon-

strated in Fig. 9. C_1, C_2, and C_3 are related to actual capacitances of the line and the load through the following relationships:

$$C_3 = \sqrt{\frac{(C_{int,tot} + C_L)^2 + C_L^2}{2}},\ C_2 = \frac{C_{int,tot}}{2} + C_L - C_3,\ \ C_1 = C_{int,tot} + C_L - C_3 \tag{27}$$

The input impedance of the coupled lossy transmission line in Fig. 9 at the low-frequency range is:

$$Z_{in,xline}(s) = \left(\frac{1 + 2C_L / C_{int,tot}}{C_L s}\right)\left(\frac{s^2 + \frac{R_{int}}{L_{int,tot}} s + \frac{2}{L_{int,tot} C_{int,tot}(1 + 2C_L / C_{int,tot})}}{s^2 + \frac{R_{int}}{L_{int,tot}} s + \frac{2(1 + C_{int,tot} / C_L)}{L_{int,tot} C_{int,tot}}}\right) \tag{28}$$

The input impedance of the RLC-π circuit shown in Fig. 9 is:

$$Z_{in,RLC-\pi}(s) = \frac{1}{(C_1 + C_2 \textcircled{S} C_3)s}\left(\frac{s^2 + \frac{R_{int}}{L_{int,tot}} s + \frac{1}{L_{int,tot}(C_2 + C_3)}}{s^2 + \frac{R_{int}}{L_{int,tot}} s + \frac{(C_1 + C_3)/(C_2 + C_3)}{L_{int,tot}(C_1 + C_2 \textcircled{S} C_3)}}\right) \tag{29}$$

where $C_2 \textcircled{S} C_3$ represents the series combination of C_2 and C_3. Equating $Z_{in,xline}(s)$ with the impedance $Z_{in,RLC-\pi}(s)$ of the proposed RLC-π circuit verifies circuit equivalence. Note that C_2 does not introduce any transmission-zero to the transfer function, because C_1-C_2-C_3 make a capacitive loop. This observation is also evident from Eq. (29).

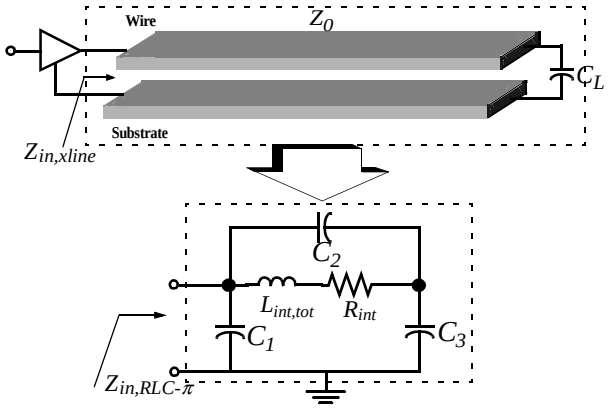

Fig. 9. A lossy transmission line and its equivalent RLC-π circuit representation

Fig. 10 shows the magnitude response of the driving-point admittance of a lossy transmission line which is electromagnetically coupled to a similar line. The line electrical parameters are also indicated in Fig. 10. First, the circuit is simulated using star-HSPICE. In the next step, the magnitude response of the driving-point admittance of the equivalent RLC-π circuit is calculated. According to Fig. 10, this circuit accurately follows the frequency variation the magnitude response of the line admittance at lower frequencies up to

32GHz. Therefore, according to Observation 1, the energy calculation of the lossy transmission line using the RLC-π circuit yield accurate results. Finally the magnitude response of the driving-point admittance of the equivalent RLC circuit is calculated and compared with those of RLC-π equivalent circuit and the lossy coupled line, as is also shown in Fig. 10. The RLC-π circuit models the lossy line more accurately than the RLC circuit over a broader range of frequencies.

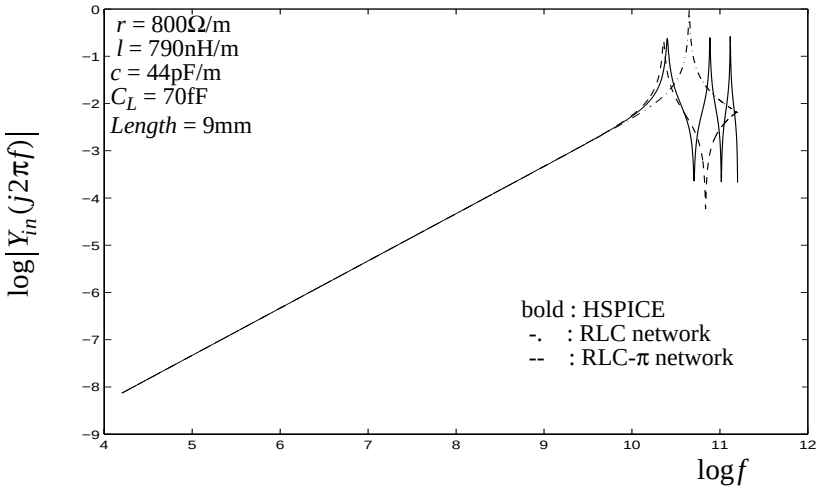

Fig. 10. The magnitude response of the driving-point admittance of an electromagnetically coupled lossy transmission line obtained using HSPICE simulation, and by replacing the line with its equivalent RLC-π circuit, and with its equivalent RLC circuit

Both RLC-π and RLC equivalent circuits synthesized for a lossy coupled transmission line are utilized to compute the interconnect driving-point impedance and the interconnect energy dissipation. A lossy transmission line driven by a large driver is modeled by the RLC-π equivalent circuit, whereas the one driven by a small driver is modeled by the RLC circuit. Using equivalent RLC-π and RLC circuits, section 3 provides a comprehensive analysis of energy dissipation of the lossy transmission lines driven by CMOS inverters.

4. ENERGY DISSIPATION OF LOSSY TRANSMISSION LINES

Consider the circuit shown in Fig. 9. that is composed of an inverter driving a lossy transmission line. The load is CMOS fanout gates are connected to the output port of this lossy transmission line and are represented by their input gate-source capacitances. The electromagnetic coupling effects are treated the same way as discussed in section 3. To encompass a wide range of driver sizes in the energy analysis, two separate analyses are performed. For the large drivers driving lon global wires, the RLC-π circuit is used to model the lossy line (Section 4.1), whereas for the small drivers driving local wires, the RLC model is utilized (Section 4.2). Fig. 11.a shows the variations of the drain-source resistance of a short-channel PMOS transistor in terms of its gate aspect-ratio. Comparing these variations with the magnitude response of a long lossy transmission line in Fig. 4.b sets forth the following criteria:

- If $r_{DS,\,PMOS_{max}} \le \left(\frac{|V_{THp}|}{V_{DD}-|V_{THp}|}\right)|Z_{xline}(j\omega_{clk})|$, then the RLC-π circuit is used. (30)

- If $\left(\frac{|V_{THp}|}{V_{DD}-|V_{THp}|}\right)|Z_{xline}(j\omega_{clk})| < r_{DS,\,PMOS_{max}} \le 2|Z_{xline}(j\omega_{clk})|$, then the RLC circuit is used. (31)

Please note that for $r_{DS,\,PMOS_{max}} > 2|Z_{xline}|$, the inverter is incapable of driving the transmission line, and therefore the voltage swing is insufficient to maintain the correct circuit operation.

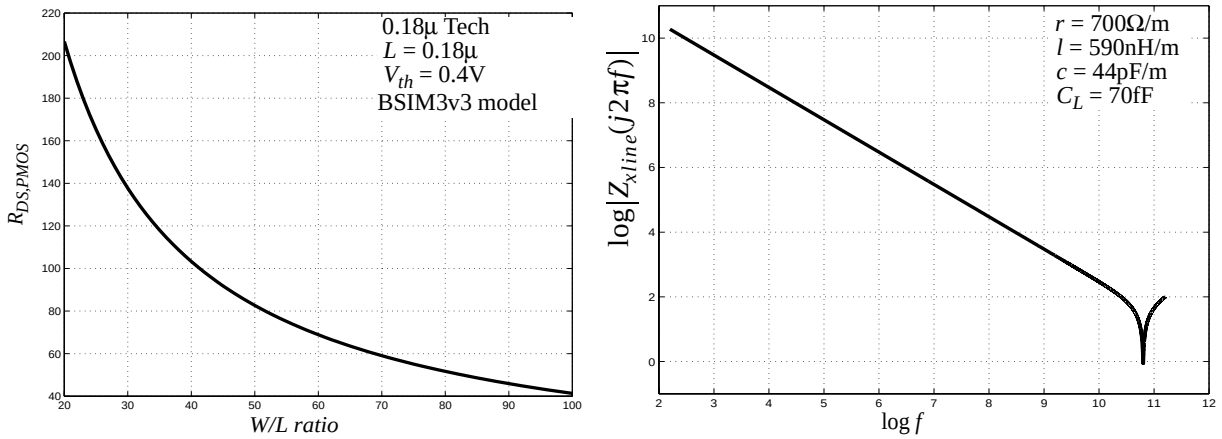

Fig. 11. (a) $r_{DS,PMOS}$ vs. the gate aspect-ratio (b) the magnitude response of the driving-point impedance of a lossy transmission line

Due to the changes in the operation regions of NMOS and PMOS transistors of the line driver during low-to-high and high-to-low transitions of the driver's output, we must distinguish between low-to-high and high-to-low transitions. During the low-to-high transition at the output, the PMOS transistor is conducting and provides a low-impedance conduction path from the supply to the load. During the high-to-low transition at the output the NMOS transistor is in "ON" condition, and no additional energy is transferred out of the power-supply.

We calculate the energy transferred out of the power-supply during a low-to-high transition at the output of the line driver. This energy is the total dissipated energy per clock period of a CMOS gate that drives another CMOS circuit through a lossy coupled transmission line. The energy delivered by the power-supply through the gate in a low-to-high transition of the output is specified by Eq. (32).

$$E_{tot} = \int_{(L \to H)} V_{DD}\, i_{DD}(t)dt \tag{32}$$

where $i_{DD}(t)$ is the current flowing from the power-supply to the load and through the PMOS transistor during the low-to-high transition of the output.The energy dissipation E_{tot} is calculated for a step voltage at the driver input.

The current is obtained using the driving-point admittance of the circuit:

$$I_{DD}(s) = \frac{V_{DD}}{s} Y_i(s) \tag{33}$$

where $Y_i(s)$ is the driving-point admittance seen from the power-supply to the source terminal of the PMOS transistor of the driver. $Y_i(s)$ consists of the admittance of the lossy line (that is modeled either using the RLC circuit or RLC-π circuit) and the PMOS device.

To include the most complete scenario, consider a lossy transmission line that is coupled to other lines through magnetic as well as electric field couplings. Furthermore, suppose that this line is driven by a CMOS inverter. The electromagnetic coupling effects are treated the same way as we discussed earlier in this section 3. Fig. 12 shows the circuit that needs to be analyzed.

4.1. Energy calculation for lossy lines driven by large inverters

Consider a lossy transmission line that is driven by a large inverter. If the condition (7) is satisfied, then the lossy transmission line is modeled by the RLC-π circuit, as indicated in Fig. 12, whose electrical parameters are obtained using Eq. (27). As for the inverter, it is known that the operating regions of the conducting transistors change during the input transition. This change of the operating regions makes the analysis cumbersome. On the other hand, when the line driver has a sufficient current drive capability, the conducting transistors of the driver operate in the linear region for a large portion of the transition time [6]. As a result, we assume that the conducting transistor will be in the linear region for the entire input transition, and is modeled as an ideal switch along with the equivalent capacitance, C_d . C_d is a parallel combination of the diffusion capacitance C_{diff} of PMOS and NMOS devices (Fig. 12). The drain-source resistance is ignored in the case of having large inverters.

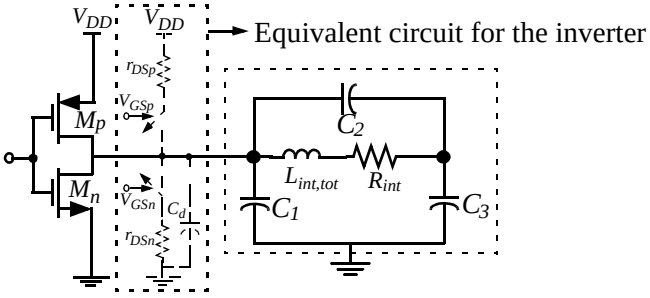

Fig. 12. The equivalent RLC-π circuit model of a lossy coupled transmission line driven by a large CMOS inverter

The π structure of the RLC-π circuit makes the impedance calculations straightforward. For instance, the diffusion capacitances of the driving CMOS circuits are placed directly in parallel with the capacitor C_1 of the RLC-π circuitry and consequently no additional calculation is required. The circuit in Fig. 12 is a

second-order circuit. Therefore, like other second-order circuits, we will distinguish between the overdamped and underdamped responses and analytical models will be derived for both underdamped and overdamped responses.

4.1.1. Underdamped response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. If $R_{int} < 2\sqrt{L_{int,tot}/(C_2 + C_3)}$ then the current and voltage waveforms will oscillate until they reach their steady state value. To obtain the total energy transferred out of the power supply Eq. (32) is used. The input current to the circuit is first obtained by solving the characteristic differential equation of the circuit shown in Fig. 12, which is a damped oscillatory waveform:

$$i_{DD} = (C_d + C_{eq,\pi}) V_{DD} \delta(t) + \frac{V_{DD}}{L_{int,tot}\omega_{d,\pi}} \left(\frac{C_3}{C_2 + C_3}\right)^2 e^{-\alpha_\pi t} \sin \omega_{d,\pi} t \tag{34}$$

where $C_{eq,\pi} = C_1 + C_2 \circledS C_3$ is the equivalent capacitance of the RLC-π circuit. α_π, the damping constant, is $\alpha_\pi = R_{int}/2L_{int}$, $\omega_{p,\pi}$, the resonant frequency, is $\omega_{p,\pi}^2 = 1/(L_{int}(C_2 + C_3))$, and $\omega_{d,\pi}$, the oscillation frequency, is $\omega_{d,\pi}^2 = \omega_{p,\pi}^2 - \alpha_\pi^2$. C_1, C_2, and C_3 are given by Eq. (27). $C_2 \circledS C_3$ represents the series combination of C_2 and C_3.

The total energy delivered by the power-supply is:

$$E_{u,step}^{xline} = (C_d + C_1 + C_3) V_{DD}^2 - \left(\frac{C_3^2}{C_2 + C_3}\right) V_{DD}^2 \left(\frac{\omega_{p,\pi}}{\omega_{d,\pi}}\right) e^{-\frac{\alpha_\pi T}{2}} \sin\left(\frac{\omega_{d,\pi} T}{2} + \Phi_\pi\right) \tag{35}$$

where $\Phi_\pi = \text{atan}(\omega_{d,\pi}/\alpha_\pi)$. Remember that $C_1 + C_3 = C_L + C_{int,tot}$. It is seen that if a CMOS inverter driving a lossy coupled line undergoes an underdamped oscillatory response, and if $R_{int}/L_{int,tot} >> 4\pi f_{clock}$ (or equivalently if $1/(2\pi\sqrt{L_{int,tot}(C_2 + C_3)}) >> 2 f_{clock}$), then the energy expression becomes:

$$E_{u,step}^{xline} = (C_d + C_{int,tot} + C_L) V_{DD}^2 \tag{36}$$

Equations (35) and (36) give the actual and steady-state energy dissipation per clock period, respectively, when the circuit experiences an underdamped oscillatory transient response.

p

4.1.2. Overdamped response

In the overdamped case R_{int} is sufficiently large (i.e., $R_{int} > 2\sqrt{L_{int,tot}/(C_2 + C_3)}$) such that it eliminates the resonances from current and voltage waveforms. Once again, to obtain the total energy transferred out of the power supply using Eq. (32), the input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit, which is an overdamped decaying waveform in this case:

$$i_{DD} = (C_d + C_{eq,\pi})\ {}_{DD}\delta(t) + \frac{V_{DD}}{L_{int,tot}\alpha_{d,\pi}}\left(\frac{C_3}{C_2 + C_3}\right)^2 \frac{1}{\omega_{d,\pi}} e^{-\alpha_\pi t} \sin\omega_{d,\pi}\ t \tag{37}$$

where $\alpha_{d,\pi} = \sqrt{\alpha_\pi^2 - \omega_{p,\pi}^2}$. The total energy delivered by the power-supply for the overdamped transient response is:

$$E_{o,step}^{xline} = (C_d + C_1 + C_3)\ {}_{DD}^{2} - \left(\frac{C_3^2}{C_2 + C_3}\right) V_{DD}^2 \left(\frac{\omega_{p,\pi}}{\alpha_{d,\pi}}\right) e^{-\frac{\alpha_\pi T}{2}} \sinh\left(\frac{\alpha_{d,\pi} T}{2} + \Psi_\pi\ \right) \tag{38}$$

It turns out that if a CMOS inverter driving a lossy coupled line has an overdamped response, and if $\alpha_\pi - \alpha_{d,\pi} >> 4\pi f_{clock}$, then the energy dissipation per each clock period is the same as Eq. (36).

Equations (36) and (38) give the steady-state and the actual energy dissipation per clock period, respectively, when the circuit experiences an overdamped transient response.

p

Remember that the electrical parameters of the lossy transmission line are a function of the geometrical parameters of the line such as wire width, wire thickness and wire length. Similarly, C_d is a function of the MOS gate aspect-ratio. Subsequently, the energy dissipation of a lossy line driven by a CMOS inverter is a function of line and driver physical parameters. Using BSIM3v3 I-V equations for the MOS transistor and accurate closed form expressions derived in [6], the energy is thus expressed in terms of the geometrical parameters of the interconnect and MOS transistors. Fig. 13.a shows the energy variation as a function of the fundamental period, *T,* and under the five different gate aspect-ratios of the driver. Fig. 13.b shows the energy variation with respect to the clock period for the five different values of the metal widths of the interconnect. The input is a periodic rectangular voltage signal. Please note that for small clock periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

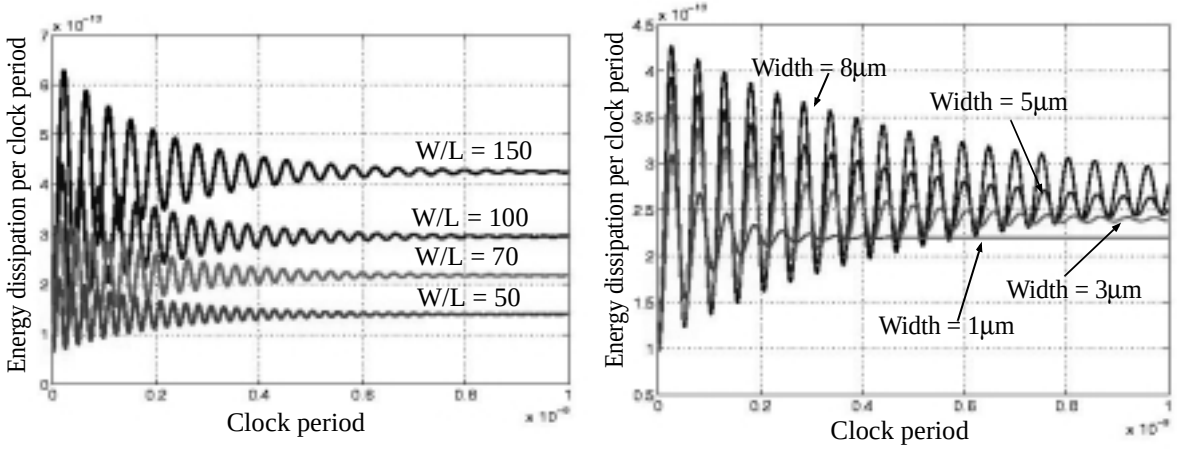

Fig. 13. (a) Energy per clock vs. clock period for six different W/L ratios. (b) Energy per clock vs. clock period for four different interconnect widths (RLC-π).

As the metal width of the interconnect decreases, the variations of dissipated energy per clock period in terms of the clock period gradually changes from a damped oscillatory function to a growing exponential function. Note that due to the large gate aspect-ratios, the overdamped response is rarely observed because the line driver's resistance will be very small and $R_{int} < 2\sqrt{L_{int,tot} / (C_2 + C_3)}$, in practice. The same statement is true when the W/L of transistors decreases. Varying the transistor size and line width will vary the steady-state value of the energy dissipation as being expected. Figures 13.a and 13.b suggest that for a given clock period, we can change the transistor sizes as well as the interconnect metal width such that the dissipated energy per clock period attains its undershoot value which is beneficial from both the speed and energy point of view. This is, however, a difficult task in practice, because process variations cause a deviation from the optimum undershoot value.

To figure out the voltage variations across the load capacitance, the same circuit utilized and is excited by a step input. Figures 14.a and 14.b show the voltage waveform across the load capacitance for different values of interconnect widths and W/L ratios of the transistors of the driver, respectively.

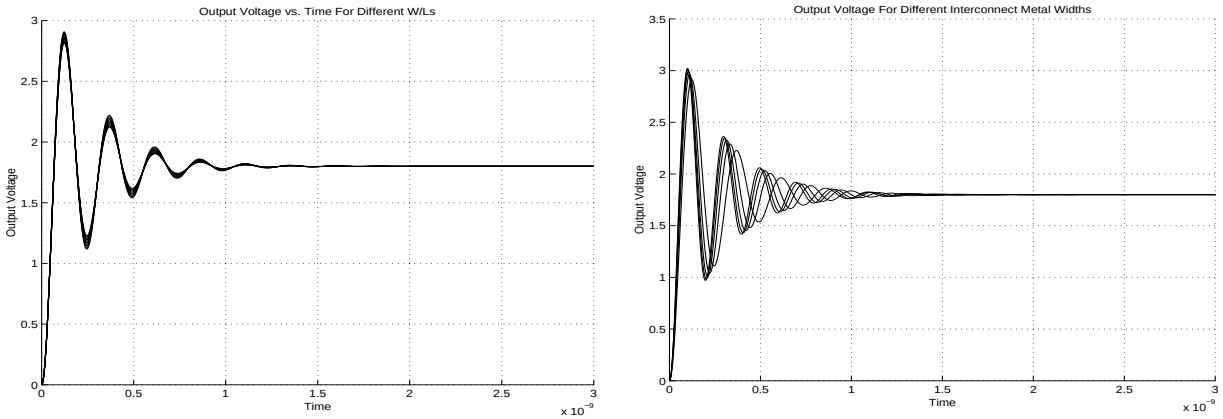

Fig. 14. (a) Voltage waveform for six different W/L ratios (b) Voltage waveform for four different interconnect widths (RLC-π)

Having accurate expressions for the energy dissipation of a lossy transmission line driven by CMOS drivers helps us propose a new design guideline for an area-efficient wire and transistor sizing to achieve the minimum energy under the noise-margin constraint. However, considering the energy dissipation alone is misleading. In other words, performing wire and transistor sizing to achieve the minimum energy may result in unacceptable delay and insufficient voltage swing, and as a result may lead to the logic and the circuit failures.

To take the effect of the circuit delay into account, we propose a new metric. For the overdamped response since all the waveforms are monotonically rising or falling waveforms, the best performance metric is the *energy-50% delay-product*. However, for the underdamped response the delay must incorporate the settling time of the oscillations as well as the percentage of maximum undershoot for noise-margin vio-

lations. To come up with a unique metric for both the underdamped and overdamped responses we use the *energy-50% delay.*(*1+undershoot%*)*-product* (*EDUP*). Fig. 15 shows the *EDUP* per clock cycle of an inverter driving a lossy transmission line with a pure capacitive load termination. Please note that for smaller W/L ratios as long as the condition given in (30) is valid, Fig. 15 can be used to see the energy variation with respect to the transistor size and the interconnect width. The small incremental positive slope of the *EDUP* metric with respect to the W/L is due to the relationship between the energy and the diffusion capacitance of the device.

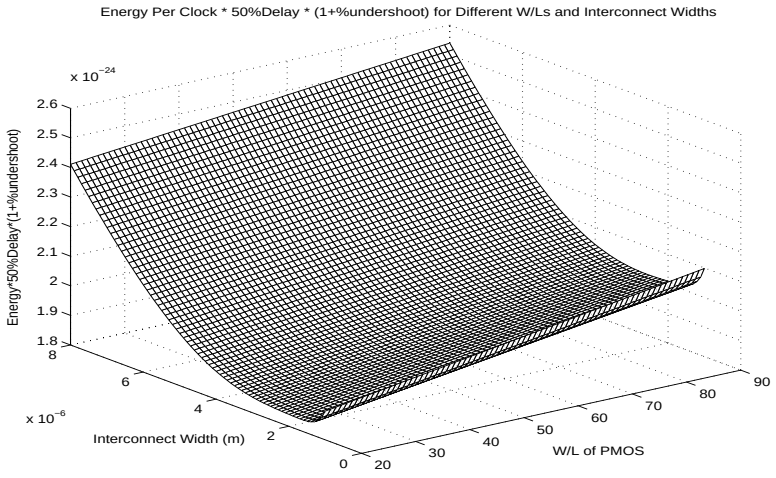

Fig. 15. *EDUP* in terms of W/L and interconnect metal width (RLC-π).

In the energy calculations of interconnects driven by CMOS circuits, it was normally assumed that transients in the current and voltage waveforms have been settled to steady state values and the energy was thus simply equal to $(1/2)CV_m^2$. Section 2.a and 2.b showed that this expression can yield quite an inaccurate result for the dissipated energy of the interconnect in high frequency ULSI circuits. Figures 16 and 17 show that modeling a lossy transmission line with a single RLC circuit do not still provide accurate results for energy dissipation analysis of a lone lossy line driven by a large CMOS inverter in both underdamped and overdamped cases. These figures show the dissipated energy of a single lossy transmission line for various line lengths when the line is modeled by the RLC-π circuit and compare it with that obtained using a single RLC circuit. For small clock cycles, the RLC circuit model is unable to give a good energy estimate. This is true for both overdamped and underdamped circuits. Figures 12 and 13 also reveal that for both underdamped and overdamped circuits when the clock cycle time is sufficiently long, the results obtained by energy calculations in RLC and RLC-π circuits are both closely equal to $(1/2)CV_m^2$.

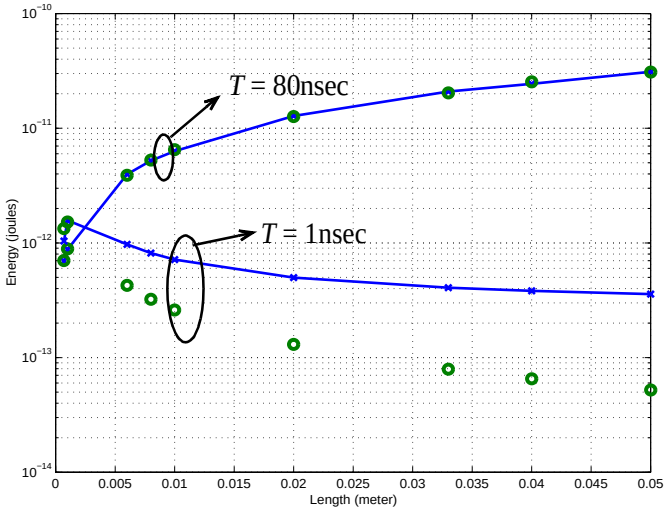

Fig. 16. A comparison between the energy-length variation of the equivalent underdamped RLC-π circuit and that of single underdamped RLC circuit of a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 80nsec

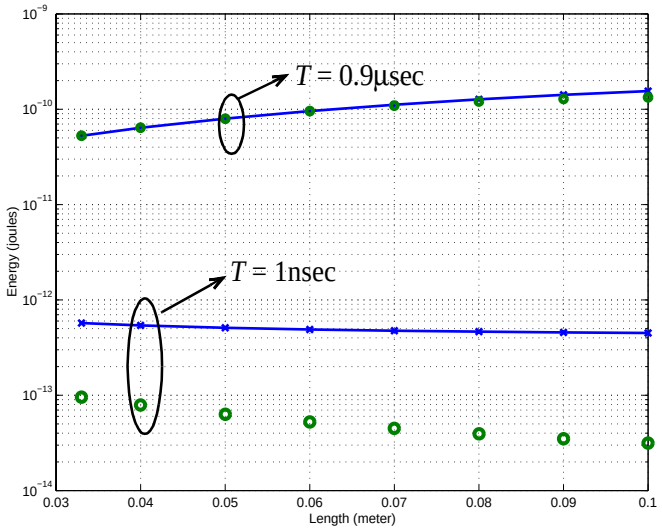

Fig. 17. A comparison between the energy-length variation of the equivalent overdamped RLC-π circuit and that of single overdamped RLC circuit modeling a lossy transmission line. The comparison has been made for two values of cycle time, T = 1nsec and T = 0.9μsec

4.2. Energy calculation for lossy lines driven by small inverters

Now consider a lossy transmission line that is driven by a small inverter. If the condition (31) is satisfied, then the lossy transmission line is modeled by the RLC circuit shown in Fig. 8. Similar to the previous section, we assume that a conducting transistor will be in the linear region for the entire input transition. In the case of small inverters, each transistor is modeled by an ideal switch in series with its drain-to-source resistance, r_{DS}. The MOS resistance thus gets in series with the RLC equivalent circuit, as shown in Fig. 18.

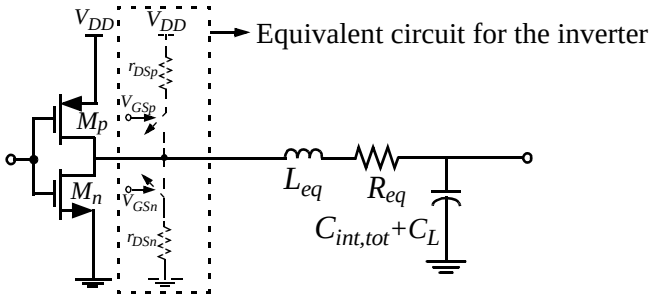

Fig. 18. The equivalent RLC circuit model of a lossy coupled transmission line driven by a small CMOS inverter

The dissipated energy per period of this circuit is calculated for both the underdamped and the over-damped responses.

4.2.1. Underdamped response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. This transient behavior occurs when $(R_{eq}+r_{DS}) < 2\sqrt{L_{eq}/(C_{int,tot}+C_L)}$. Calculating the current flowing out of the power-supply voltage and plugging it in Eq. (32) leads to the following expression for the dissipated energy:

$$E_{u,tot}^{RLC} = (C_{int,tot}+C_L+C_d)V_{DD}^2\left[1-\left(\frac{\omega_p}{\omega_d}\right)e^{-\frac{\alpha T}{2}}\sin\left(\frac{\omega_d T}{2}+\Phi\right)\right] \quad (39)$$

where $\alpha = (R_{eq}+r_{DS})/2L_{eq}$, $\omega_p^2 = 1/L_{eq}(C_{int,tot}+C_L)$, $\omega_d = \sqrt{\omega_p^2-\alpha^2}$, and $\Phi = \text{atan}(\omega_d/\alpha)$. The effect of the diffusion capacitances of the driver is taken into account by simply adding C_d to the first parenthesis of Eq. (39). It is easily observed that the steady-state value of the dissipated energy per period is:

$$E_{u,tot}^{RLC} = (C_{int,tot}+C_L+C_d)V_{DD}^2 \quad (40)$$

p

4.2.2. Overdamped response

In the overdamped case, the resistor is sufficiently large (i.e., $(R_{eq}+r_{DS}) > 2\sqrt{L_{eq}/(C_{int,tot}+C_L)}$) such that it eliminates the resonances from current and voltage waveforms. The total energy delivered by the input source is:

$$E_{o,tot}^{RLC} = (C_{int,tot}+C_L+C_d)V_{DD}^2\left[1-\left(\frac{\omega_n}{\omega_d}\right)e^{-\frac{\alpha T}{2}}\sin\left(\frac{\omega_d T}{2}+\Phi\right)\right] \quad (41)$$

where $\Psi = \text{atanh}(\alpha_d/\alpha)$. Similar to the underdamped response, C_d is added to the first parenthesis of Eq. (41). Once again the steady-state value of the dissipated energy per period is the same as Eq. (40).

p

Once again, using BSIM3v3 I-V equations for the MOS transistor and accurate closed form expressions derived in [6], the energy variation in terms of the geometrical parameters of the interconnect and MOS transistors are obtained. Fig. 19.a shows the energy variations as a function of the fundamental period, *T*, and under the five different gate aspect-ratios of the driver for the equivalent RLC circuit. Fig. 19.b shows the energy variation with respect to the clock period for the five different values of the metal widths of the interconnect. The input is a periodic rectangular voltage signal. Please note that for small periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

Figures 20.a and 20.b show the voltage waveform across the load capacitance for different values of interconnect widths and W/L ratios of the transistors of the driver, respectively.

Like the previous section, considering the energy dissipation alone to propose new design guidelines is misleading. To take the effect of the circuit delay into account, we propose a new metric, *the energy-50% delay.*(*1+undershoot%*)*-product* (*EDUP*). Fig. 21 shows the variation of the *EDUP* in terms of the interconnect width and PMOS W/L ratio. The *EDUP* is an increasing function of the W/L ratio for larger values of the W/L. For large values of W/L ratios, as long as the condition given in (31) is satisfied the formulations of this section and the plot in Fig. 31 is valid. For larger values of W/L ratios, the RLC-π circuit must be used and therefore Fig. 15 must be utilized.

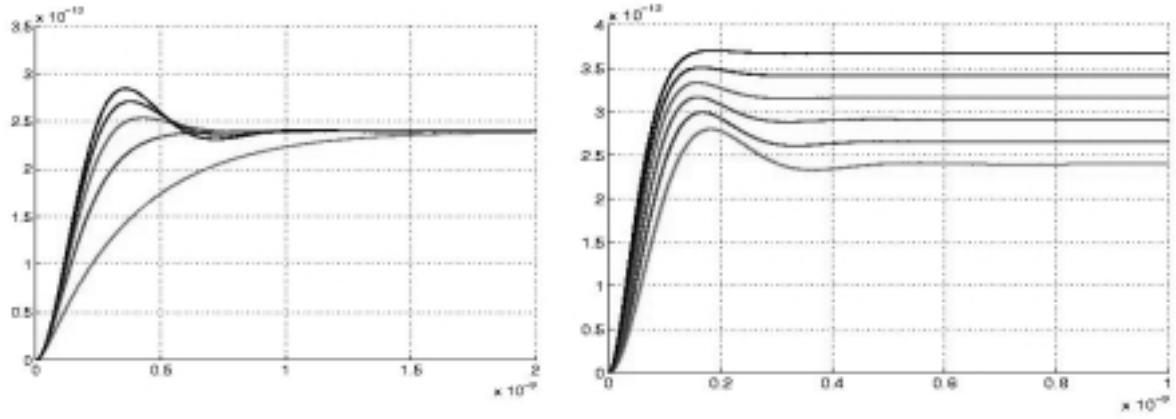

Fig. 19. (a) Energy per clock vs. clock period for five different W/L ratios (b) Energy per clock vs. clock period for six different interconnect widths (RLC)

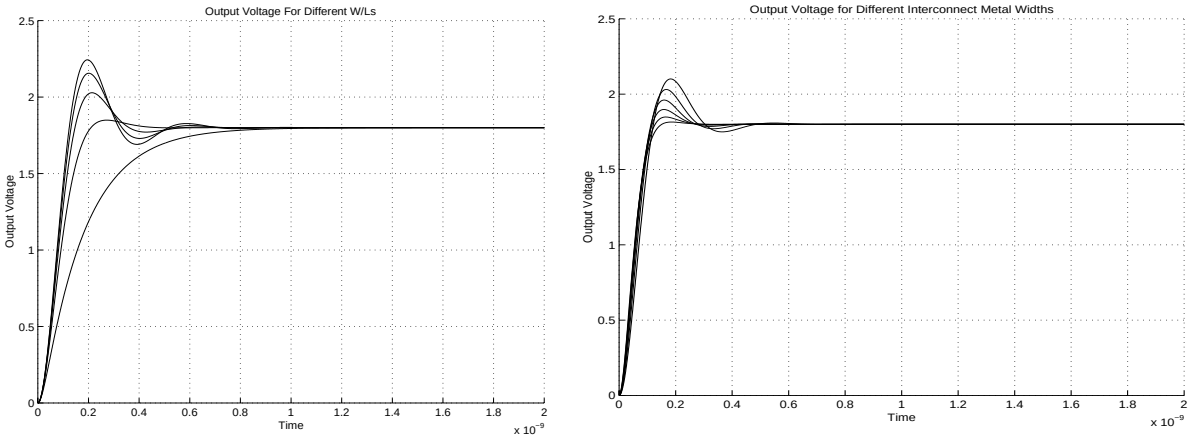

Fig. 20. (a) Voltage waveform for five different W/L ratios (b) Voltage waveform for four different interconnect widths (RLC)

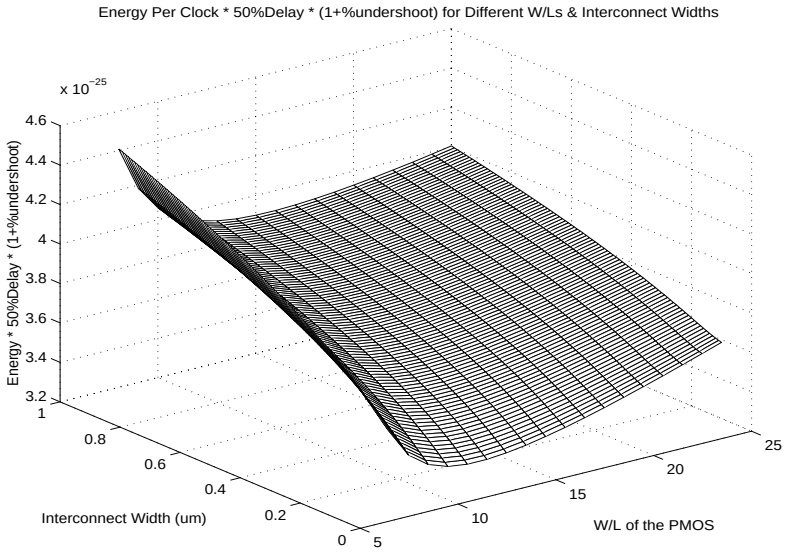

Fig. 21. *EDUP* in terms of W/L and interconnect metal width (RLC)

5. CONCLUSION AND FUTURE WORKS

This paper presented accurate closed-form expressions for the interconnect energy dissipation in high-speed ULSI circuits. The energy was calculated using an approximate expression for the driving-point impedance of a lossy transmission line. The effect of electromagnetic (inductive and capacitive) couplings on the energy dissipation was also accounted for in the derivations. We synthesize a new stable circuit that is capable of modeling the transmission line for a broad range of frequencies. Several experimental results

show that the energy calculated using this circuit is almost equal to the one calculated by directly solving the complicated transmission line equations.

This paper showed that the actual energy dissipation can be quite different from the value predicted by the steady-state $(1/2)CV^2$ model. Using this notion, we will define a new metric that enables us to design interconnects in such a way as to optimize the energy dissipation subject to a given noise margin.

6. REFERENCES

[1] Semiconductor Industry Associations, International Technology Roadmap for Semiconductors: 2000, http://public.itrs.net/Files/2000UpdateFinal/2kUdFinal.htm.

[2] J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proceedings of the IEEE, Special Issue on Limits of Semiconductor Technology,* Vol. 89, No. 3, pp. 305- 324, March 2001.

[3] T. Uchino, J. Cong, "An Interconnect Energy Model Considering Coupling Effects," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 555-558, Las Vegas, June 2001.

[4] A. Deutsch, P. W. Coteus, G. Kopcsay, H. Smith, C. W. Surovic, B. Krauter, D. Edelstein, P. Restle, "On-chip Wiring Design Challenges for Gigahertz Operation," *Proceedings of the IEEE*, Vol. 89, No. 4, pp. 529- 555, April 2001.

[5] C. N. Taylor, S. Dey, Y. Zhao, "Modeling and Minimization of Interconnect Energy Dissipation in Nanometer Technologies," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 754-757, Las Vegas, June 2001.

[6] S.-M. Kang, Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, pp. 196-204, McGraw-Hill Companies, Inc., 1999.