Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend

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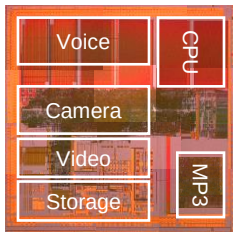
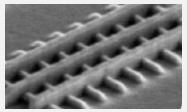
Chip and System Integration Trends for Better PPA & System Performance

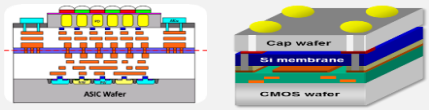
Multiple Chips on PCB



SoC



3D Transistors
(FinFET, GAA-NWT)



3D Stacking
(BSI, Monolithic MEMS)

3D Packaging
(WLP, WoW)

- **Better performance**
- **Better Power**
- **Better form factor**

Platform Solutions

Mobile

High Performance Computing

Automotive

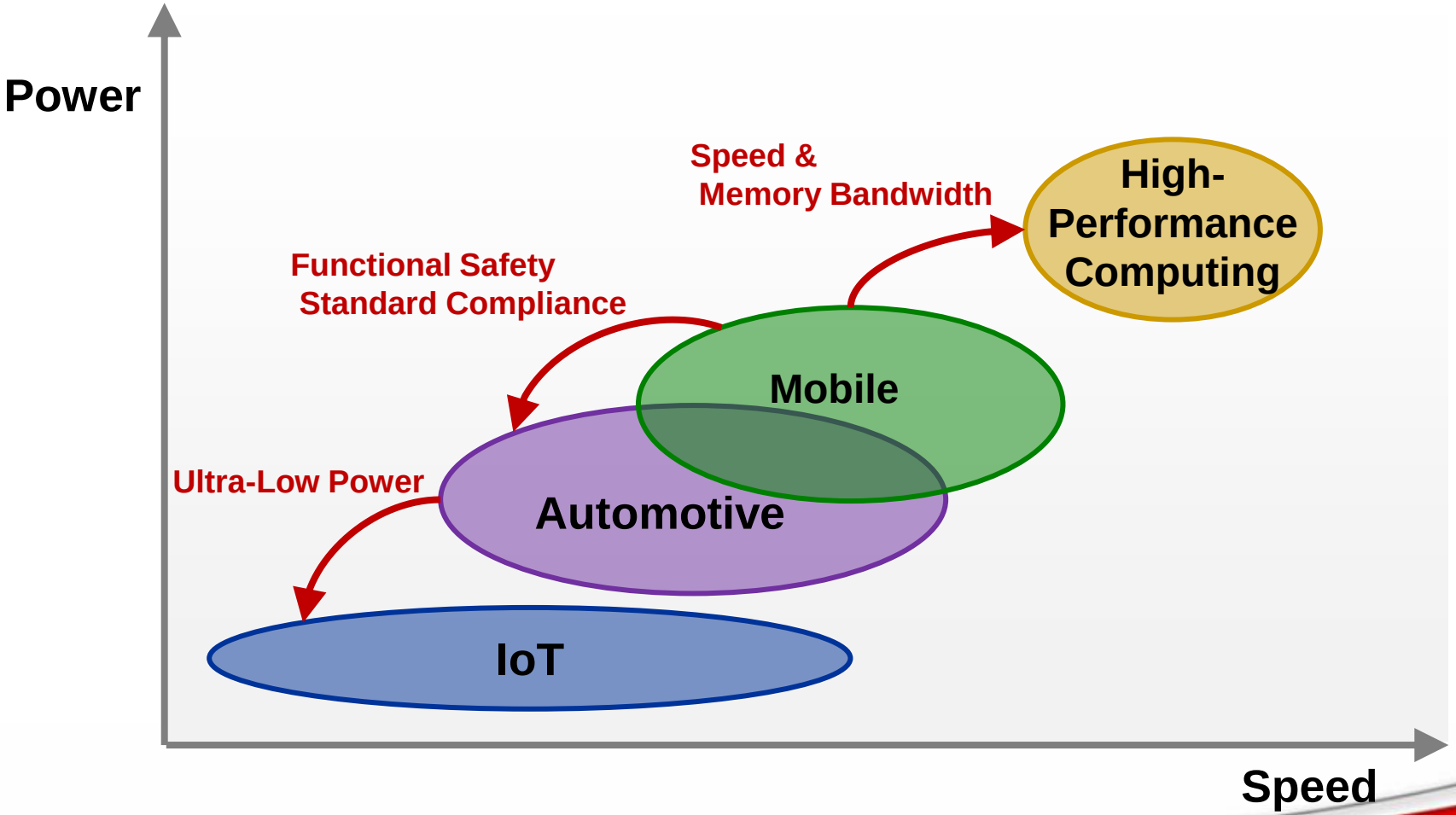
IoT

SYSTEM INTEGRATION

- **System performance/ Bandwidth**
- **Application-specific**
- **Process technology + Design Solutions**

2D **3D**

Application-Optimized Design Platforms Area, Performance and Power



Semiconductor Trend

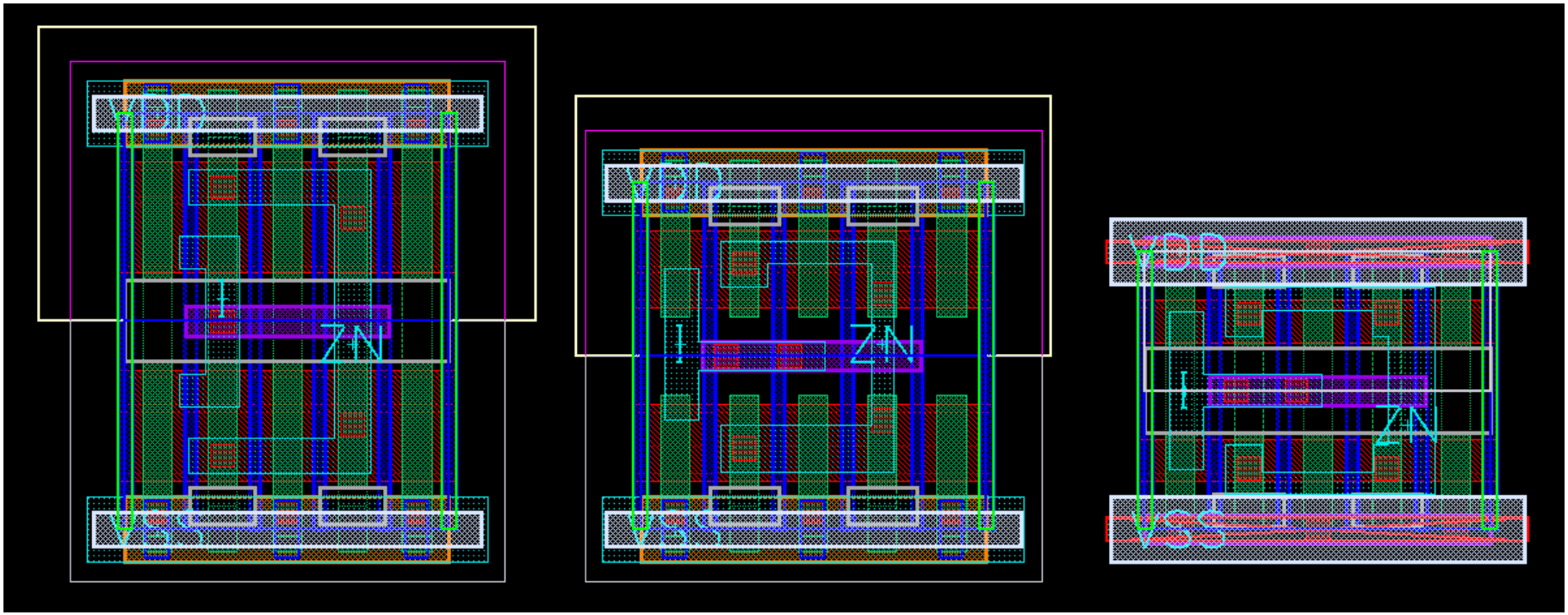
- Area: process primary dimension scaling slows down
  - Very challenging to continue Moore's law economically
  - Process and design co-optimization to provide enough area scaling
- Performance: dimension scaling grows metal and via resistance exponentially
  - Fully automatic and smart via pillar design flow to reduce high resistance impact
- Power: ultra low voltage for ultra low power
  - Robust design and variation modeling at low voltages
- Heterogeneous integration
  - Low cost and high system performance 3D packaging
- High physical design complexity
  - Machine learning to be applied to physical design

Area Scaling

- Process primary dimension (metal, gate and fin pitch) scales less and per generation cadence takes longer
- Process-design co-optimization innovation to keep area scaling
  - Fin depopulation to increase cell density
  - Power plan and cell layout co-optimization to increase cell placement utilization
  - EUV to increase routing density

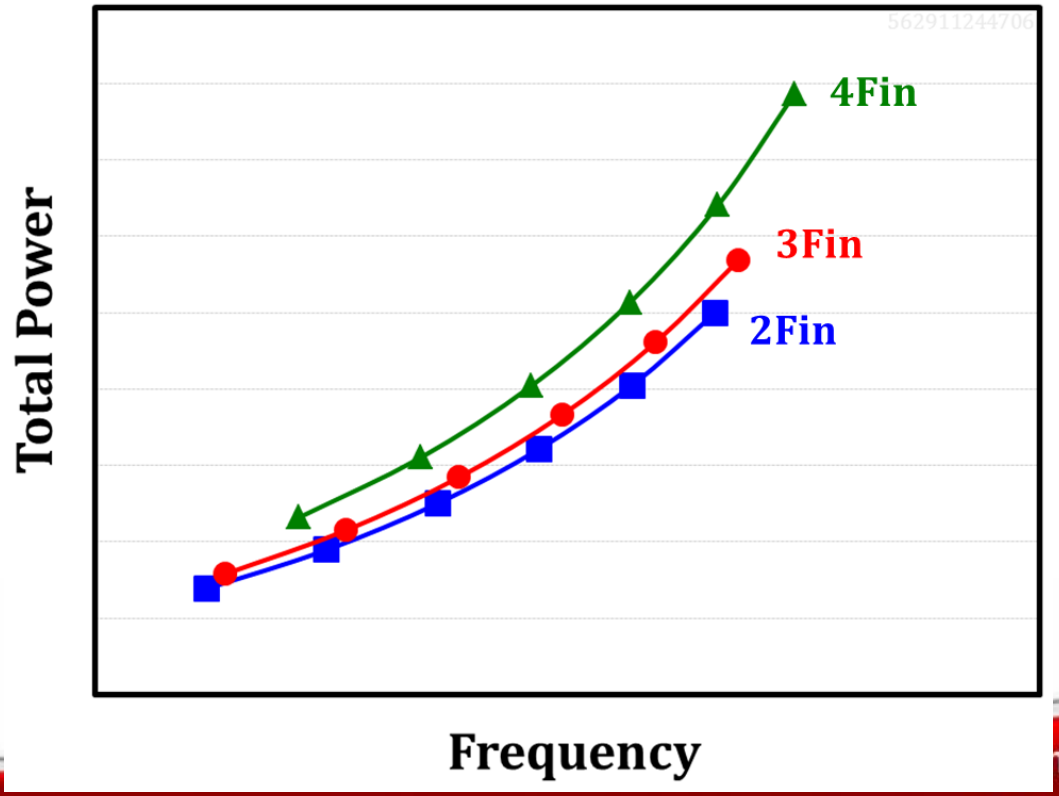
Fin Depopulation can Increase Density
and Reduce Process Dimension Scaling Pressure

4-fin cell **3-fin cell** **2-fin cell**

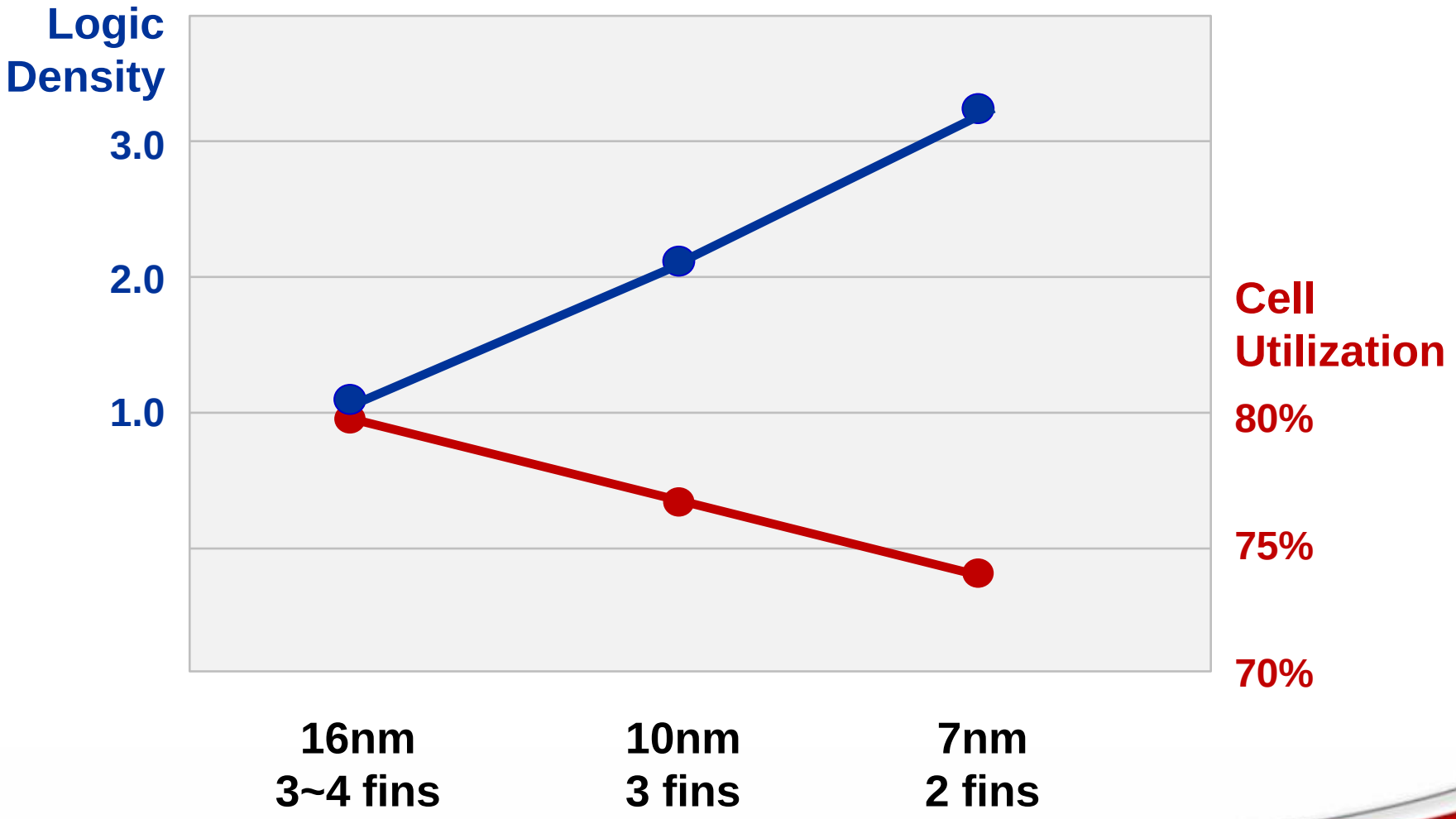


Fin Depopulation can Increase Speed and Power Efficiency

- Higher fins have highest speed
- Fewer fins have highest speed@same power and lowest power@same speed



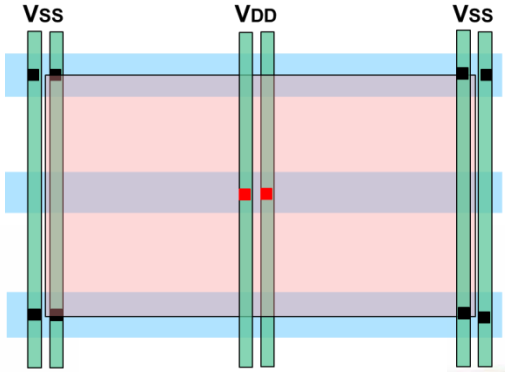
Fin Depopulation Impact on Logic Density and Cell Utilization



Logic Density Improvement (I)
Power Plan Optimization

- To improve power plan IR, PG via count is increasing over technology generations

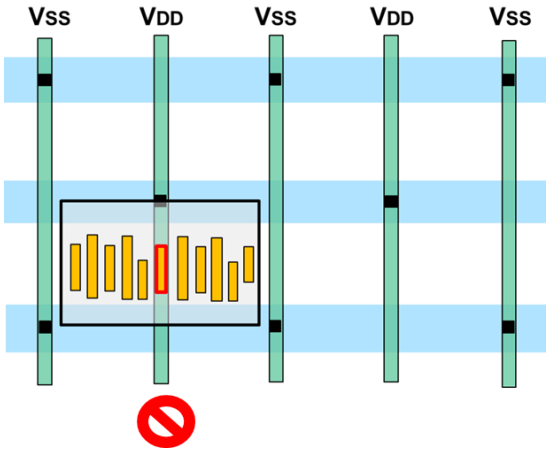
- However, shrinking PG pitch impacts routing resources. So different and new PG design approaches evolved



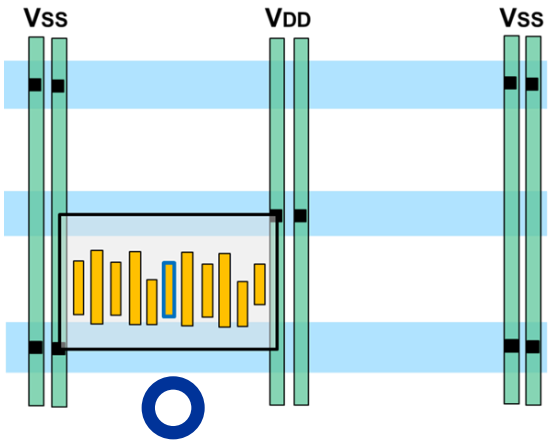
Allows better cell placement freedom

Logic Density Improvement (II)
Power Plan and Cell Layout Co-optimization

Uniform M1

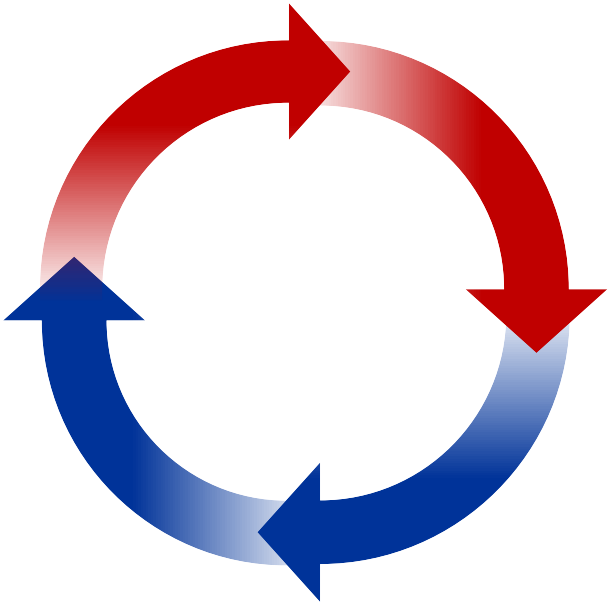


Dual M1



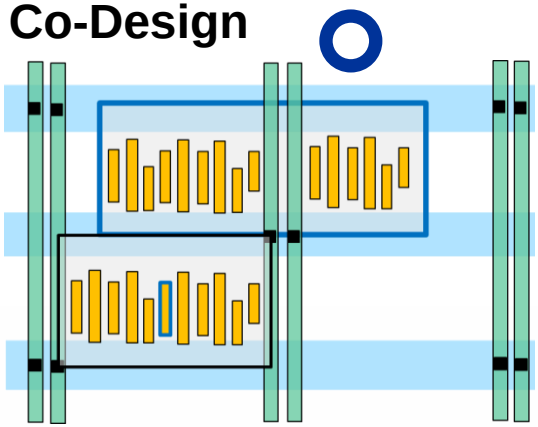
PG design has to be friendly to cell architecture (Uniform → Dual)

Top Down

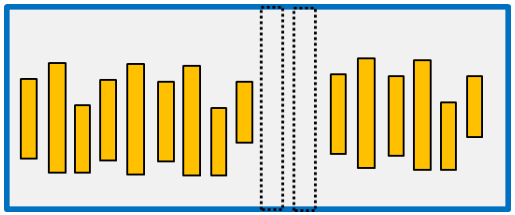


Bottom Up

PG and Cell Optimized Co-Design



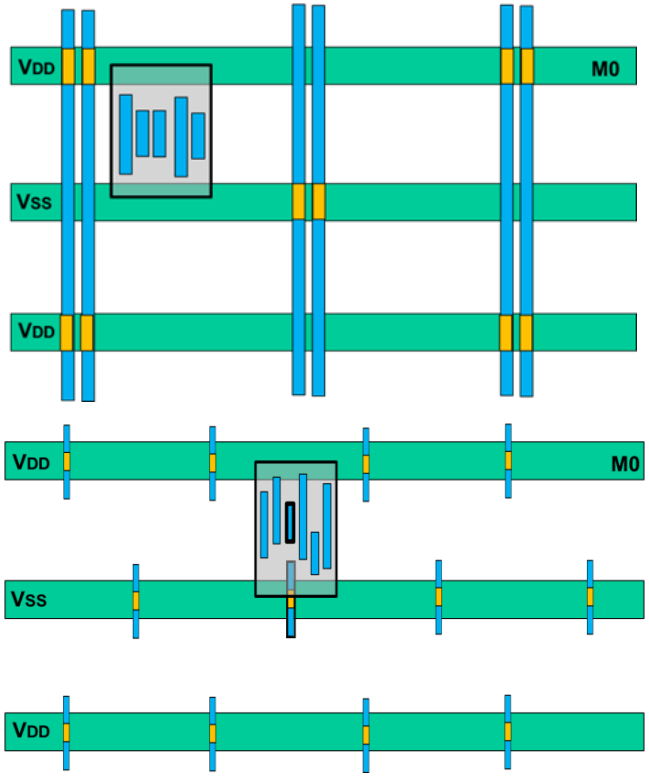
Cell re-Design



Big cell design has to be redesigned to be compatible with Dual PG architecture

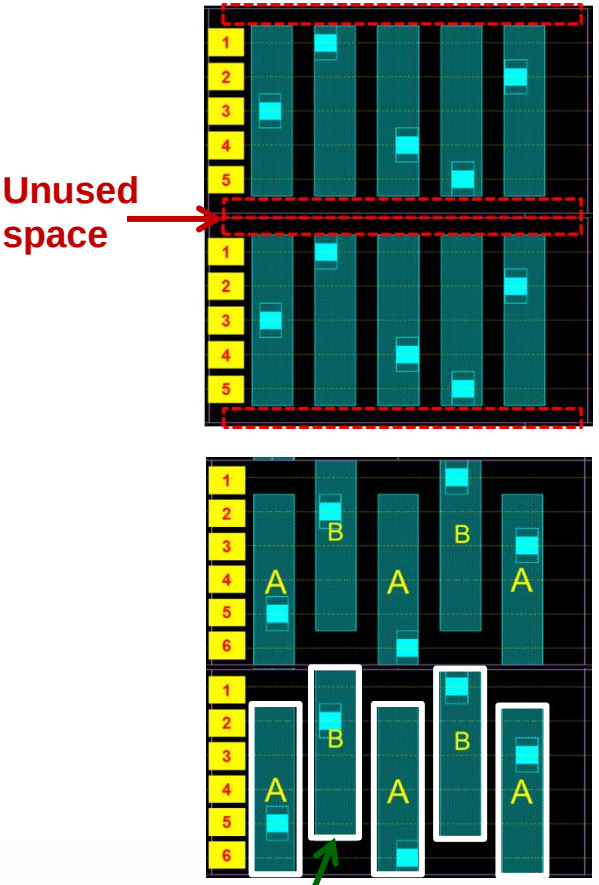
Logic Density Improvement (III)
Power Plan and Cell Layout Push to Limit

Power strap:
Less cells placed under PG



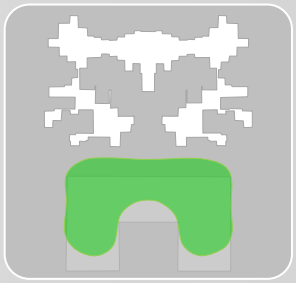
Power stub:
More cells placed under PG

No stagger pin: 5 access points

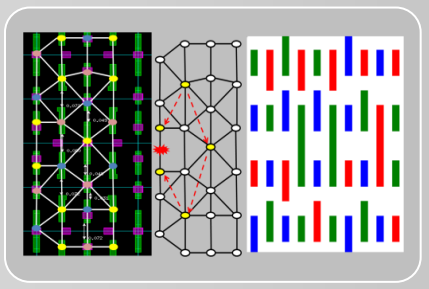


Stagger pin: 6 access points

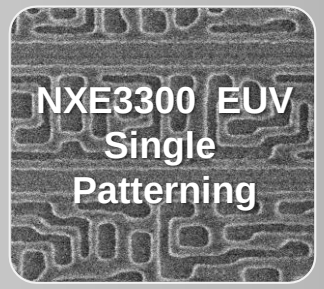
Logic Density Improvement (IV)
EUV to Increase Routing Density



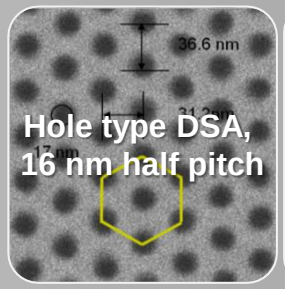
Inverse Litho.

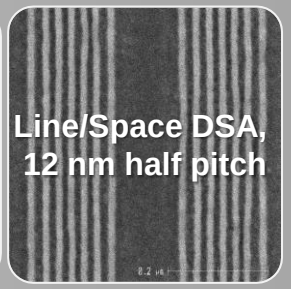


Multiple patterning



EUV

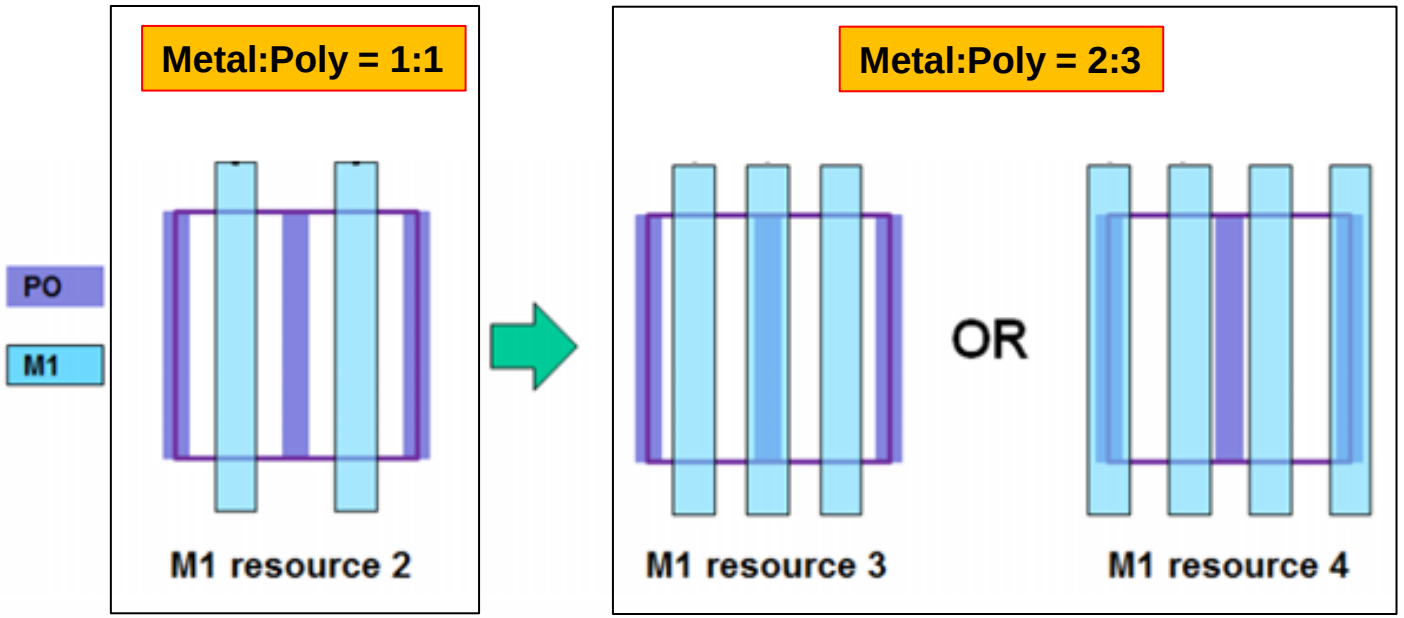




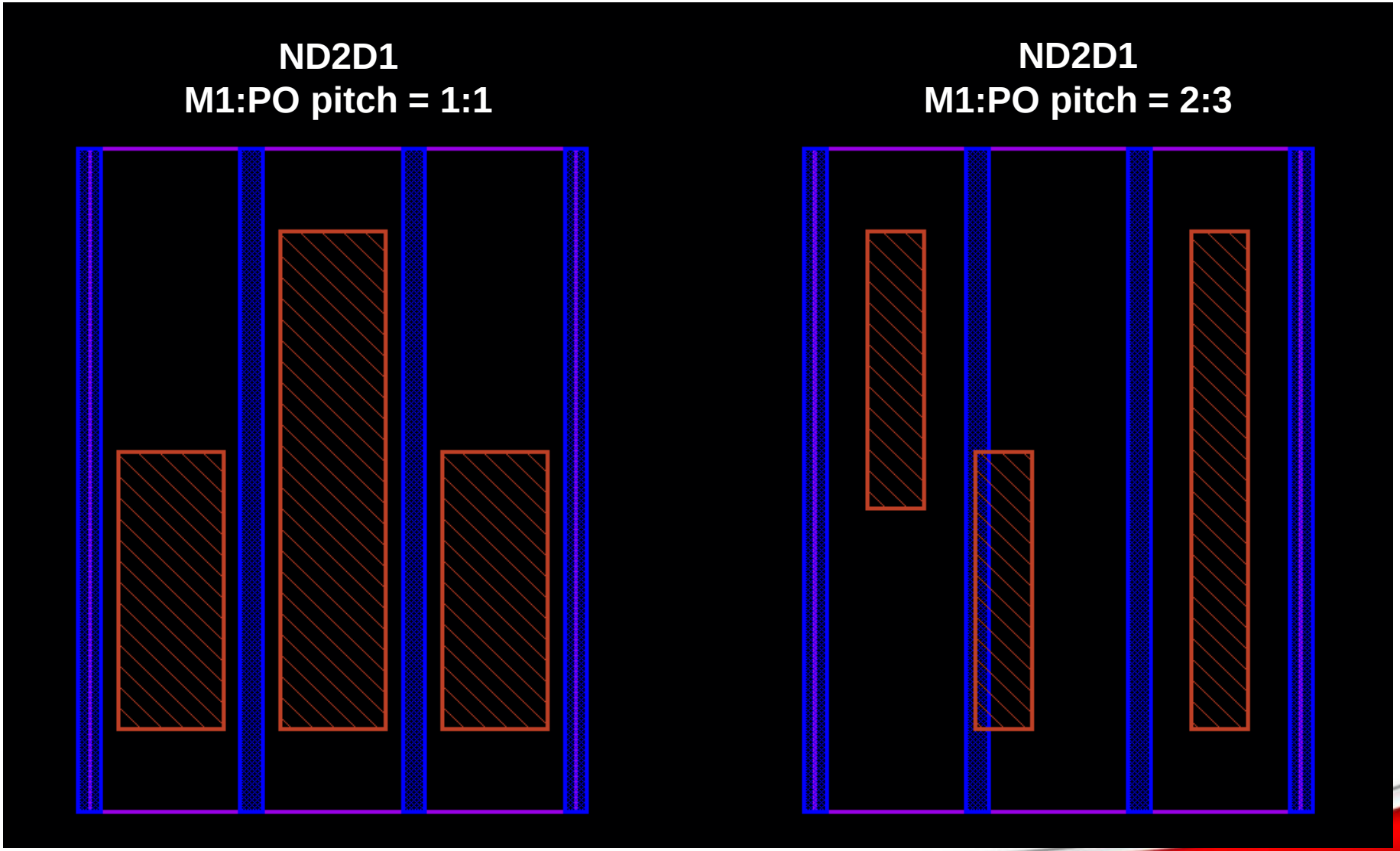
Directed Self-Assembly

EUV Metal
Metal : Poly pitch = 2 : 3

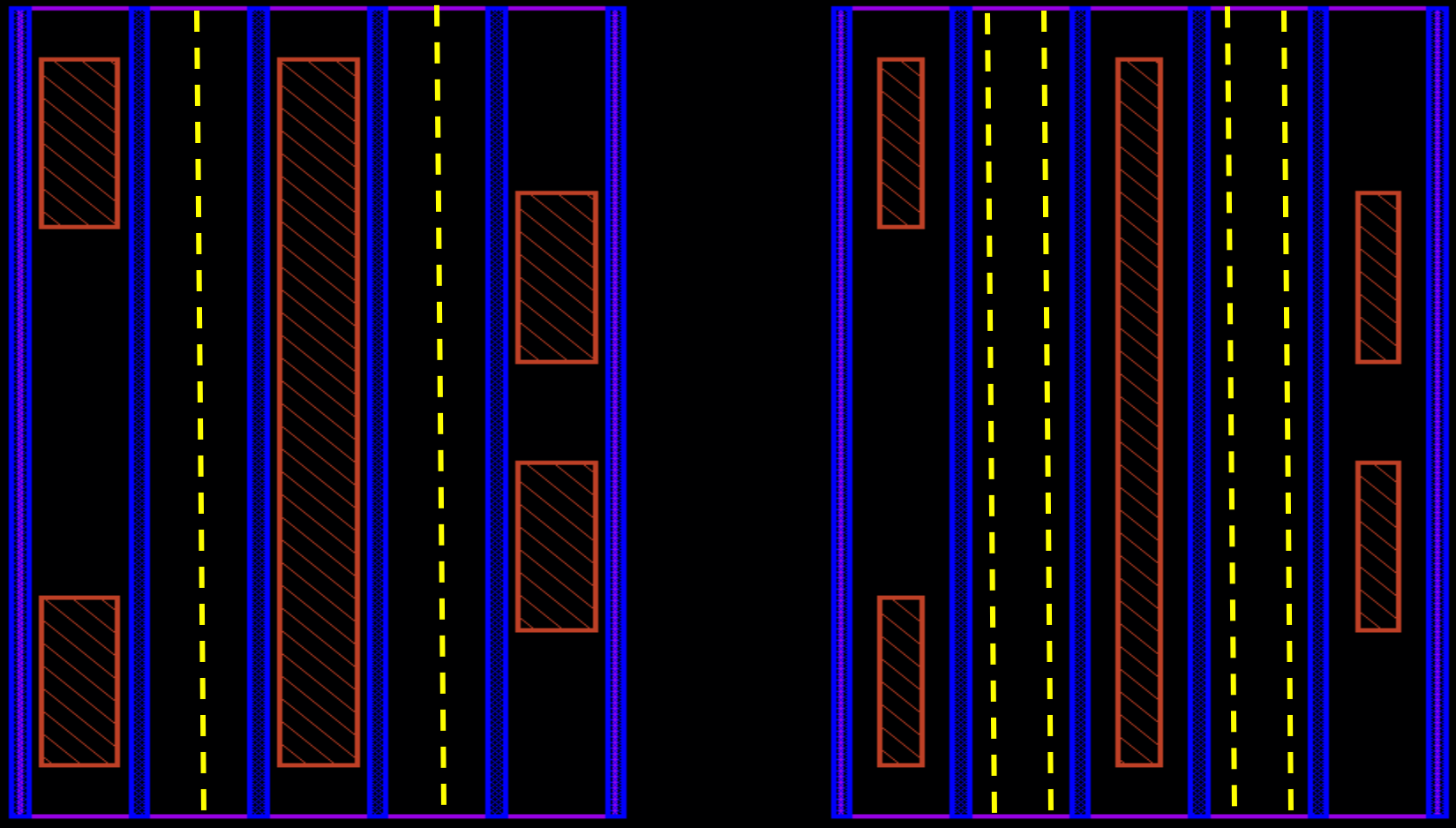
- More Metal resources for logic density improvement
- 2 library sets are needed for two metal offset.



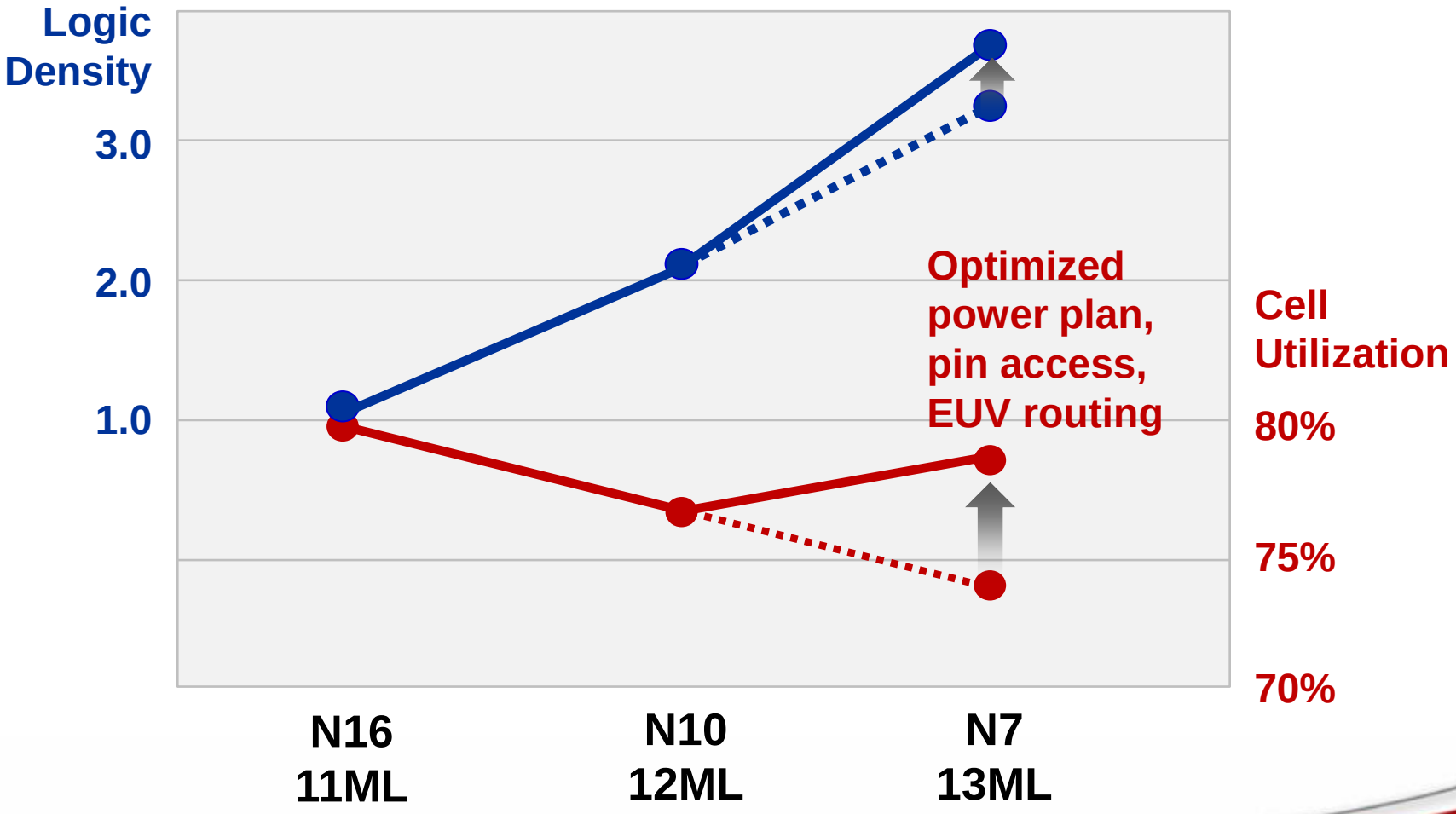
Less Coupling from Metal : Poly = 2 : 3



More Routing from Metal : Poly = 2 : 3



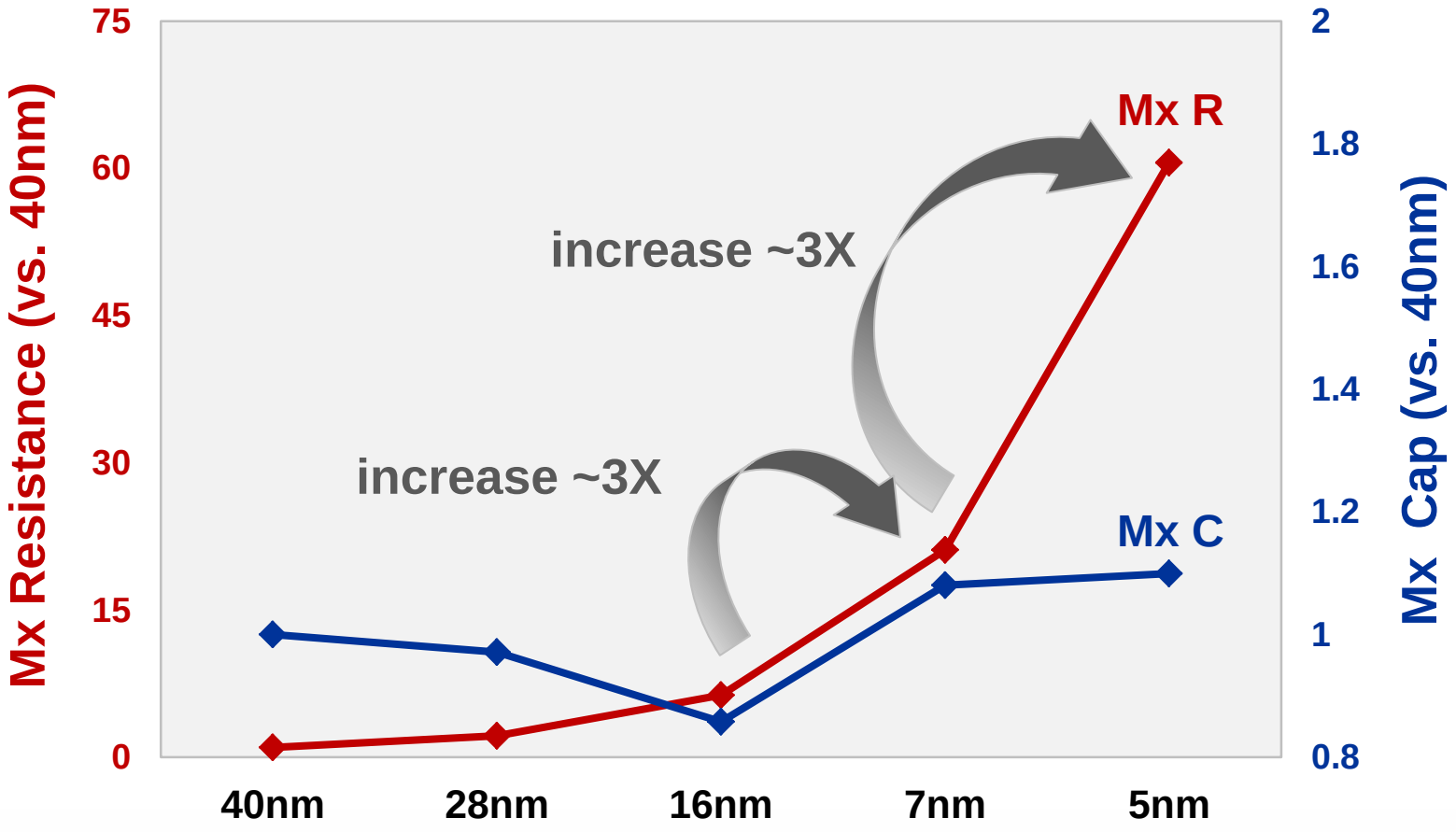
Enhanced Logic Density and Cell Utilization Trends



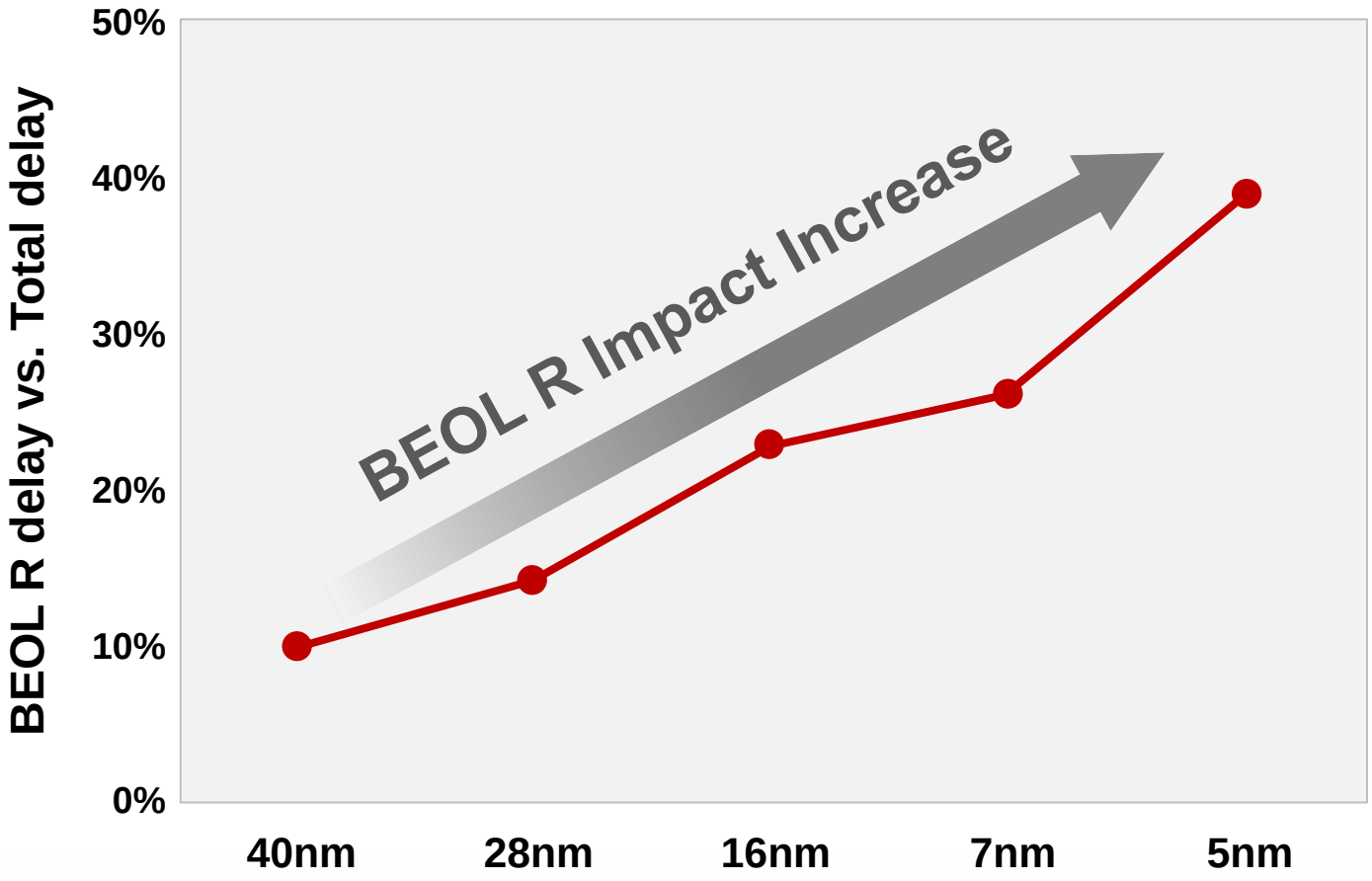
Performance Scaling

- **Process dimension scaling grows metal and via resistance exponentially**
- **Fully automatic and smart EDA design flow is needed to effectively solve high resistance issue for 7nm and beyond**

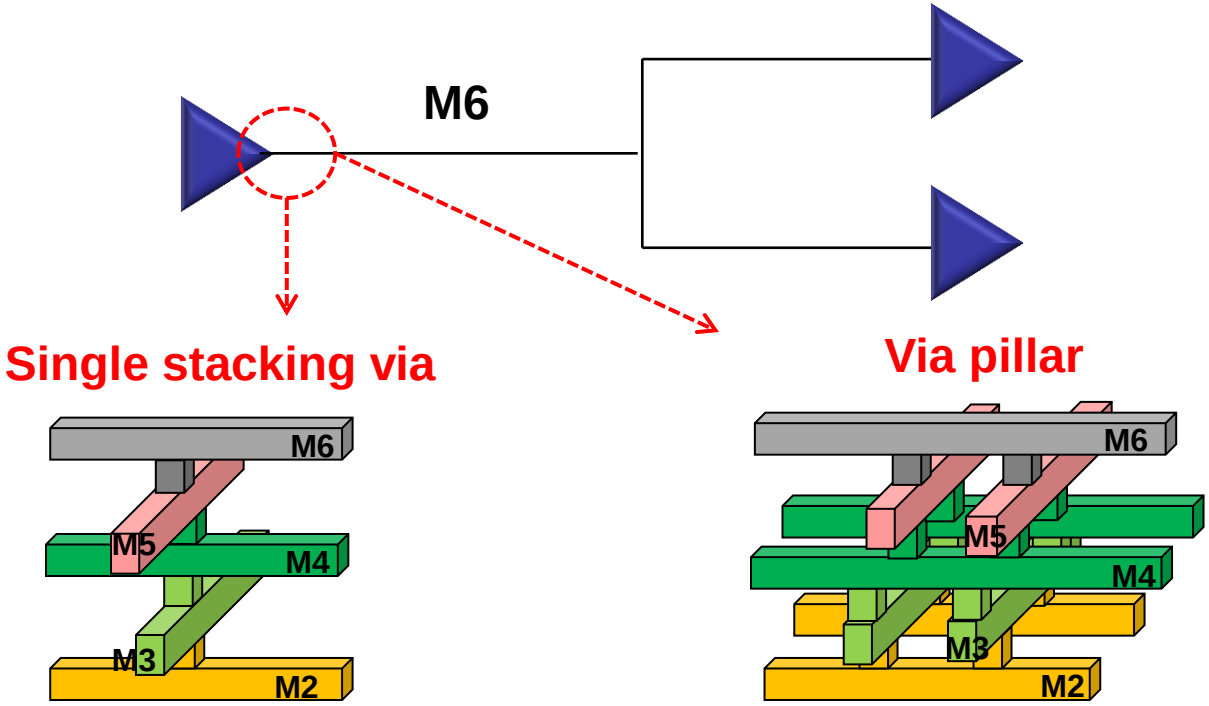
Cross Node Metal RC Scaling



Cross Node Wire R and Via Impact



VIA Pillar

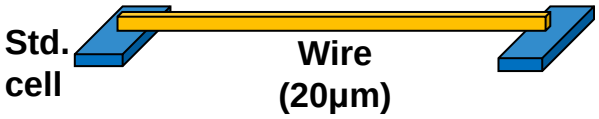


- **Large drivers + upper thick metal + via pillar to reduce transistor, metal and via resistance**
- **VIA-Pillar enablement is complex and requires EDA enablement across all Implementation phases**

Via Pillar Insertion

- Implies layer promotion for better wire resistance
- Effectively reduces source Via resistance

Connection through DPT layer: DPT wire resistance dominates



Metal R	Source Via R
55.43X	1X

Layer promotion to non-DPT layer: Source Via resistance increases

Metal R	Source Via R
13.23X	3.29X

Via pillar: Best combination of metal and source Via resistance

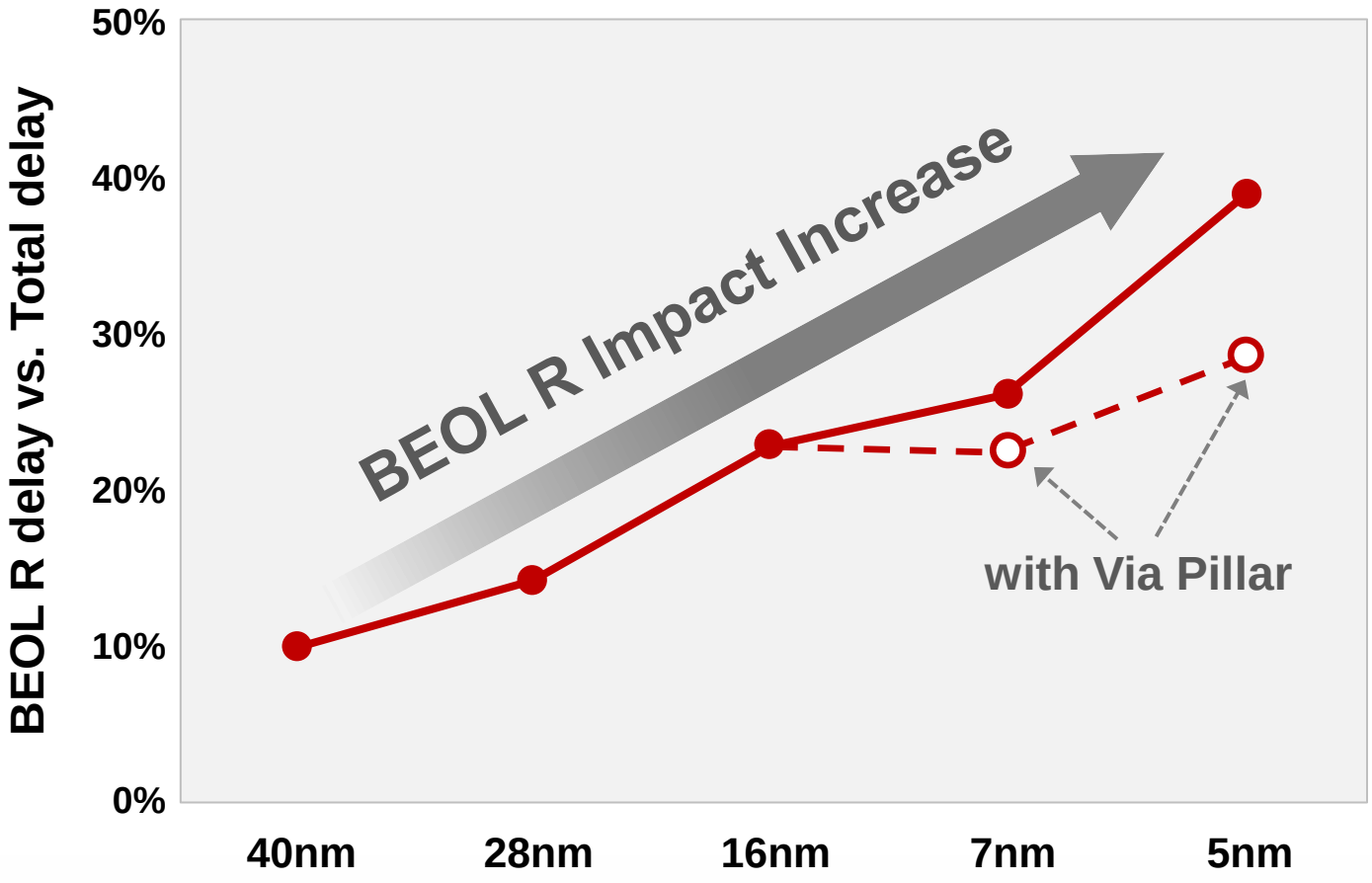
Metal R	Source Via R
13.23X	1X

Std. cell

Double Patterning Technology (DTP) Layer

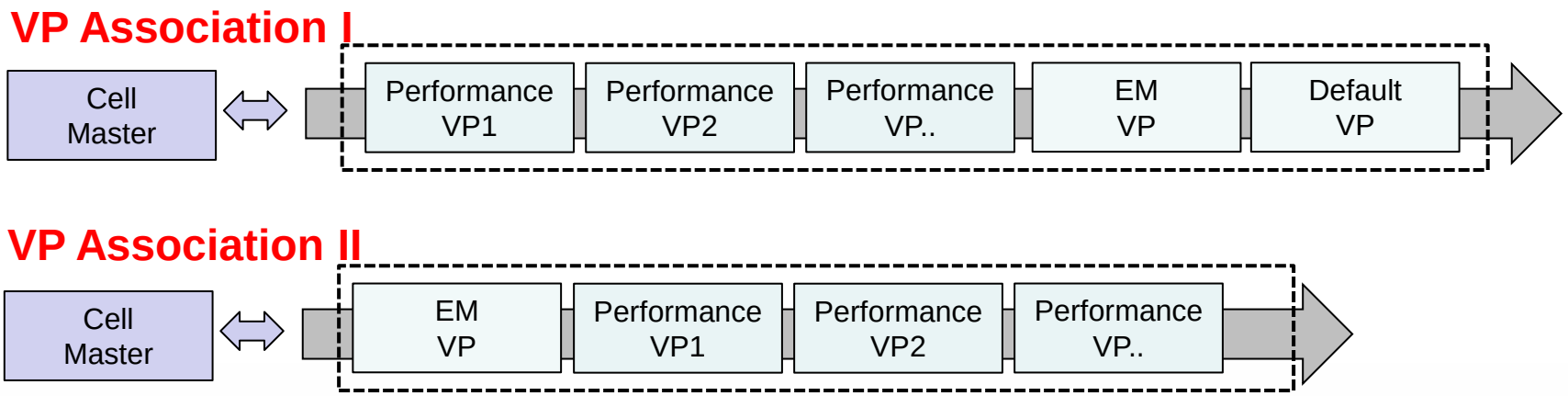
Non-Double Patterning Technology (DTP) Layer

Cross Node Wire R and Via Impact

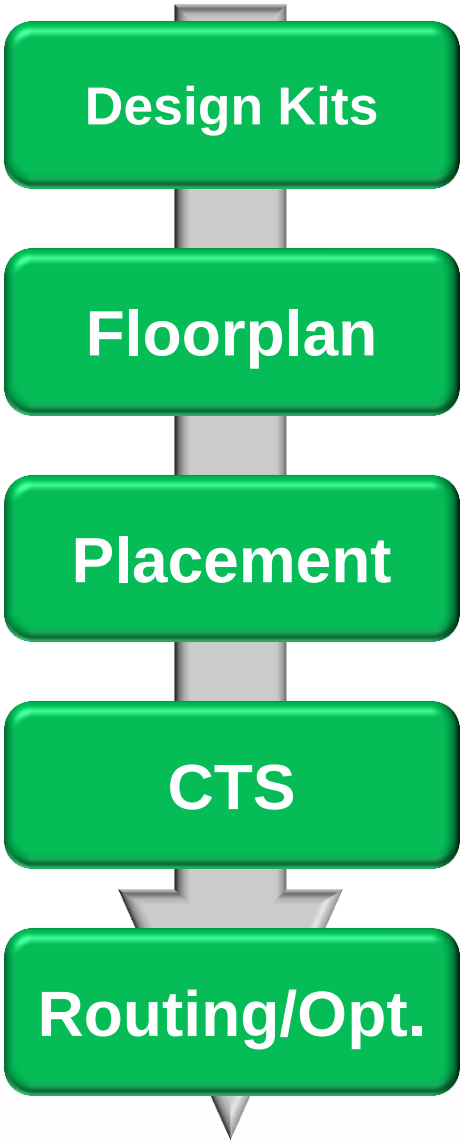


Via Pillar Type and Usage

- **EM via pillar (EM VP), used to guarantee cell-level EM, has to be 100% inserted**
  - **One cell master will only have 1 EM VP**
- **Performance via pillar (Performance VP), which is larger than EM VP, can reduce more resistance**
  - **One cell master can have multiple performance VP**



Via Pillar Automatic Design Flow



- VIA pillar (VP) definition, association

- VP aware placement
- Automatic NDR

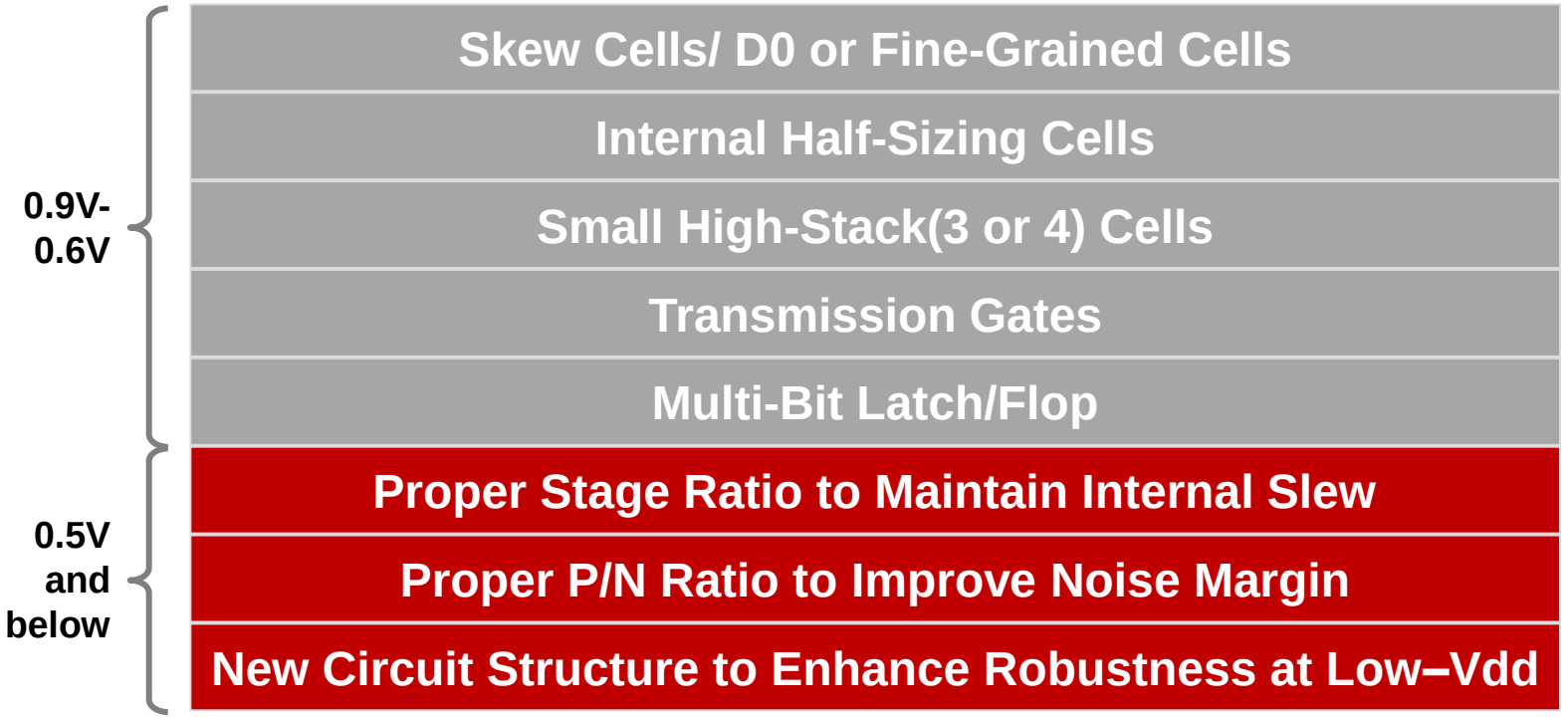
- VP insertion and verification
- CTS with VP

- VP optimization
- DEF out option

Voltage and Power Scaling

- Low voltage design reduces power effectively
- Low voltage design challenges
  - Functionality robustness
  - Accurate variation modeling

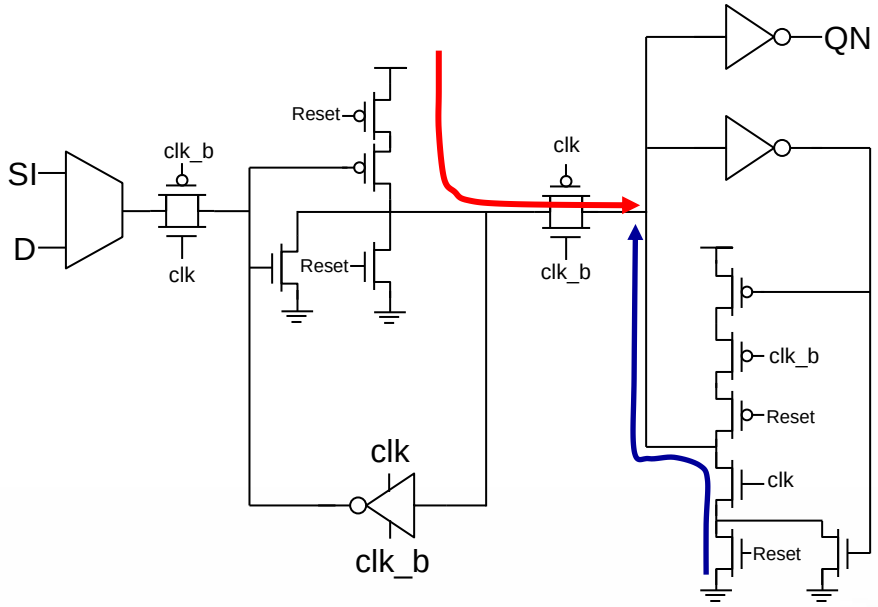
Ultra-Low-Voltage Standard Cell Solution



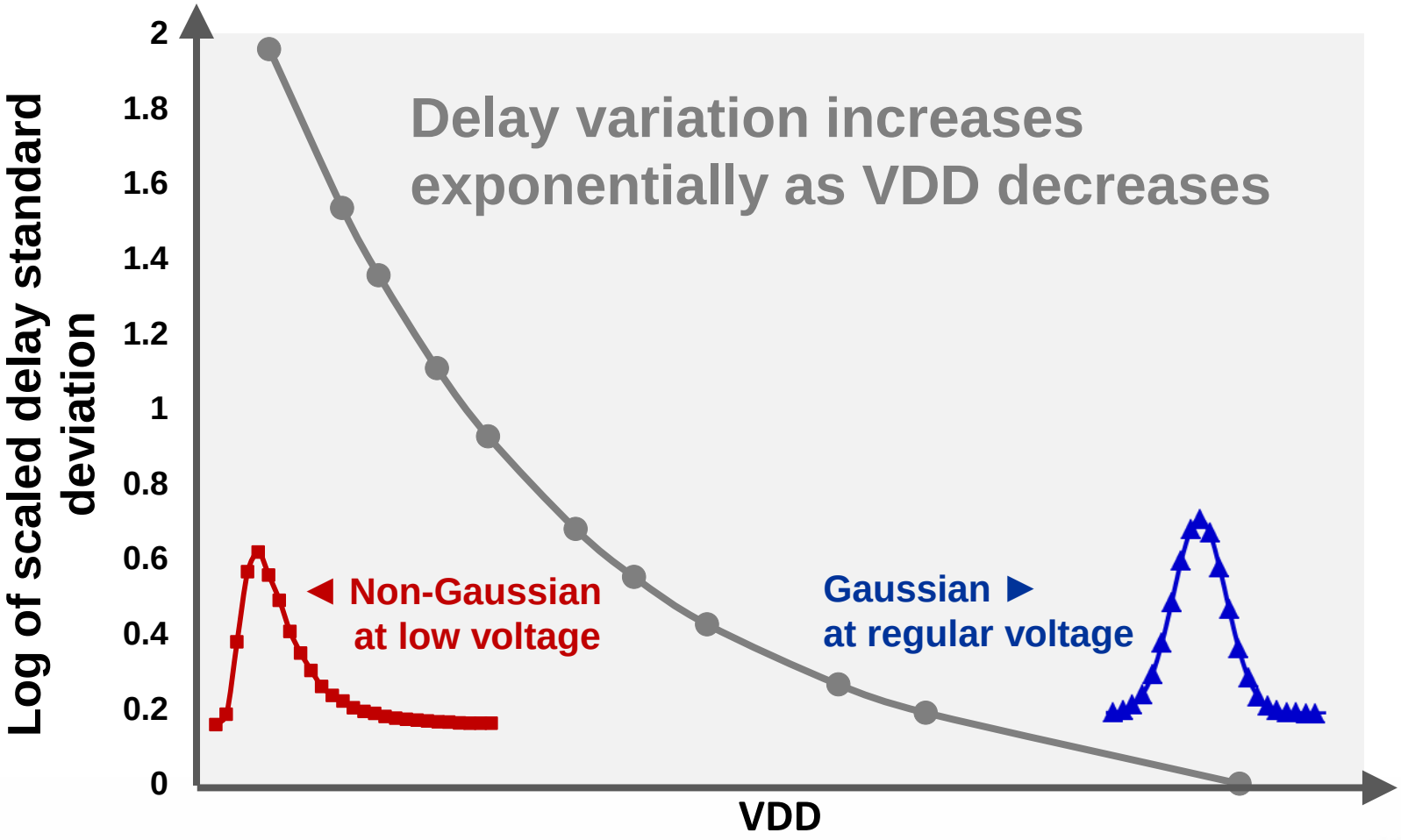
- Improve cell performance by reducing delay degradation and variation induced by low-Vdd

Flop Low Voltage Design Robustness

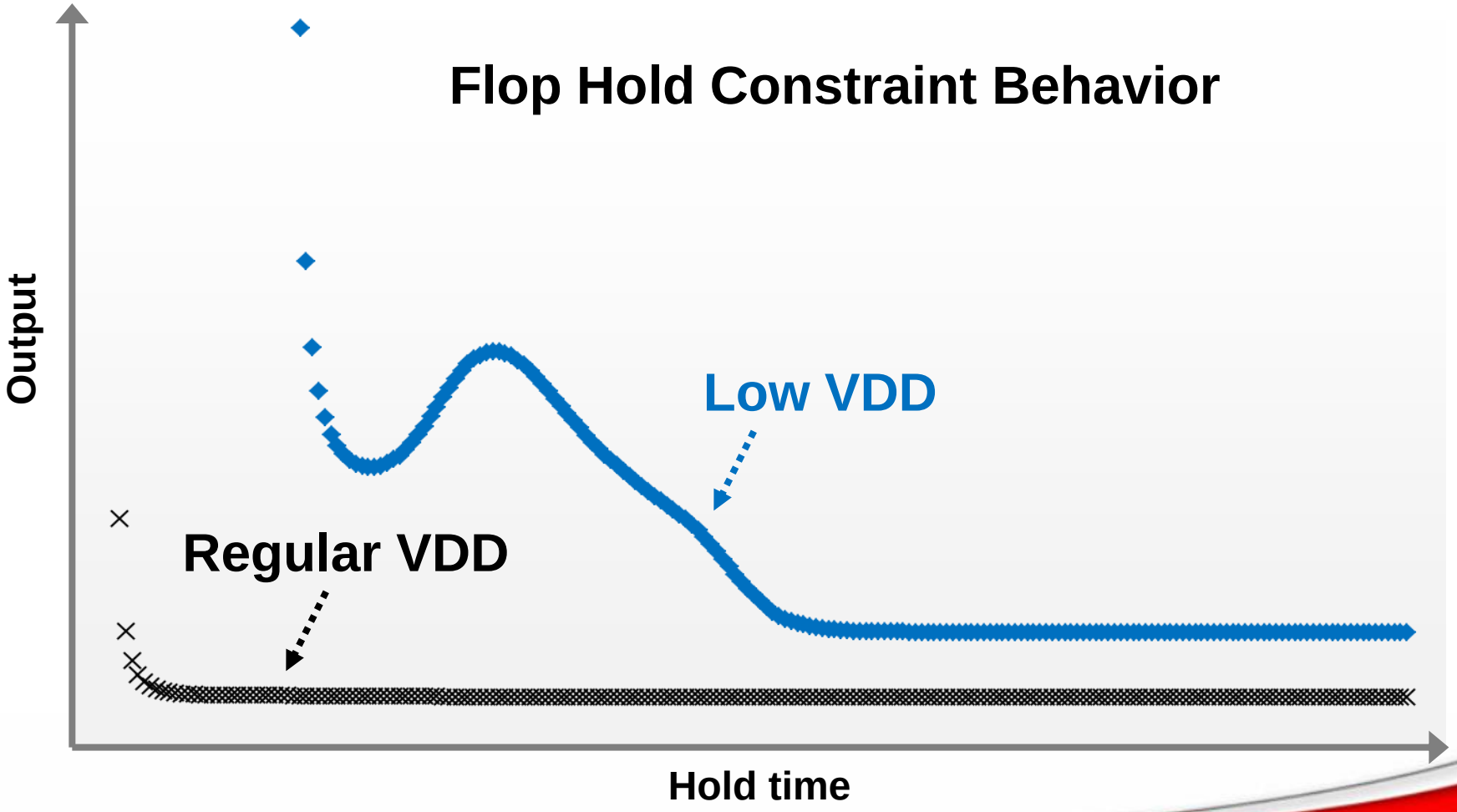
- **High sigma design checks are required to ensure robust operation at low operating voltage**
- **For write operation, forward path (red) must be stronger than feedback path (blue)**



Delay Variation Increases at Lower VDD

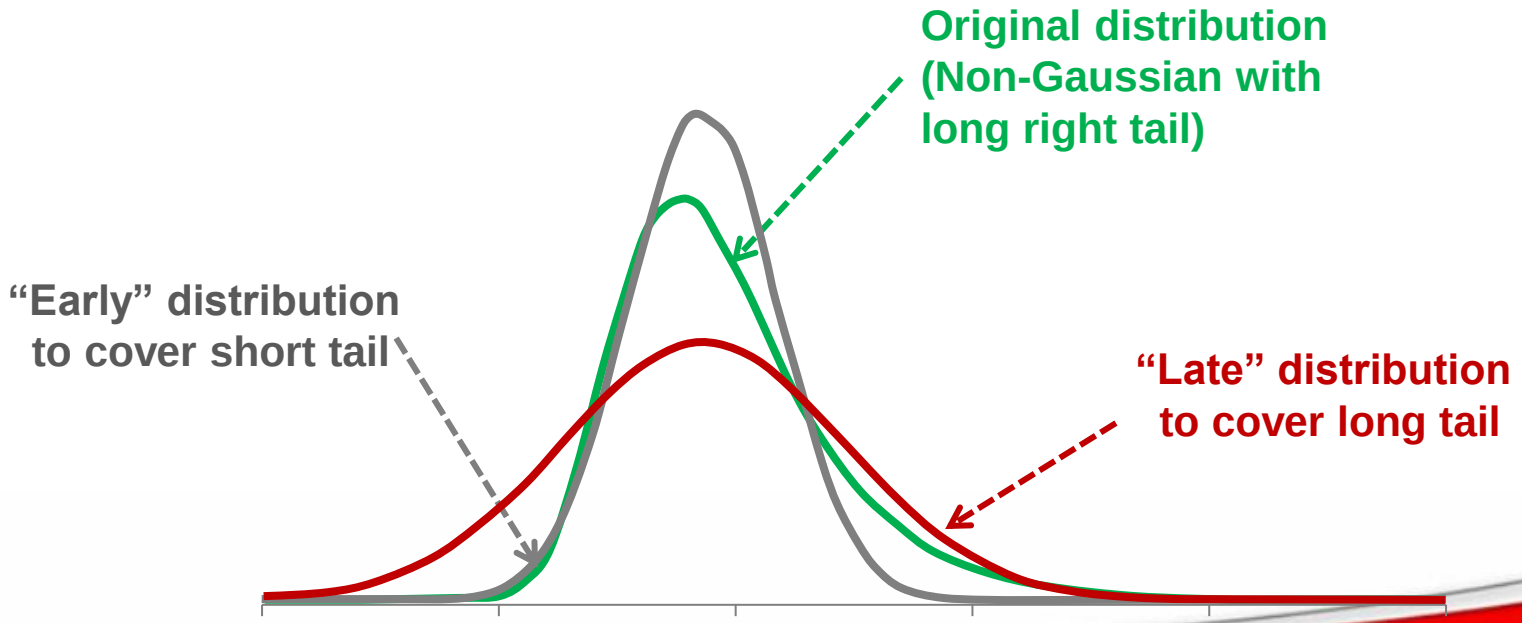


Abnormal Hold-Time Caused by Low-Vdd Non-Gaussian Behavior



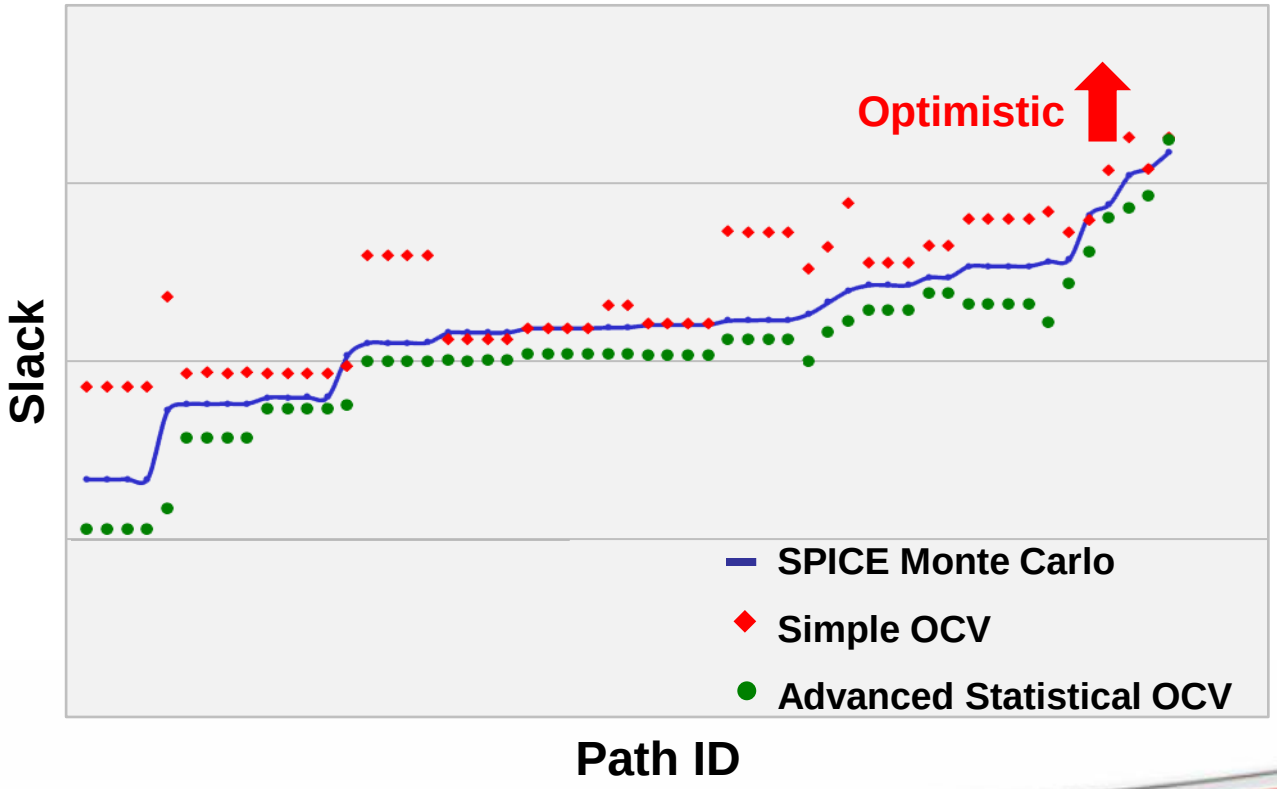
Solutions for Low-Vdd Variations (I)

- **Methodology improvement**
  - **Timing values are models by both "mean" and "early/late distribution"**
  - **Implement the new models in timing characterization and STA tools**



Solutions for Low-Vdd Variations (II)

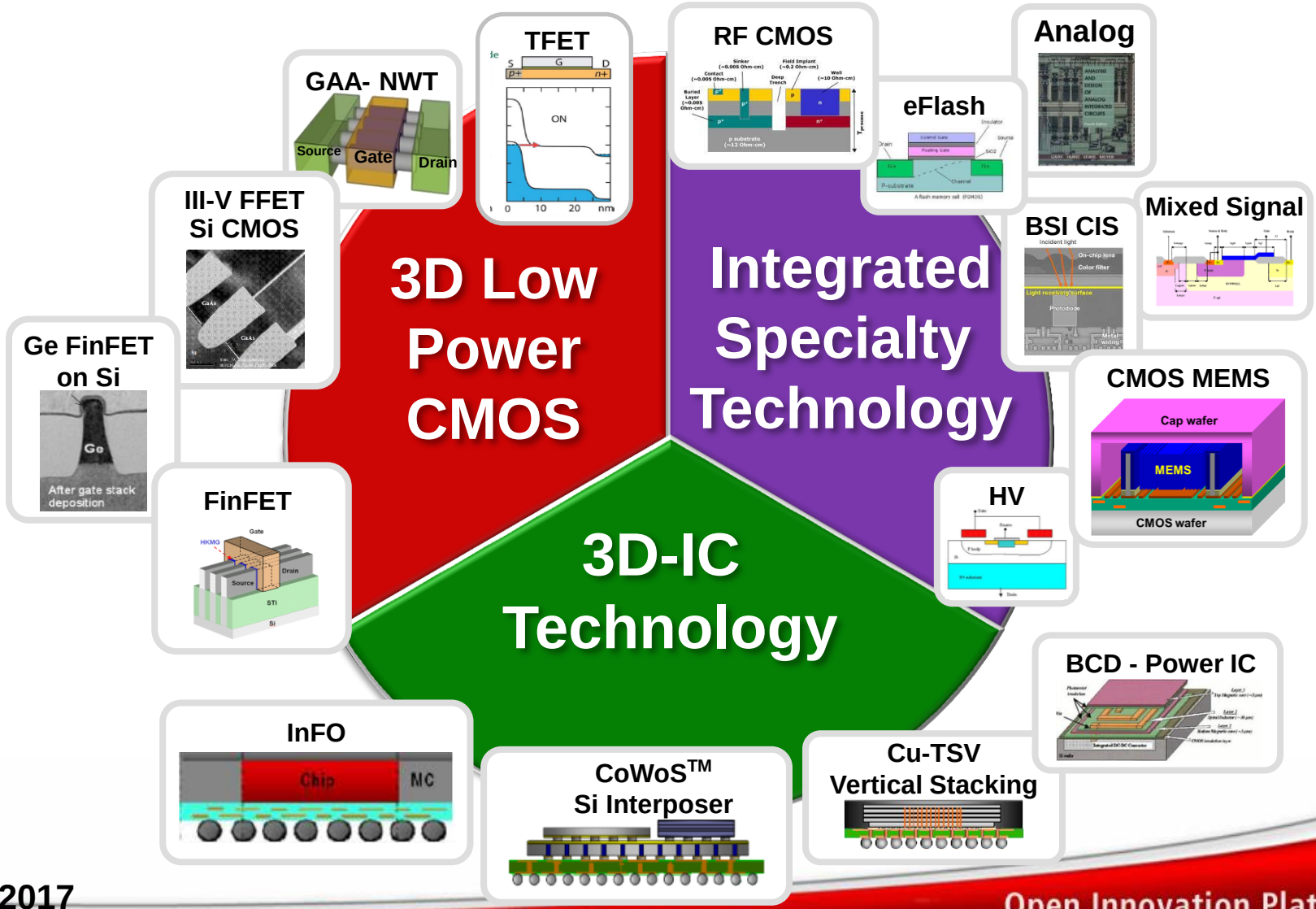
- By using new timing model and advanced statistical OCV method, we achieve more accurate STA results compared to Monte-Carlo simulations



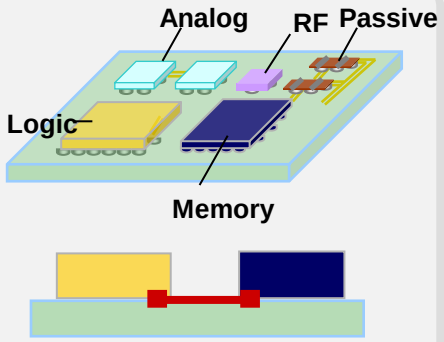
Heterogeneous Integration

- Low cost and high system performance
- InFO and CoWoS integration
- Integrated EDA design flow for package and chips

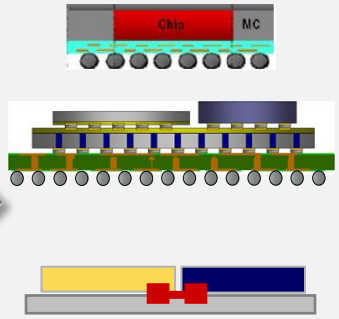
Future Device Possibilities Through Heterogeneous Technology Integration



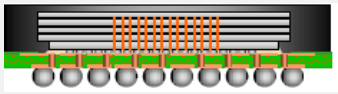
3D Packaging for Better System Performance and Form Factor



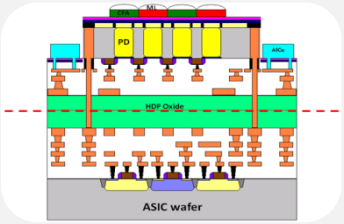
Conventional



CoWoS / InFO



Vertical Stacking



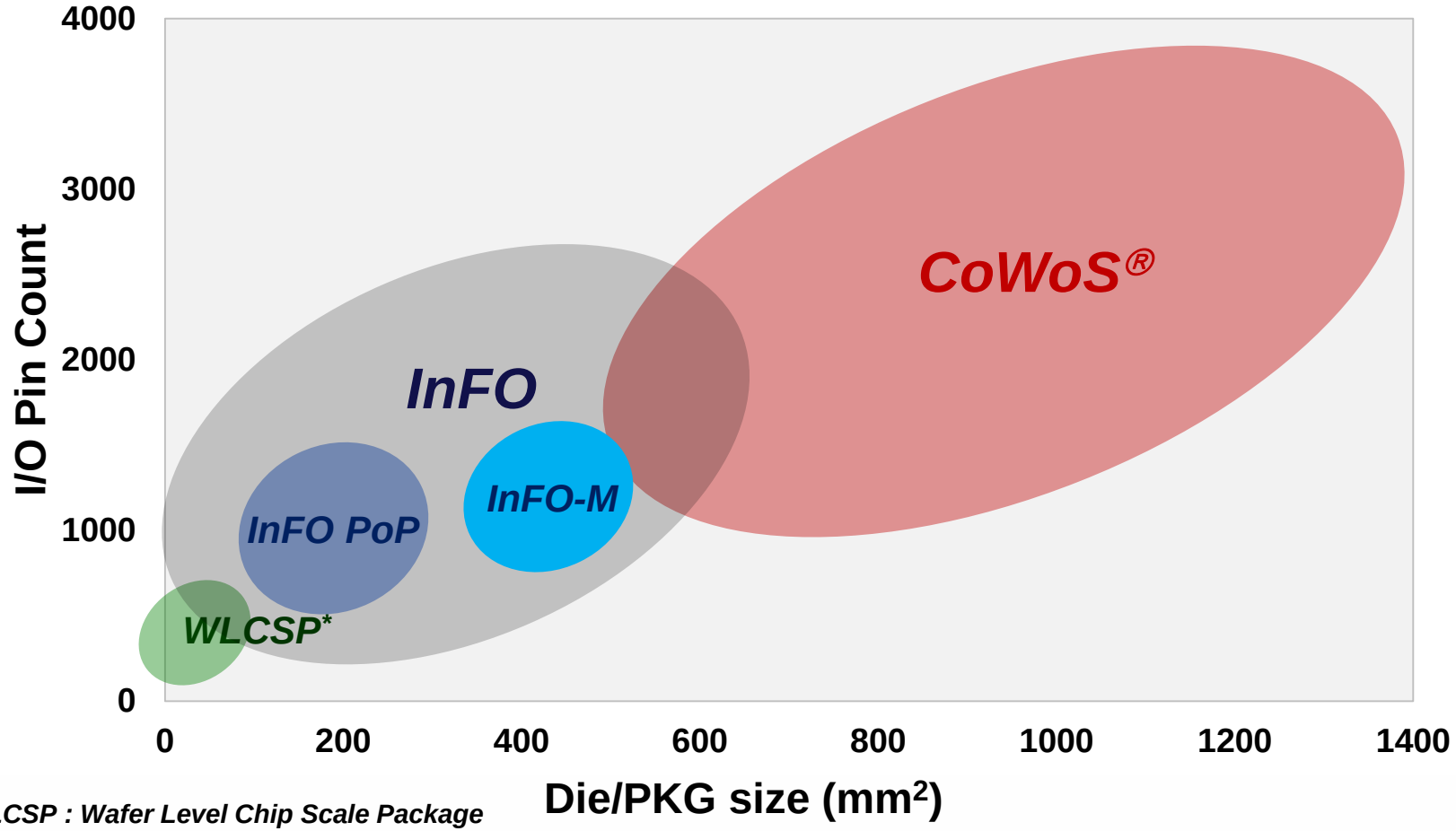
Wafer Bonding

Conventional SIP or MCM
(Wirebond, Flipchip, SMT)

3D Wafer-based System Integration
(CoWoS, InFo-PoP, Vertical Stacking, Wafer Bonding)

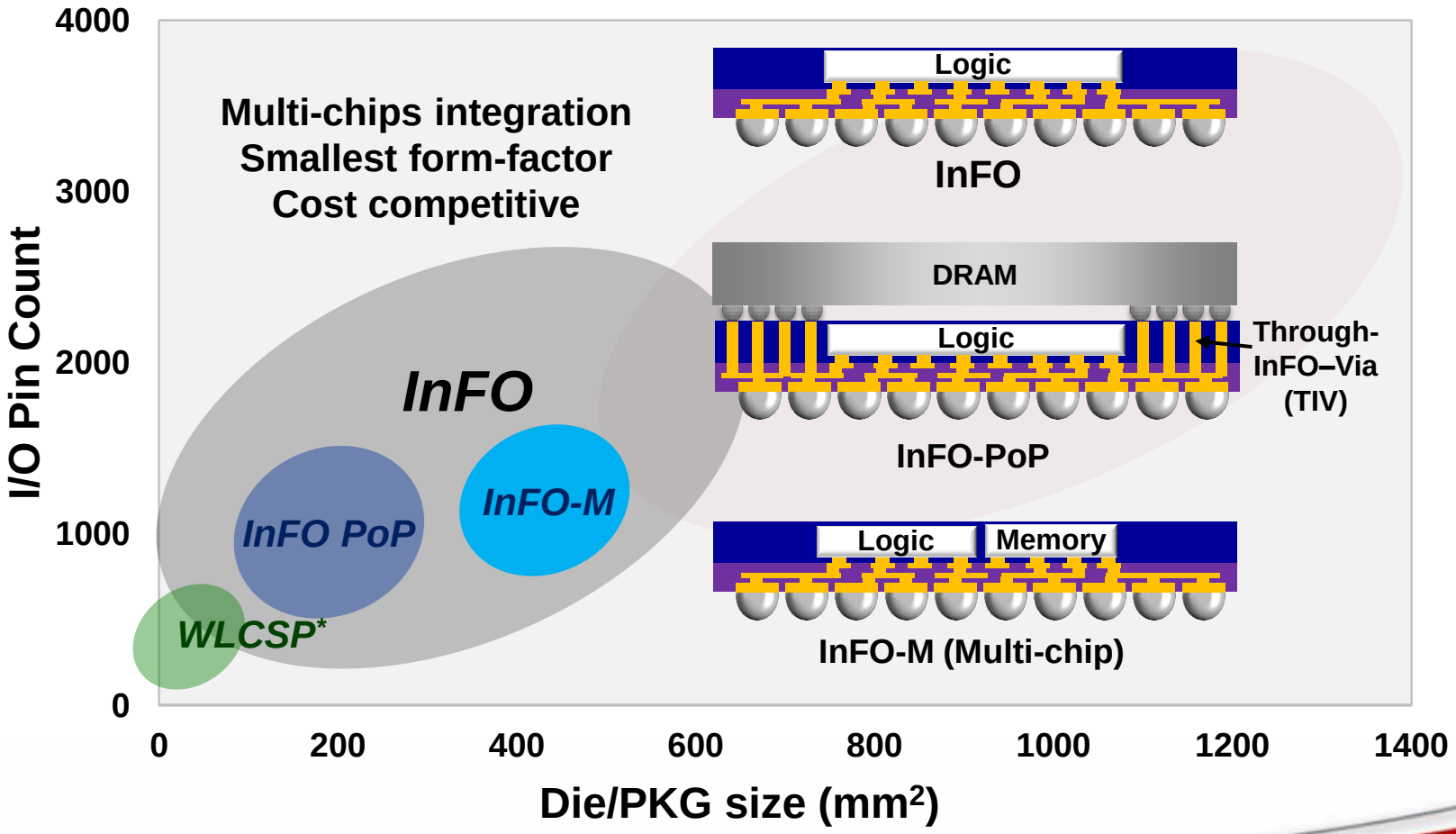
Sources: A-SSCC 2014, IEDM 2014, VLSI 2015

Different Systems Require Different Packaging Solutions

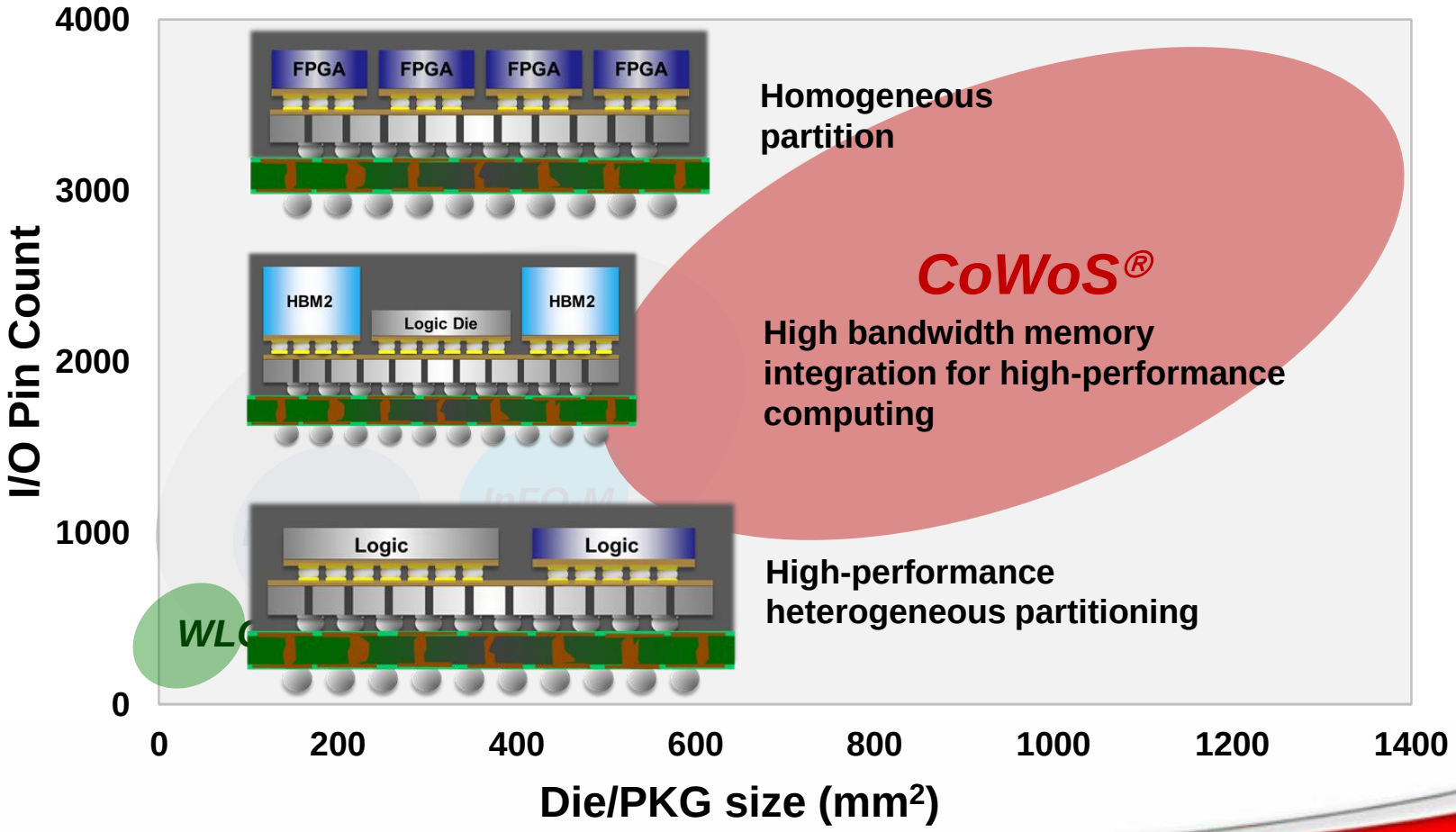


* *WLCSP : Wafer Level Chip Scale Package*
** *InFO : Integrated Fan-Out*
*** *CoWoS : Chip on Wafer on Substrate*

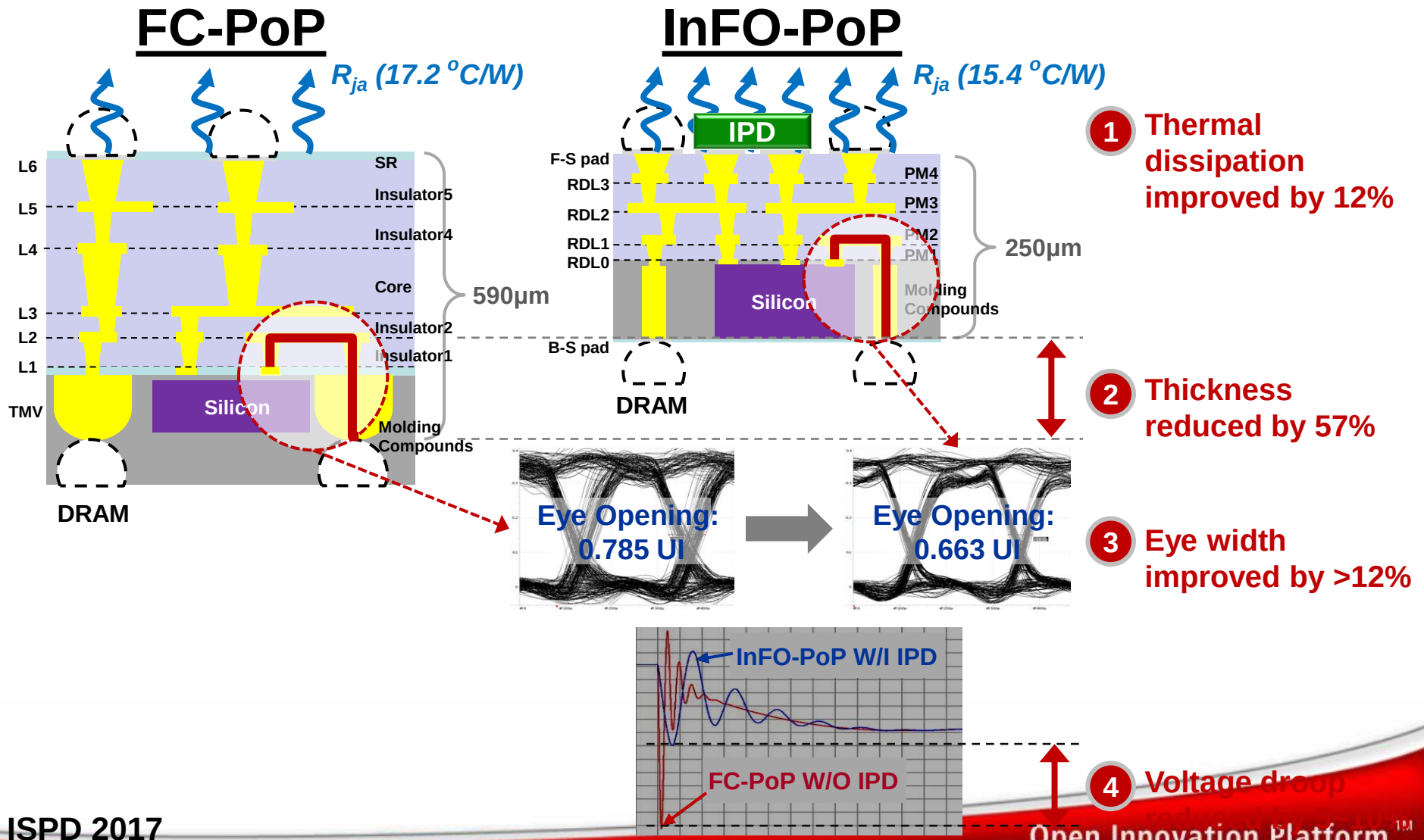
Wafer-Level Packaging Technologies: Integrated Fan-Out (InFO)



Wafer-Level Packaging Technologies: Chip-on-Wafer-on-Substrate (CoWoS)

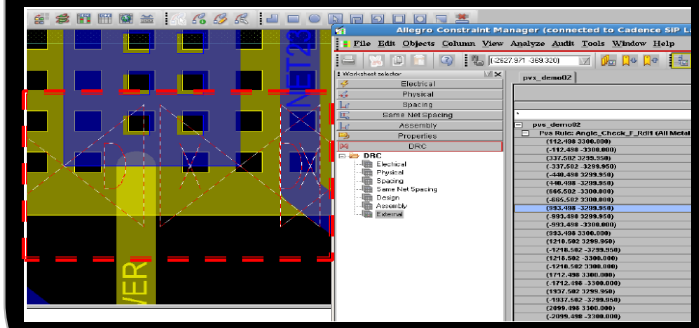


Advanced Packaging Co-Design – SoC + InFO + IPD (Integrated Passive Device)



InFO Design Solutions (InFO Only)

PKG Layout In-design DRC

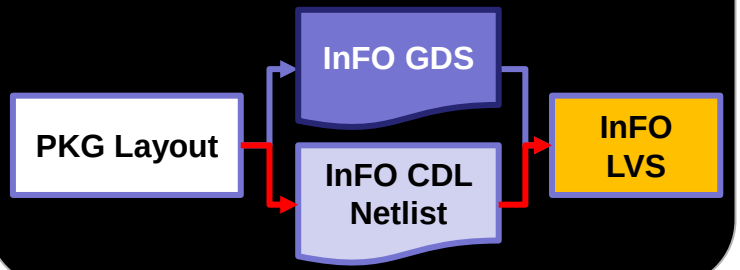


InFO Layout Creation

InFO DRC/LVS

InFO RC Extraction

CDL Netlist Auto-Export



RLCK Extraction

< 4GHz RC/RLCK Extraction for STA, IR, SEM, & PI Analysis

S-parameter Extraction

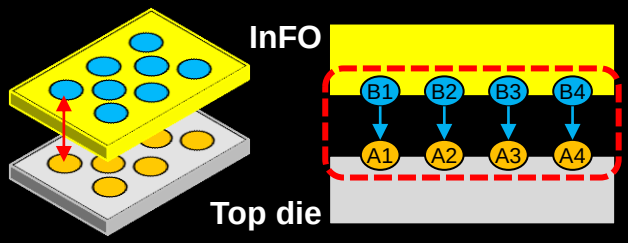
4GHz – 10GHz S-parameters Extraction for SI/PI, & EMI analysis

InFO Design Solutions (Dies + InFO)

Inter-die DRC/LVS

Inter-die DRC

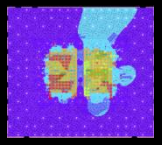
Inter-die LVS



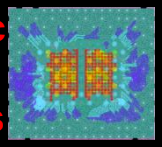
Inter-die DRC/LVS

EM/IR Analysis

Static IR Analysis

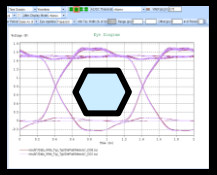


Dynamic IR Analysis

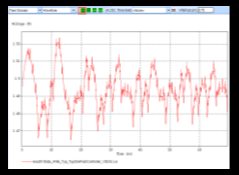


SI/PI Simulation

SI Analysis



PI Analysis

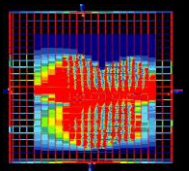


SI/PI Simulation

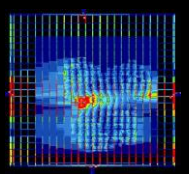
Thermal Analysis

Thermal-aware EM/IR Analysis

Normal Analysis (No Thermal)



Thermal-aware Analysis



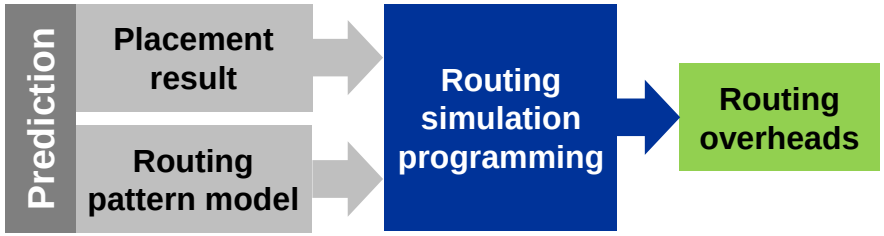
Applying Machine Learning to Complex Physical Design Problems

- Place and route Machine Learning experiment
- Feature extraction and convolutional neural network data mapping
- Clock gating and routing congestion speed improvement

Machine Learning-Based Design Solution

- **Eliminate human & fixed-model subjective bias with statistical important features**

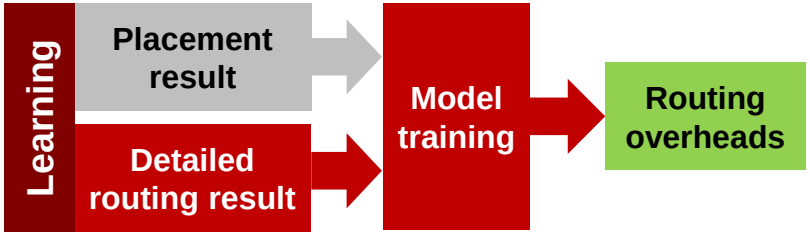
Traditional EDA Approach



Easy to be biased and no guaranteed quality

Only heuristics are possible

Machine Learning Approach

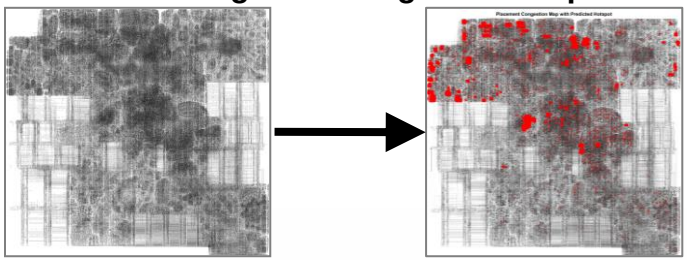


Leverage widely used deep learning packages

Traditional (EDA) flow

Pre-route design

Congestion map after routing

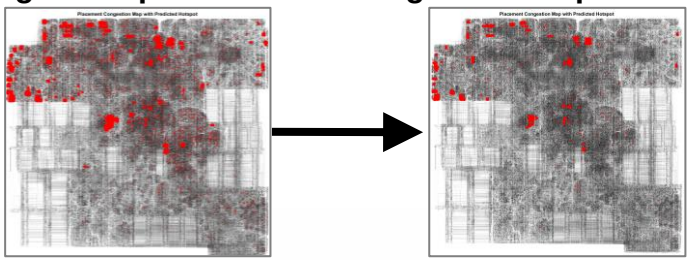


Only know routing results after running routing

Flow enables by Machine Learning

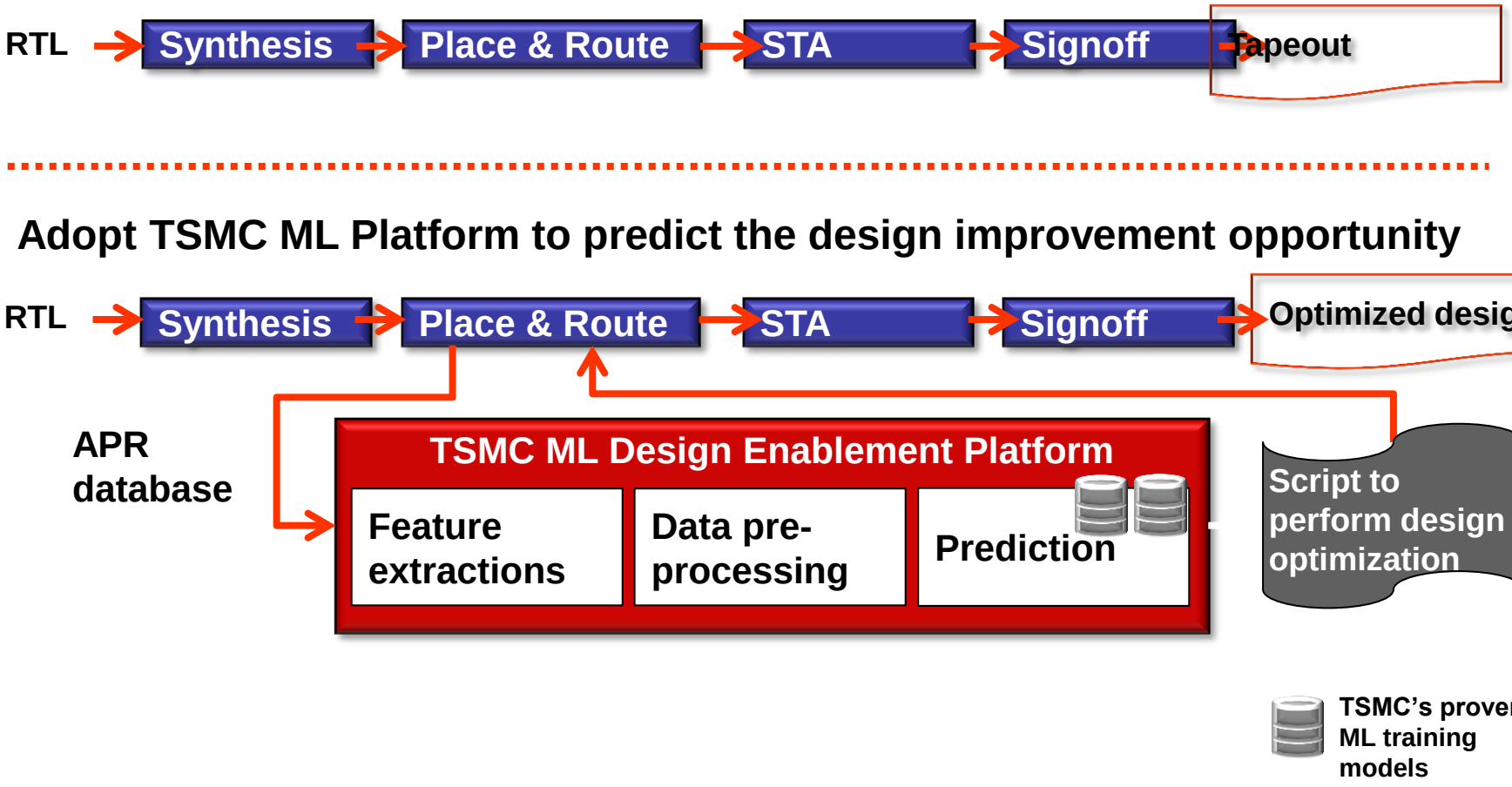
Congestion prediction

Congestion map after routing

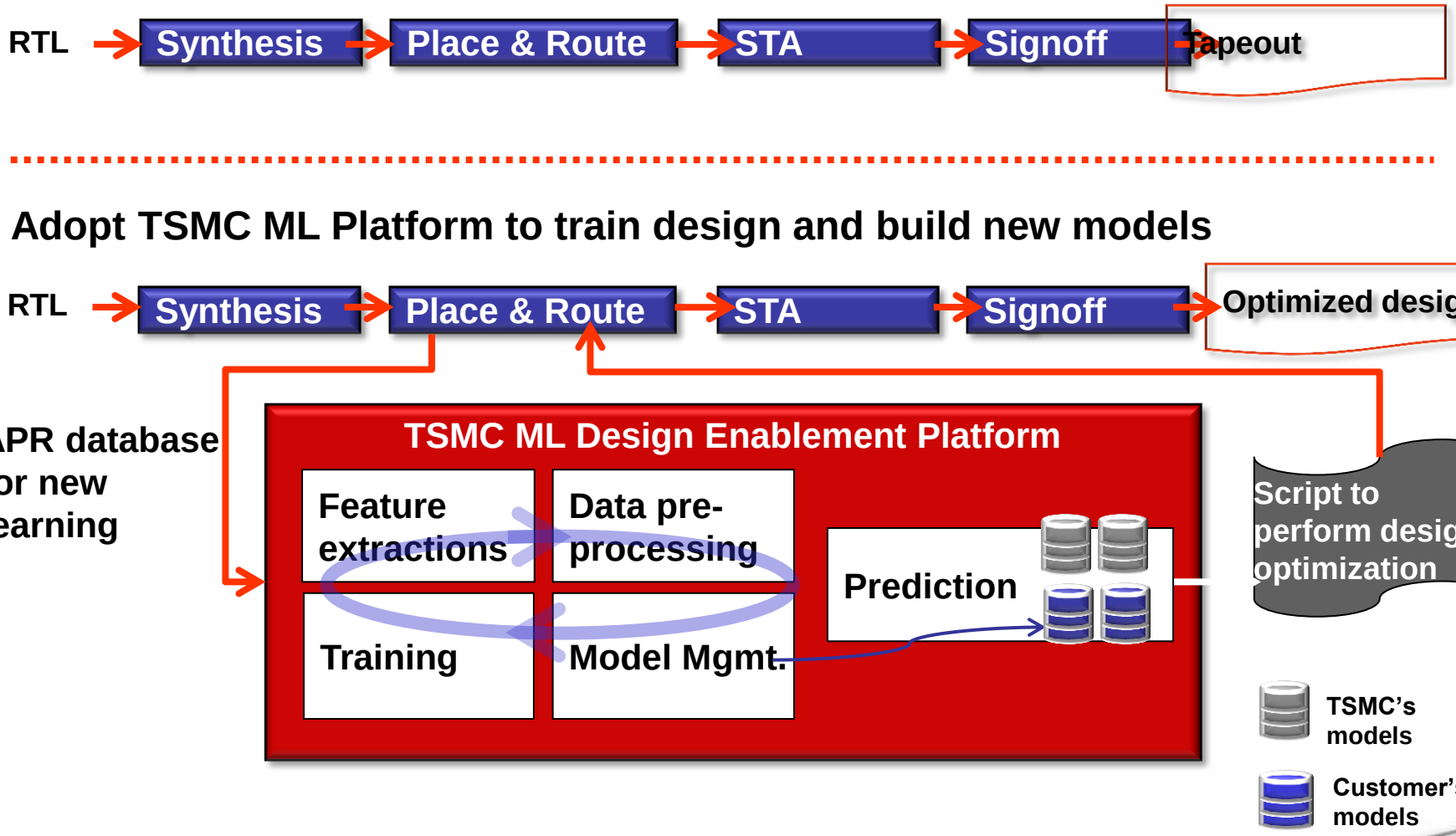


Able to predict routing behavior and improve congestion with new recipes to achieve 40Mhz speed improvement

ML Design Enablement Platform

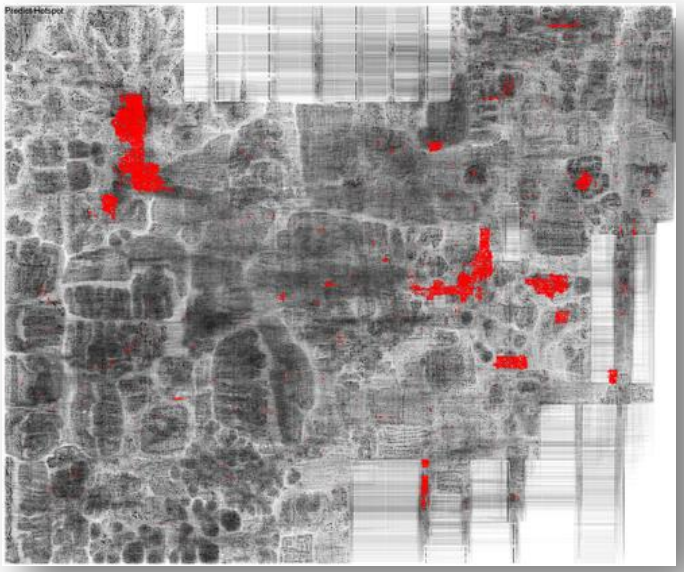


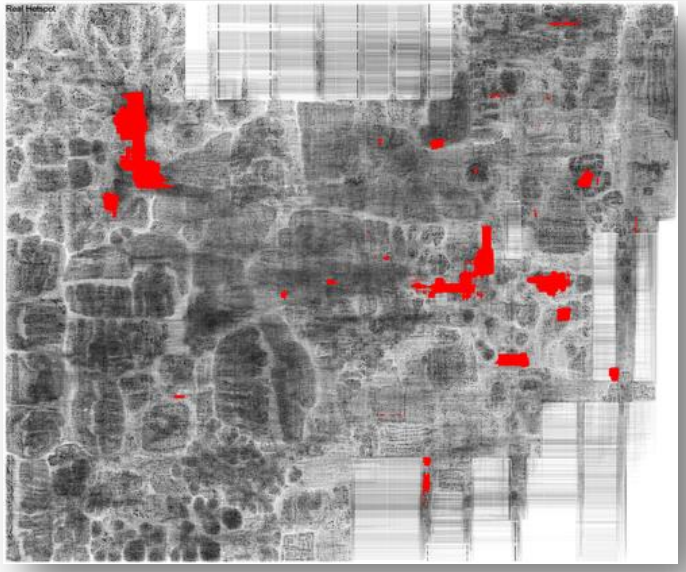
ML Design Enablement Platform



Performance Gains Prediction from ML

- **Capability to predict and set accurate ARM A72 clock gating latency to avoid over-design and achieve better speed from 50 to 150Mhz**
- **Post-route speed is improved by 40MHz with detour prediction and early fix**





Achieved 95% matching on A72

Conclusion

- **Five semiconductor industry trends, issues and solutions are discussed: area, performance and power scaling, heterogeneous 3D integration and Machine Learning**
- **Physical design and EDA play even more critical roles to extend Moore's law and to enable highly integrated complex 3D SOC chips**